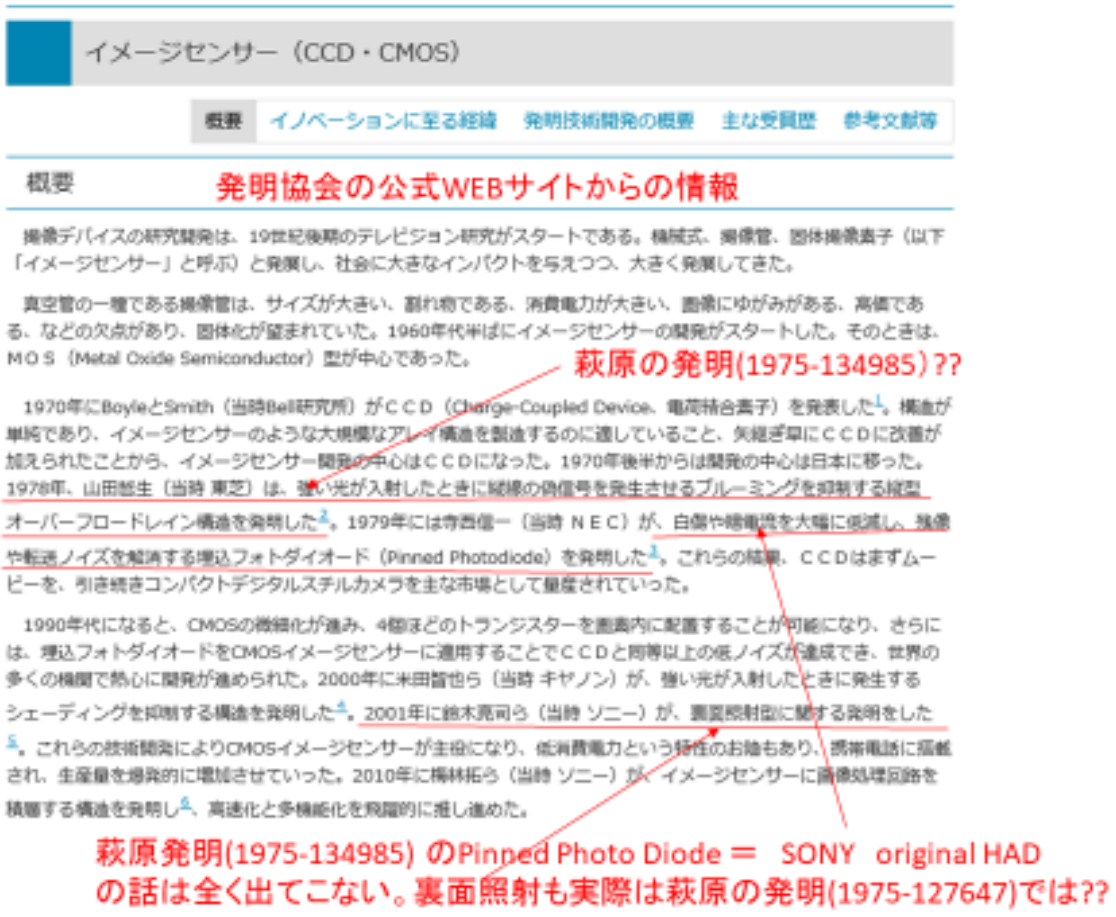
Japanese Official Invention Acknowledgement WEB site

See http://koueki.jiii.or.jp/innovation100/innovation_detail.php?eid=00059&test=open&age=



This Japanese Official Invention Acknowledgement WEB site, written in Japanese, says,

(1) The vertical Overflow drain was invented by Yamada-san of Toshiba in 1979.
(2) The pinned photo diode was invented by Teranishi-san of NEC in 1979.
(3) The back-light illumination image sensor was invented by Suzuki-san of Sony in 2001.

But Hagiwara believes that

(1) Hagiwara invented in 1975 the vertical Overflow drain , NOT Yamada-san of Toshiba in 1979.
(2) Hagiwara invented in 1975 the pinned photo diode, NOT Teranishi-san of NEC in 1979.
(3) Hagiwara invented in 1975 the back-light illumination image sensor, NOT Suzuki-san of Sony in 2001.

Which one is the truth ? Please judge for yourself.

Yoshiaki Hagiwara visited his friends in Sony Kumamoto Technology Center on November 19, 2018.

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

This is a commonly misunderstood misused set of terminologies.

First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

share edit

edited Aug 16 at 19:17

answered Sep 21 '13 at 14:34

placeholder

27.3k ● 8 ● 49 ● 97

It is important that this reply stand for context and to correct for a historical error and misreporting. One cannot understate the importance of how significant his techniques and efforts have been. Even if this doesn't align with the EE.SE . In the previous form of my answer, I was reporting on the narrative that has been promoted in the image design community. Attribution is imortant.
– placeholder Aug 16 at 19:20

A03_Hagiwara invented the Pinned Photo Diode in 1975.

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Evidence that Hagiwara invented the Pinned Photo Diode in 1975.

Yoshiaki Hagiwara, Ph.D. IEEE Life Fellow

****

Evidence that Hagiwara at Sony is the true inventor of the Pinned Photo Diode is given by the two Japanese patents Hagiwara filed in 1975 at Sony, Japanese Patent (1975-127647) and (1975-134985). The evidence is described in details in these two Hagiwara 1975 patents.

In 1978 Sony announced a new video camera in Tokyo and New York Press Conferences at the same date, one held by Sony Chairman Akio Morita in New York and the other one held by Sony President Kazuo Iwama in Tokyo at the same date in 1978.

The video camera announced in the two Press Conference was built with the Frame Transfer CCD image sensor with the Pinned Photo Diode light detecting photo sensing picture cell structure that Hagiwara invented in 1975, which has a very light sensitivity, a very low noise and a very low image lag features.

The figures N0.1 thru No.5 in Hagiwara 1975 patent (1975-134985) explained in details an example of the interline transfer CCD image sensor application with the Hagiwara invented Pinned Photo Diode.

Sony engineers, after the 1978 Press Conferences in Tokyo and New York, worked hard for, and succeeded to acquire, the production and the reliability technolgy of the CCD video camera of the interline transfer CCD image sensor application with the Pinned Photo Diode light detecting picture cell structure with the vertical overflow drain function built in each P+NPNsub junction (thyristor) type PPD.

With the diligent SONY engineers efforts, SONY could produce the portable Passport size Compact CCD image sensor video camera, with the Pinned Photo Diode (PPD) that Hagiwara invented in 1975.
And at the same time, Sony filed a trading name officially, which is the SONY Brand Name of " Sony original HAD sensor " .

A03_Hagiwara invented the Pinned Photo Diode in 1975.

With the help of the Hagiwara invented Pinned Photo Diode, which was now called as " Sony original HAD sensor " with the strong SONY original sales features of high light sensitivity, low noise and no image lag characteristics, Sony could become soon very dominant and strong over the world consumer video camera markets.

The feature of no image lag characteristics in the Hagiwara invented Pinned Photo Diode is explained and shown in details, as an example application case, in the figure No.6 of Hagiwara 1975 Japanese Patent (1975-134985) and also in the figure No.7 of Hagiwara 1975 Japanese Patent (1975-127647) in details.

Hagiwara 1975 Japanese Patent (1975-127647) proposed a Back Light illumiantion type light detecting photo sensing picture cell structure with the buried layer type photo signal charge storage. And in the figure No.7 of Hagiwara 1975 Japanese Patent (1975-127647) was shown clearly how the signal charge in the buried storage layer are trasfered completely to the region under the charge transfer gate formed on the front side of the silicon wafer. This means clearly the light sensing picture cell structure, which is now worldly called as the Pinned Photo Diode, has the very important feature of no image lag characteristics.

The patent claim descriptions and the patent figures for possible patent application examples given in details in these two Hagiwara 1975 Japanese patents (1975-127647) and (1975-134985) support the fact that Hagiwara is the true inventor of Pinned Photo Diode.

In conclusion, it is a clear cool fact that Hagiwara at Sony is the true inventor of the Pinned Photo Diode. The Haiwara patents claims that the light detecting picture cell structure (now called as the Pinned Photo Diode) can be applied to any kind of charge transfer devices (CTD) which includes the BBD type, the classical MOS type, the CCD type and the modern CMOS image sensor type charge transfer devices.

Hagiwara proposed the Pinned Photo Diode with P+NPNsub junction (thyrisor) type light detecting picture cell structure with the vertical over flow drain for the first time in the world.

A03_Hagiwara invented the Pinned Photo Diode in 1975.

Moreoever, Hagiwara proposed in the Japanese patent application example of figure No.7 of Japanse patent (1975-126747) the Back Light illumination Pinned Photo Diode (PPD) type Light Detecting Picture Cell Structure for the first time in the world.

Moreoever, Hagiwara proposed in the 1975 patent application example of figure No.4 of Japanse patent (1975-134985) the Schottky Barrier type Light Detecting Picture Cell structure in the Interline transfer type CCD image sensor applicaiton for the first time in the world.

However last year Hagiwara learned a very surprising news：

****
2017 Queen Elizabeth Prize for Engineering Foundation.
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The winners of the 2017 Queen Elizabeth Prize for Engineering Foundation were：

(1) George E. Smith for the CCD image sensor invention

(2) Michael Tompsett for the CCD image sensor development.

(3) Nobukazu Teranishi for the invention
of the pinned photodiode (PPD) and

(4) Eric Fossum for developing the CMOS image sensor.

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Hagiwara, as the true inventor of the Pinned Photo Diode, got really surprized at the announcement that Teranishi was awarded for the invention of the pinned photodiode(PPD).

And many SONY dilligent engineers working for the compact digital CMOS image sensors got really surprized at the announcement that Fossum was awarded for developing the CMOS image sensor.

A03_Hagiwara invented the Pinned Photo Diode in 1975.

The truth is that Teranish did not invent the PPD. Teranish only published in his 1982 IEDM paper the image lag free interline CCD image sensor with the PPD light detecting photo sensor structure that was invented by Hagiwara in 1975. Hagiwara 1975 patents clearly defined the image lag free interline transfer CCD image sensor as an application example in his 1975 patent claims. And the first image lag Interline transfer CCD image was designed by Hagiwara and developed by Sony deligent engineer team in 1980 with the transparent electrode type MOS type light detectiong structure with CCD charge transfer mode and with the lateral overflow drain function.

Fossum wrote a paper on "Active Pixel Sensors: Are CCD's dinosaurs ?" , in Proc. SPIE, Vol.1900, pp.2-14, 1993. However, the three transistor type active circuit was already invented by Bill Regitz of Honeywell in 1969. This active pixel sensors was not Fossum invention. Fossum actually did not develop the active pixel sensors either. Sony dilligent engineerings did.

Hitachi MOS Image Sensor Engineers and Intel MOS Process Engineers all knew that eventually scaled down MOS Process Technology will conquer all other kinds of Process Technologies including CCD image sensor technology because of the power consideration and scaled down dimensional advantage of CMOS process technology. The three transistor CMOS active picture cell was already invented as, since the three-transistor circuit is identical to, the three-transitor circuit of the DRAM cell with the active source follower type current amplification. Fossum was just a commentator in his SPIE 1993 paper above. Fossum was just emphasizing the well understood fact and speculations that the original image sensor experts all knew in 1970s. Fossum did not invent active pixel sensors. Peter Noble did. Fossum actually did not develop the active pixel sensors himself either.

Sony diligent engineerings developped the active pixel Pinned Photo Diode type Light detecting photo sensors for compact digital CMOS image sensors with the Back Light Illumination.

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A Pinned Photo Diode of the NPNN+ junction type

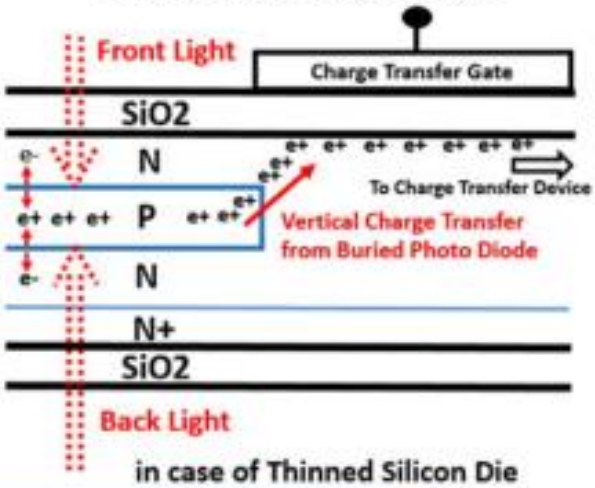
with vertical charge transfer function.

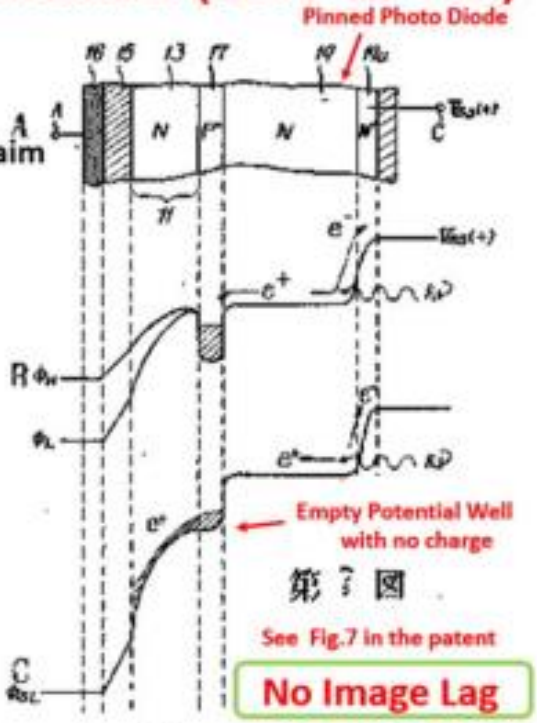
See Japanese Patent Document Number (1975-127647)

File	1975-127647	Filed	1975/10/23
Public	1975-051816	Public	1977/04/26

A Pinned Photo Diode defined in the Patent Claim

The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.





No Image Lag

SONY HAD and PPD are the same thing !

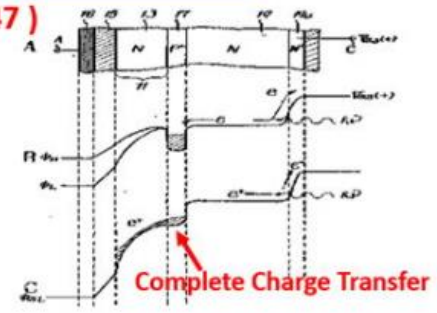
PPD in Complete Charge Transfer Mode

A Pinned Photo Diode of the N+NPNN+ junction type

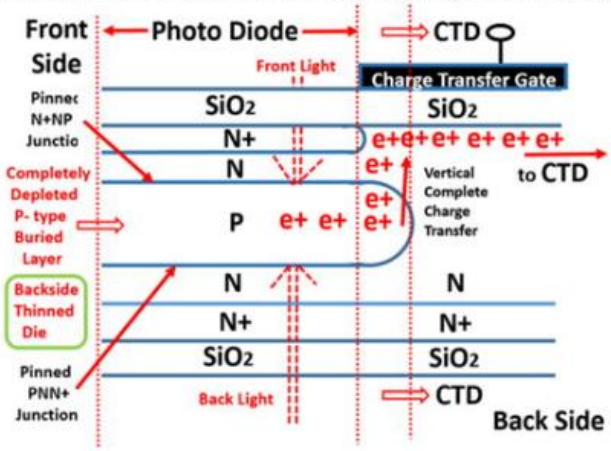
See Japanese Patent Document Number (1975-127647)

with Vertical Complete Charge Transfer Function.

File	1975-127647	Filed	1975/10/23
Public	1975-051816	Public	1977/04/26



A Pinned Photo Diode defined in the Patent Claim



The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

特許請求範囲

(1)半導体基体の一方の主面側に、
(2)絶縁膜を介して電荷転送用電極が被着配列される
(3)1の導電型の転送領域が形成され、
(4)之より上記半導体基体の他方の主面側に
(5)上記転送領域に接する他の導電型の領域と
(6)該領域に接する1の導電型の領域とより成る
(7)受光領域が形成され、
(8)上記転送用電極に所要の電圧を印加することにより、
(9)上記受光領域に蓄積した電荷を
(10)上記転送領域に転送し、上記電荷転送用電極に
(11)上記所要の電圧とは異るクロック電圧を印加して
(12)上記基体の上記一方の主面に沿って
(13)電荷の転送を行うようにしたことを
(14)特徴とする固体撮像装置。

Patent Claims defined in Japanese

SONY HAD and PPD are the same thing !

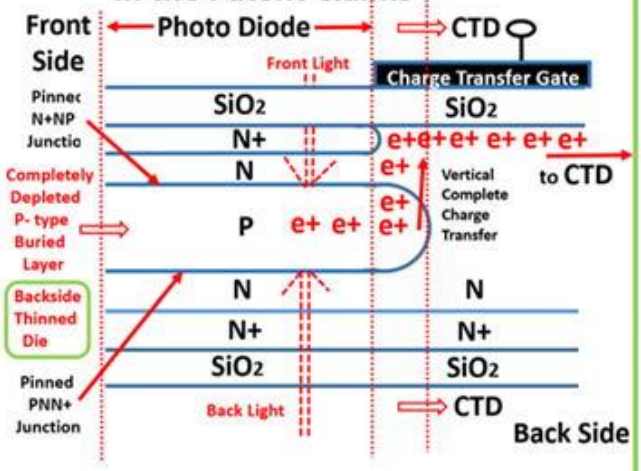
PPD in Complete Charge Transfer Mode

A Pinned Photo Diode of the N+NPNN+ junction type

See Japanese Patent (1975-127647)
with Vertical Complete Charge Transfer Function.

File	1975-127647	Filed	1975/10/23
Public	1975-051816	Public	1977/04/26

A Pinned Photo Diode defined in the Patent Claims



The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

SONY HAD and PPD are the same thing !

Patent Claims

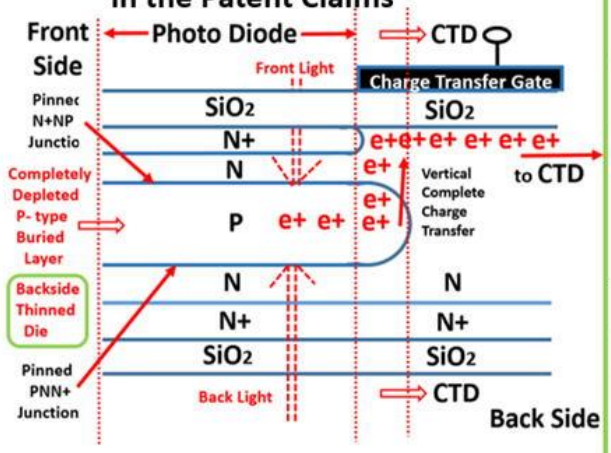
(1)On the front side surface of the semiconductor substrate die (Nsub), Here Nsub can be chosen for easy-understanding. The substrate can be a P-type substrate (Psub) but will make pictures more confusing and complex.)
(2) the charge transfer MOS gate (CTG) electrode is formed on the oxide insulator (SiO2) layer Which is formed on the surface of the substrate die Nsub. This MOS gate now is a PMOS type gate.
(3) The first doping type region (N) is formed to store and transfer signal charges under the CTG electrode. For easy-understanding, this first region can be an N-well in the N-sub type substrate die.
(4) Besides that, along the backside surface of the semiconductor substrate Nsub ,
(5) another region (P) of another doping type is formed in the substrate die(Nsub), which is placed adjacent to the charge transfer region under the CTG. This second region(P) can be formed by self-aligned deep ion-implantation to the surface type PMOS charge transfer polysilicon electrode. So this second region (P) is a buriedregion inside the Nsub and just under the first region(N).

A Pinned Photo Diode of the N+NPNN+ junction type

See Japanese Patent (1975-127647)
with Vertical Complete Charge Transfer Function.

File	1975-127647	Filed	1975/10/23
Public	1975-051816	Public	1977/04/26

A Pinned Photo Diode defined in the Patent Claims



The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

SONY HAD and PPD are the same thing !

(6) With the first region (N) ,
(7) this second region (P) in the substrate die Nsub makes a light detecting photo diode. which is an NPNsub junction type Pinned Photo Diode.
(8) By applying a proper voltage of one-shot pulse to the Charge Transfer Gate (CTG) electrode,
(9) the photo signal charge carriers stored in the photo storage region, that is, in the NPN type Pinned Photo Diode,
(10) Are to be transferred to the adjacent charge storage region under the oxide layer of the CTG.
(11) Then, by applying on the CTG electrode different clock voltage, (which is not the one-shot pulse applied before,) the signal charge carriers under the CTG are transferred further along to the nearby charge transfer device (CTD). This CTD can be either a CCD type or a CMOS type.
(12) Along the front side surface of the region N,
(13) the signal charge carriers are to be transferred to the adjacent CCD type CTD or CMOS type CTD.
(14) The combined solid state image sensor structure, with these features, including all its usage and operations (of the Photo Diode and Charge Transfer Device defined above) is in the scope of the patent claims defined above.

A Pinned Photo Diode of the P+N-PNsub junction (thyristor) type

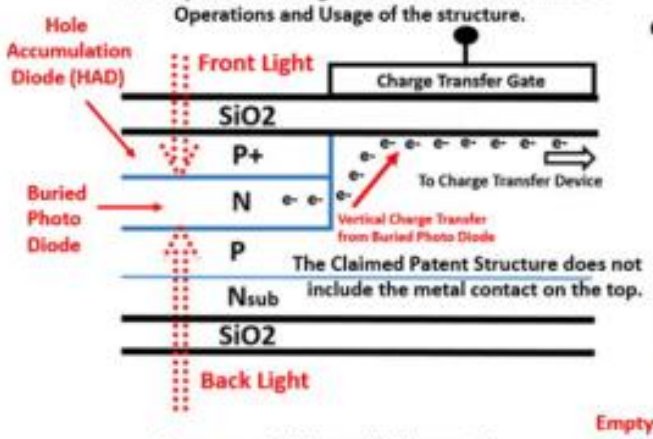
with vertical overflow drain function invented by Hagiwara 1975

See Japanese Patent Document Number (1975-134985)

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

A Pinned Photo Diode defined in the Patent Claims

The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

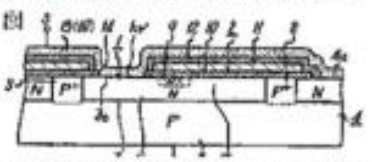


in case of Thinned Silicon Die

SONY HAD and PPD are the same thing !

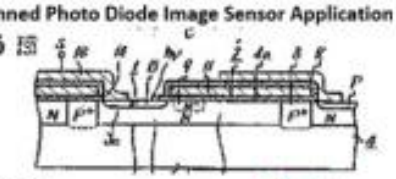
One Schottky Barrier Image Sensor Application

第 4 図

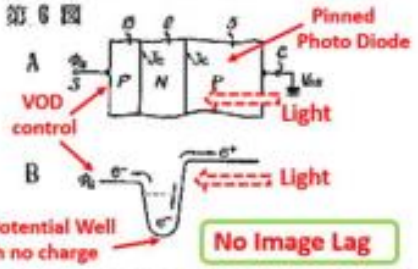


One Pinned Photo Diode Image Sensor Application

第 5 図



第 6 図



No Image Lag

PPD in Complete Charge Transfer Mode

A Pinned Photo Diode of the P+N-PNsubN+ junction (thyristor) type

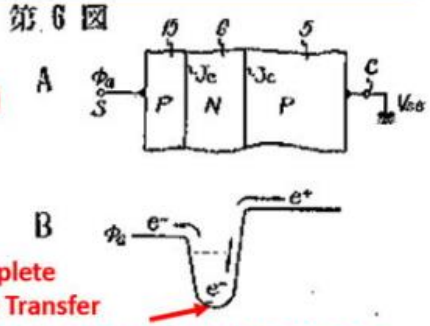
with vertical overflow drain function invented by Hagiwara 1975

See Japanese Patent Document Number (1975-134985)

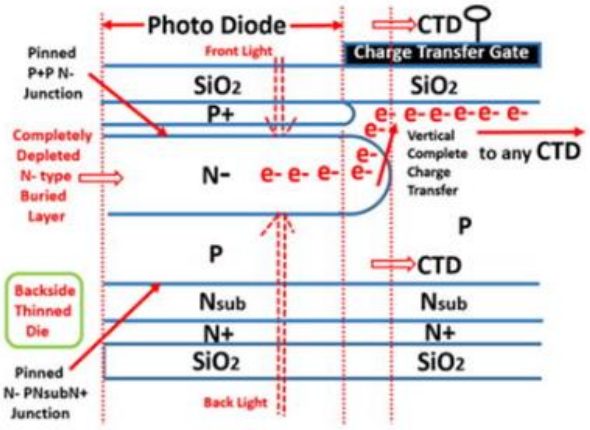
File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

A Pinned Photo Diode defined in the Patent Claims

第 6 図



Empty Potential Well with completely majority-carrier depleted base signal charge storage area.



The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

SONY HAD and PPD are the same thing !

特許請求範囲

(1)半導体基体に、
(2)第1の導電型の第1半導体領域と、
(3)之の上に形成された第2導電型の第2半導体領域
(4)とが形成されて光感知部と
(5)之よりの電荷を転送する電荷転送部とが
(6)上記半導体基体の主面に沿う如く配置されて成る
(7)固体撮像装置に於いて、
(8)上記光感知部の上記第2半導体領域に
(9)整流性接合が形成され、
(10)該接合をエミッタ接合とし、
(11)上記第1及び第2半導体領域間の接合を
(12)コレクタ接合とするトランジスタを形成し、
(13)該トランジスタのベースとなる上記第2半導体領域に
(14)光学像に応じた電荷を蓄積し、
(15)ここに蓄積された電荷を上記転送部に移行させて、
(16)その転送を行うようにしたことを
(17)特徴とする固体撮像装置。

Patent Claims defined in Japanese

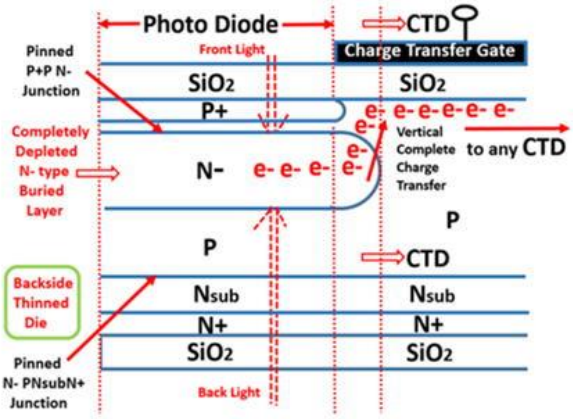
A Pinned Photo Diode of the P+N-PNsubN+ junction (thyristor) type

with vertical overflow drain function invented by Hagiwara 1975

See Japanese Patent Document Number (1975-134985)

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

A Pinned Photo Diode defined in the Patent Claims



The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

SONY HAD and PPD are the same thing !

Patent Claims

(1)In a semiconductor substrate die (Nsub),
(2) the first type semiconductor region (P) is formed. This first region P can be a P-well.
(3) And the second region (N-) of the second type is formed in the first region (P) .
(4) The two regions (N and P) together form a light detecting photo diode structure (NP).
(5) A charge transfer structure (CTD), receiving the photo charge from the NP junction,
(6) is formed along the front surface of the semiconductor substrate die (Nsub).
This charge transfer structure can be just one charge transfer gate electrode for the MOS type charge transfer device or a series of many numbers of charge transfer gate electrodes adjacent to each other in a line that forms a CCD type charge transfer device (CTD).
(7) In so-defined solid state image sensor,
(8) upon the second region (N) of the photo sensing element structure (NP),
(9) another rectifying junction is formed.

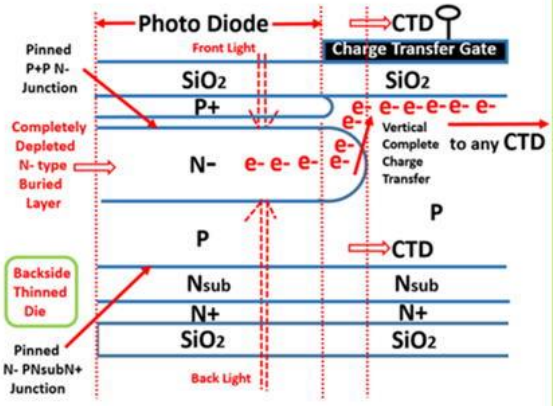
A Pinned Photo Diode of the P+N-PNsubN+ junction (thyristor) type

with vertical overflow drain function invented by Hagiwara 1975

See Japanese Patent Document Number (1975-134985)

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

A Pinned Photo Diode defined in the Patent Claims



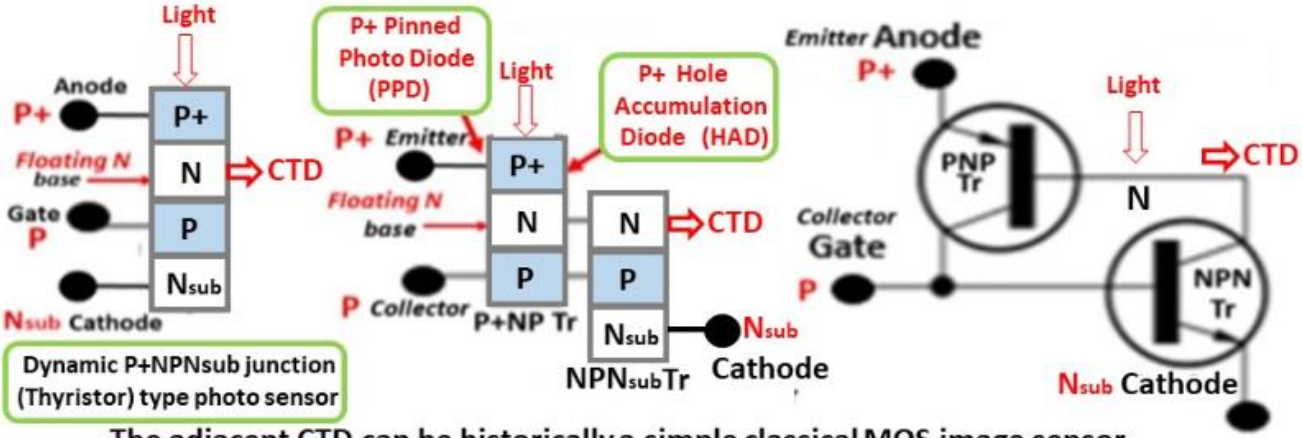
The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

SONY HAD and PPD are the same thing !

(10) This junction (P+N) can be called as an emitter junction of the P+NP junction type transistor structure for convenience.
(11) Furthermore the junction (NP) composed of the second region (N) and the first region (N)
(12) Can be called as a collector junction (NP) of the P+NP junction type transistor structure.
(13) The second region (N), which can be now called as the base region of the P+NP junction type photo transistor structure ,
(14) Is the photo-charge storage area of the majority carriers, generated according to the illuminated optical image information.
(15) After transferring the photo signal charge from the base region (N) to the adjacent charge transfer structure (CTD),
(16) The adjacent charge transfer) structure further performs the subsequent proper charge transfer operations to the final chip outlet.
(17) So-define solid state light detecting sensor structure is in the scope of the patent claims.

P+NPNsub junction (Thyristor) Type Photo Sensing Structure invented by Hagiwara in 1975 for the built-in vertical overflow drain (VOD) function and excellent blue light sensitivity with no image lag.

Pinned Photo Diode (PPD) and **Sony original Hole Accumulation Diode (HAD)**, patented by Hagiwara at SONY in 1975 Japanese Patent (JAP 50-134985), originally defined as a dynamic photo sensing P+NPNsub junction Structure with the storage electron charge in the base N region to be transferred completely, from the N charge storage region in complete majority-carrier depletion mode, to the adjacent charge transfer device (CTD) to realize no image lag pictures.

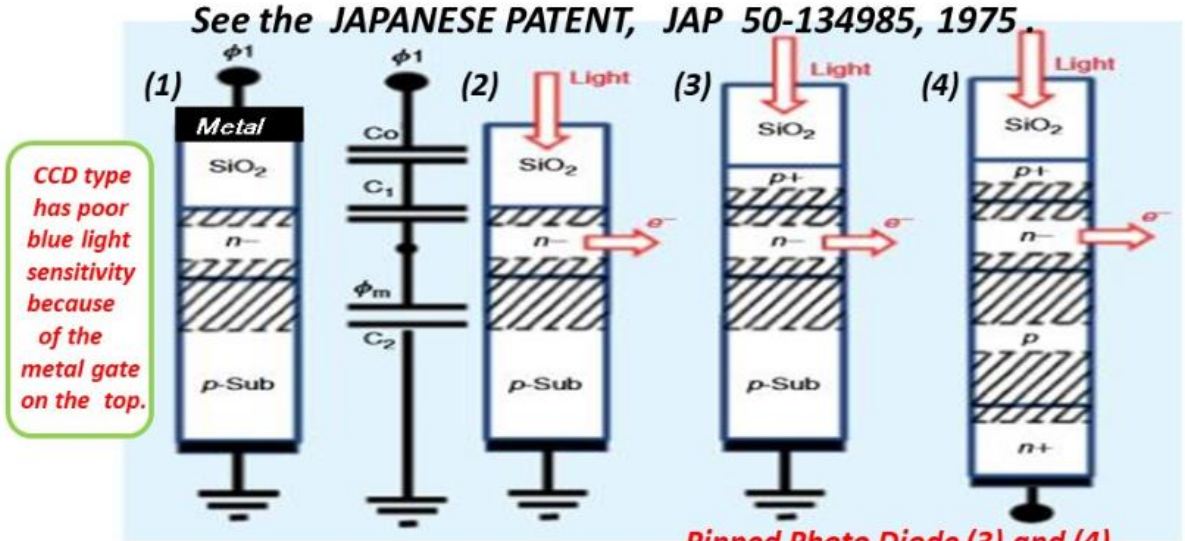


The adjacent CTD can be historically a simple classical MOS image sensor, Bucket Brigate(BBD) type image sensor, Frame Transfer type CCD imager, Interline Transfer type CCD imager, or current CMOS technology active image sensor.

PPD and **Sony HAD** are the same thing, both invented by Hagiwara at Sony in 1975.

Hagiwara at Sony invented the pinned photo diode 1975.

See the JAPANESE PATENT, JAP 50-134985, 1975.



Pinned Photo Diode (3) and (4) invented by Hagiwara 1975

(1) Buried Channel CCD type MOS capacitor sensor proposed in 1969

(2) Dynamic N-/P junction photo sensor conceived by Hagiwara 1975

(3) Dynamic P+/N-/P junction photo sensor by Hagiwara in 1975

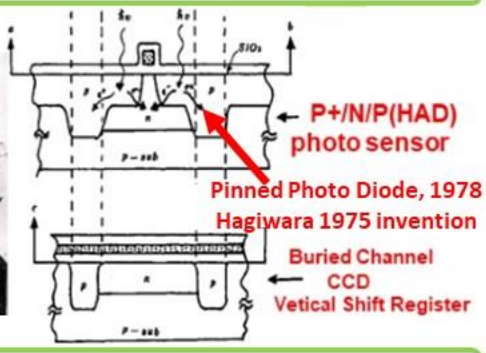
(4) Dynamic P+/N-/P/Nsub junction photo sensor by Hagiwara in 1975

The key idea is lightly doped N-type storage layer in the pinned photo diode (3) and (4), for complete charge transfer with no image lag, similar to the lightly doped N- type buried layer of BCCD of type(1).

Reference: IEEE Solid-STATE CIRCUITS MAGAZINE, SUMMER 2013 issue, pp. 6

SONY original 570H x 498 V One-chip FT CCD Image sensor with Pinned Photo Diode, 1978

In 1978, at Sony Tokyo Press Conference by Kazuo Iwama, and
at Sony New York Press Conference by Akio Morita,



Sony announced the Video Camera and 8 mm VTR in one box.

High quality pictures of current SONY HAD CMOS Image sensor with Pinned Photo Diode

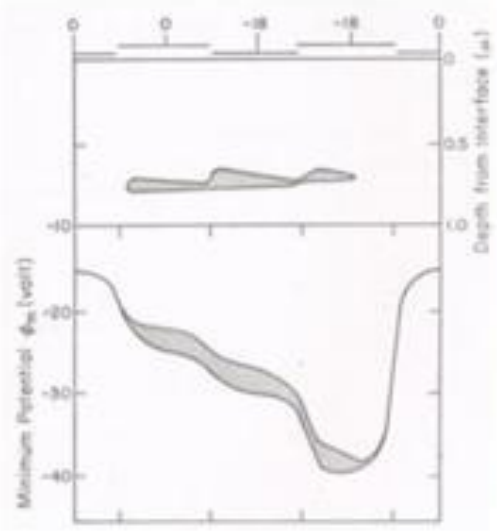
Front-illuminated CIS **Back-illuminated CIS**

Sony original HAD sensor and the pinned photo diode are the same thing.
Both are Hagiwara 1975 invention. See JAPANESE PATENT JAP 50-134985, Nov.10, 1975

Charge-Coupled Devices and Applications

Chairman
Lewis M. Terman

My PhD thesis paper
on buried channel CCD
at ISSCC1974, in Philadelphia, USA



Prof. T. C. McGill

Prof. C. A. Mead

Prof.C.A.Mead and Hagiwara (Daimon) at CalTech , Sept 1972 .

128-Bit Multicomparator

CARVER A. MEAD, RICHARD D. PASHLEY, MEMBER, IEEE, LEE D. BRITTON, YOSHIAKI T. DAIMON, AND STEWART F. SANDO, JR., MEMBER, IEEE

Abstract—A 128-bit multicomparator was designed to perform the search-sort function on arbitrary length data strings. Devices can be cascaded for longer block lengths or paralleled for bit-parallel, word-serial applications. The circuit utilizes a 3-phase static-dynamic shift register cell for data handling and a unique gated EXCLUSIVE-NOR circuit to accomplish the compare function. The compare operation is performed bit parallel between a "data" register and a "key" register with a third "mask" register containing DON'T CARE bits that disable the comparator. The multicomparator was fabricated using p-channel silicon-gate metal-oxide-semiconductor (MOS) technology on a 107 × 150 mil chip containing 3350 devices. With transistor-transistor logic (TTL) input, data rates in excess of 2 MHz have been attained. The average power dissipation was 250 mW in the dynamic mode and 300 mW in the static mode.

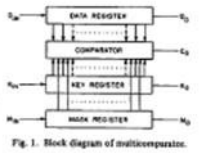


Fig. 1. Block diagram of multicomparator.

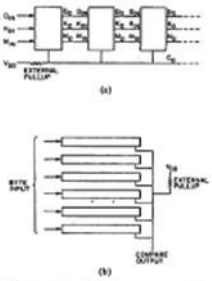


Fig. 2. Possible connections of multicomparator. (a) Cascaded. (b) Bit-parallel, word-serial.

INTRODUCTION

OVER the past several years, there have been significant amounts of energy devoted to the fabrication of larger and faster semiconductor memories and conventional central processing units (CPU's) in chip form. In the process, many other applications of large-scale integration (LSI) to computer architecture have been neglected [1]. LSI has removed the technological distinction between logic and memory. It is now economically feasible to decentralize the CPU of a computer by replacing much of its maintenance software with functional hardware to improve system efficiency. Presently, an inordinate amount of processing time is spent on organizing and accessing files in peripherals. Peripherals are usually controlled directly by the CPU and have little or no associated logic of their own. A great improvement in this situation can be made by developing peripheral logic units. This would allow each peripheral to accomplish its own internal processing and thus reduce CPU housekeeping duties. This paper describes a 128-bit multicomparator that is designed to perform the search-sort function.

The block diagram of the multicomparator is shown in Fig. 1. The circuit consists of three independently clocked static-dynamic shift registers with associated EXCLUSIVE-NOR gating. In operation, the device indicates a match between the data word and the unmasked bits of the key word. The multicomparator is loaded with a key word by serially shifting the word into the key register and locking the register in static mode. While the key word is being loaded, the comparator is enabled by entering zeros[1] in the appropriate locations of the mask register. Masking allows the multicomparator to search for bit strings of varying length and composition. For example, assume it is necessary to search for all words containing a specific 113-bit code. By entering the 113-bit code in the key register and masking out the rest of the comparator, the multicomparator is conformed to search for this code wherever it occurs in the data file. Once the multicomparator is loaded with "key" and "mask" words, the file being searched is serially shifted through the data register. The data words are compared in bit parallel with the unmasked bits of the key word as they pass through the data register. When a match is found, the compare output goes high.

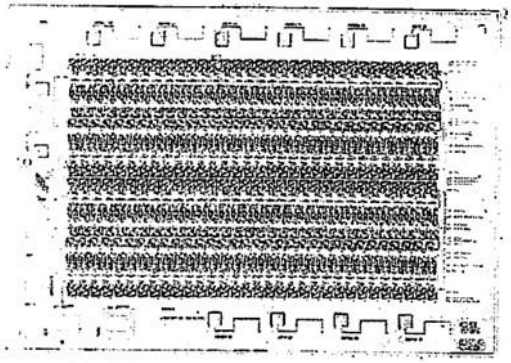
Large multicomparators can be constructed of the 128-bit circuits. Cascaded [Fig. 2(a)], the comparator can be used to search for words longer than 128 bits. By implementing multicomparators in parallel [Fig. 2(b)], a word-serial, bit-parallel

Manuscript received March 15, 1976; revised July 16, 1976.

C. A. Mead is with the California Institute of Technology, Pasadena, CA 91125.
R. D. Pashley and S. F. Sando, Jr., are with the Intel Corporation, Santa Clara, CA.
L. D. Britton is with the Hewlett-Packard Laboratories, Cupertino, CA.
Y. T. Daimon is with the Sony Corporation, Tokyo, Japan.

[1] Voltage conventions: high="1"=V_{DD}, low="0"=V_{SS}. Note that since V_{DD} is negative for p-channel MOS and positive for n-MOS transistor-transistor logic (TTL) levels may or may not have reverse polarity depending on the processing used.

128-Bit Multicomparator chip, designed by Hagiwara et al and fabricated in Intel, 1972



Ref: IEEE Journal of Solid State Circuits, VOL.SC11,No.4, October 1976

ISSCC1989 Paper on Sony 4 M bit Fast Cache SRAM for Digital Image Sensor

A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads

FUMIO MIYAJI, YASUSHI MATSUYAMA, YOSHIKAZU KANAISHI, KATSUNORI SENOH, TAKASHI EMORI, AND YOSHIAKI HAGIWARA, MEMBER, IEEE

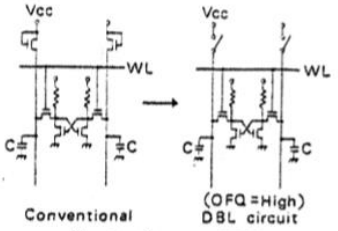


Fig. 6. Concept of DBL.

—A 25-ns 4-Mbit CMOS SRAM with 512K word × 8-bit orga- has been developed. The RAM was fabricated using a 0.5-μm and double-aluminum CMOS technology and was assembled 400-mil DIP. A small cell size of 3.6 × 5.875 μm² and a chip 46 × 17.41 mm² were obtained. A fast address access time of 25 a single 3.3-V supply voltage has been achieved using our newly dynamic bit-line load (DBL) circuit scheme incorporated with an transition detector (ATD), divided word-line structure (DWL), sense amplifier, and low-noise output circuit approach. A low current of 46 mA at 40 MHz and low standby currents of 70 μA 5 μA (CMOS) were also attained.

I. INTRODUCTION

MEMORY capacity of SRAM's has quadrupled

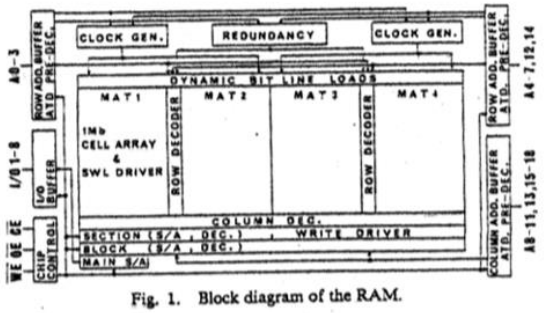
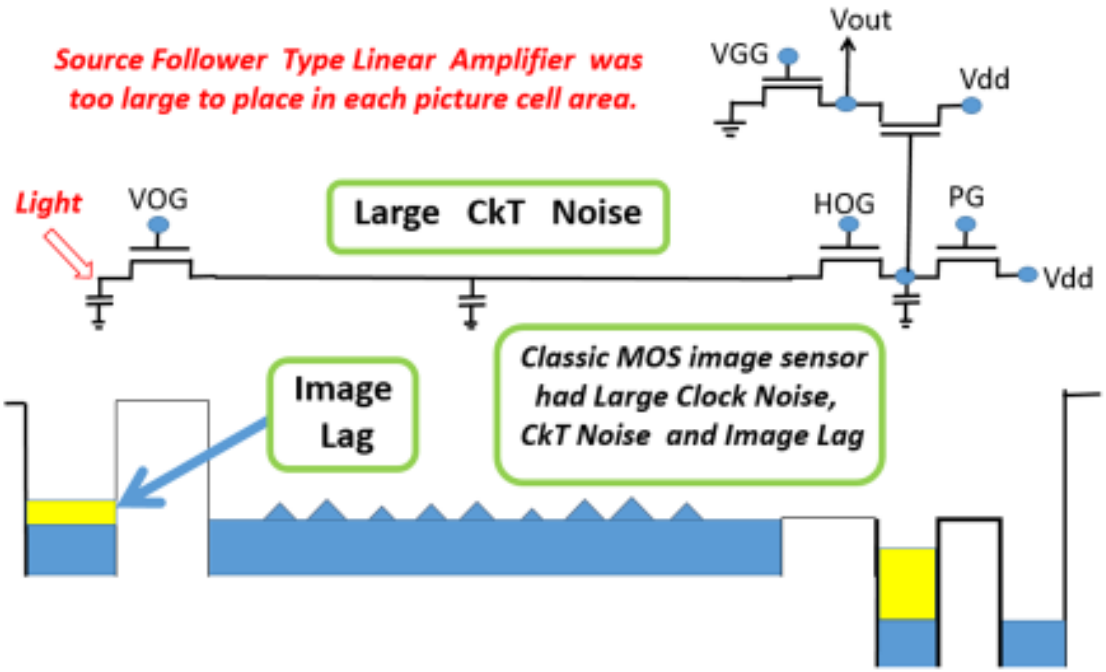


Fig. 1. Block diagram of the RAM.

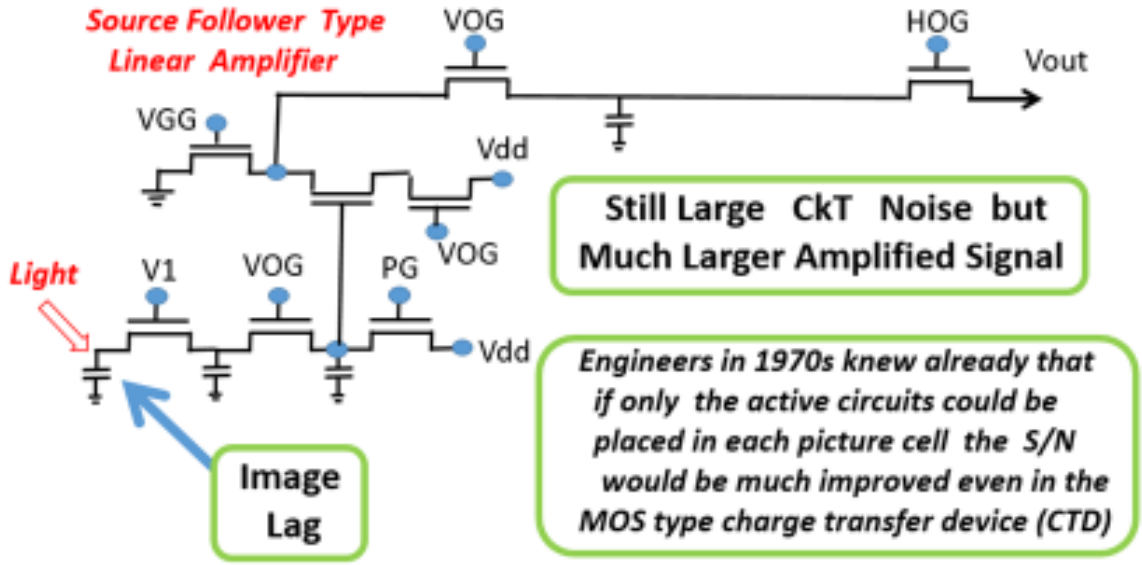
See also Journal of the Solid State Circuits, Vol. 24, No.5, October 1989

Classic MOS image sensor type Charge Transfer Device (CTD)



1 = Clock High = Switch ON ; 0 = Clock Low = Switch OFF

Active Pixel Type CMOS image sensor type Charge Transfer Device (CTD)

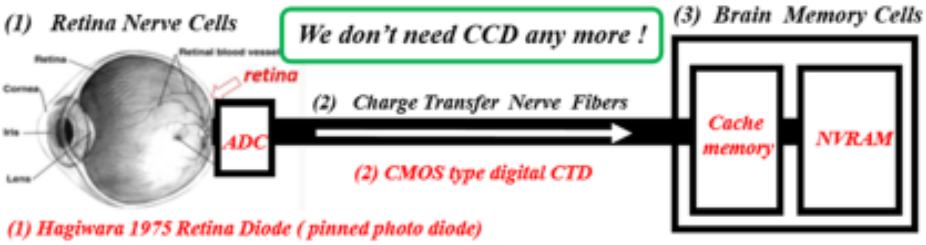


But we have to sacrifice the picture cell light detecting window area. The only Solution would be the back light illumination with thinned die.

Hagiwara Patent (1975 – 127947) invention already gave the solution with the Image Lag Free Pinned Photo Diode with Back Light Illumination.

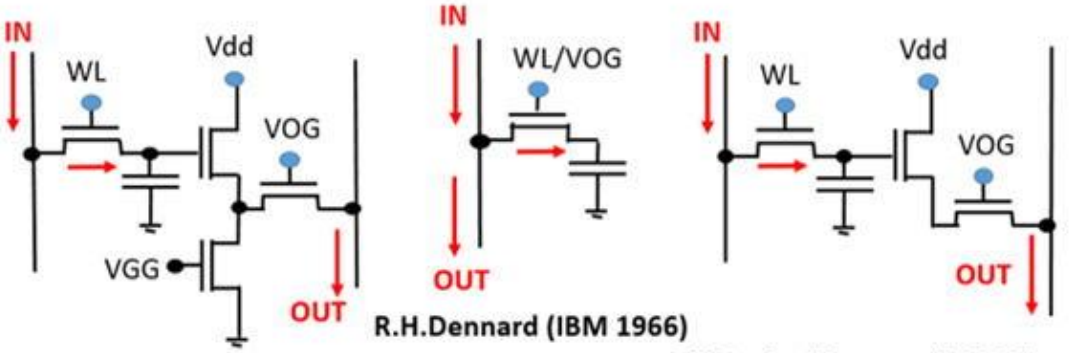
Digital CMOS image sensor

is made of (1) Pinned Photo Diode (2) Charge Transfer Device(CTD) (3) A/D converter (4) Fast Cache SRAM and (5) Slow Nonvolatile RAM



Pinned Photo Diode for DCIS was invented by Hagiwara in 1975.
Back illuminated CMOS image sensor was developed by Sony Engineers
First A/D converter for DCIS was first developed by Sony Engineers.
First Cache 4M bit SRAM for DCIS was developed by Hagiwara in 1989.
First Nonvolatile RAM for DCIS was invented by Prof. Simon Sze in 1966

History of DRAM Cell

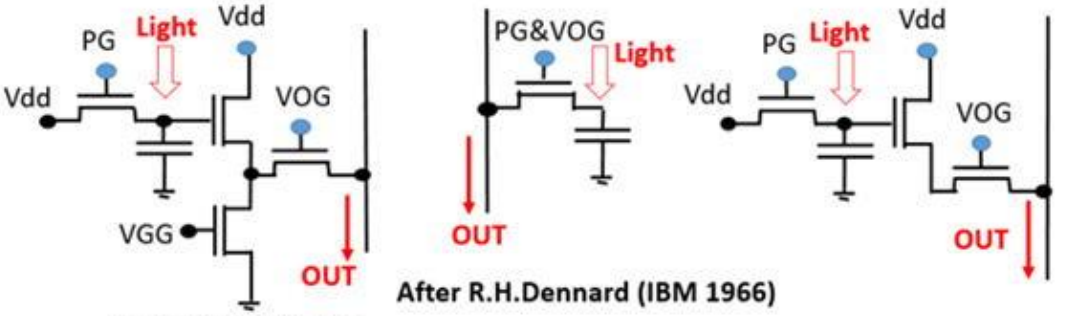


Conventional DRAM Cell before 1966

R.H.Dennard (IBM 1966)

Bill Regitz (Honeywell 1969) Intel 1101 @ISSCC1970, Philadelphia.

History of Photo Diode Cell



Conventional Active Photo Diode Cell before 1966

After R.H.Dennard (IBM 1966)

After Bill Regitz (Honeywell 1969) Intel 1101 @ISSCC1970, Philadelphia.

Engineers in 1966 working on the classical MOS image sensors already knew the conventional Source Follower Type Active Picture Element Cell (Pixell) Photo Diode, by the analogy of DRAM cases as shown above. Nothing is new about the Active Picture Element Cell (Pixell) Photo Diode CMOS image sensor.

Comparison of four types of Light Detecting Sensor Structures

feature \ type	N+Psub	SCCD	BCCD	P+N-PNsub
Sensitivity	○	X	X	○
Image Lag	X	○	○	○
Surface Dark Current	X	X	X	○
Surface Trap Noise	X	X	○	○
Vertical OFD Function	X	X	X	○

Hagiwara invented the P+N-PNsub type Pinned Photo Diode

See Japanese Patents (JA 1975-127647) and (JA 1975-134985)

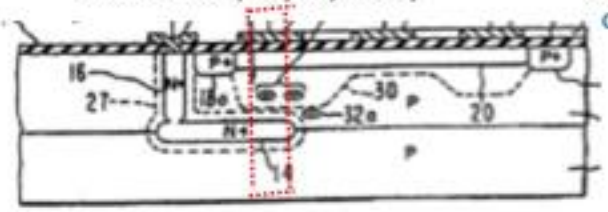
The Pinned Photo Diode is much better than the CCD type light detector.
The Active Pixell CMOS type DIGITAL CTD is much better than the CCD type ANALOG CTD.

In the total performance, CMOS Image sensor in digital system is considered to be much better than CCD image sensor in analog charge transfer system now.

Fairchild_to_Sony_Patent_War_1991_to2000

SONY- Fairchild Patent War (1991-2001) on Pinned Photo Diode with Vertical OFD

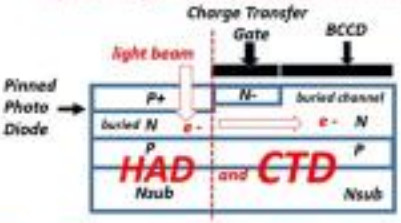
Fairchild Early Patent on CCD sensor with vertical OFD protection USP3896485 (July 22, 1975)



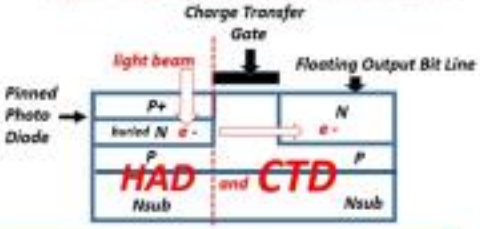
Fairchild Early Patent, filed on July 22, 1975, applied on the surface CCD type MOS capacitance with poor blue sensitivity while Sony Hagiwara Patent, filed on Nov. 10, 1975, appiled on the Pinned Photo Diode, with good blue sensitivity and low dark current also with the built-in vertical overflow drain function, which was well known as the P+NPNsub Thyristor Punch-Thru action. Sony took more than ten years in this Patent War to challenge to explain the differences on the two image sensor structures and the two vertical overflow drain sturctures to the authorities who did not have any backgrounds on the semiconductor device physics.

Sony Hagiwara Patent on Pinned Photo Diode with P+NPNsub Thyristor type vertical OFD protection JAP50-134985 (November 10, 1975)

Case(1) *Hagiwara Diode 1975 (Sony HAD) Application with a Charge Transfer Device (a CCD type CTD case) defined in Hagiwara 1975 Japanese Patent 58-1215101*



Case(2) *Hagiwara Diode 1975 (Sony HAD) Application with a Charge Transfer Device (a CMOS type CTD case) defined in Hagiwara 1975 Japanese Patent 58-1215101*



See Hagiwara Japanese Patent Application (50-134985, 1975)

SONY- Fairchild Patent War (1991-2000) on Pinned Photo Diode with Vertical OFD

CCD特許侵害訴訟

ソニー、逆転勝訴

日刊 7/16

NY東部地裁

電子機器の基幹部品である電荷結合素子（CCD）の特許侵害訴訟を審理していた米ニューヨーク東部地裁は、ソニー（社長出井伸之氏）を訴えていた米ローラル・フェアチャイルド社の主張を退け、ソニー勝訴の判決を下した。同訴訟はソニーが特許を侵害しているとの陪審員評決が二月に出ていたが、ソニーが逆転勝訴した。フェアチャイルドは日立製作所、東芝など日欧の大手電機メーカー二十社以上を同様の趣旨で訴えており、ソニーの勝訴は他社の裁判にも影響を与えそうだ。

ソニーが十五日明らかにしたところによると、ニューヨーク東部地裁は「ソニー製のCCDはローラル・フェアチャイルド社の二件の特許に抵触しない」との判決を下し、陪審員の評決を覆した。フェアチャイルドは控訴するかどうかの態度をまだ明らかにしていないという。

CCDはカメラ一体型VTRやファクスなどの電子機器に使われる光学部品で、「電子の目」と呼ばれる重要部品。フェアチャイルドは自社が保有するCCDの製造プロセスと構造に関する二件の特許を侵害しているとして九一年九月、ソニーのほか日立、東芝、仏トムソン、松下など日欧の大手各社を訴えていた。ソニーは「当社のCCDはフェアチャイルドの特許とは異なる製造プロセスと構造を採用していると主張してきたが、その正当性が認められた」としている。ただフェアチャイルドが控訴すれば、裁判が長引く可能性も残っている。

From Japanese News Paper, July 16, 1996.

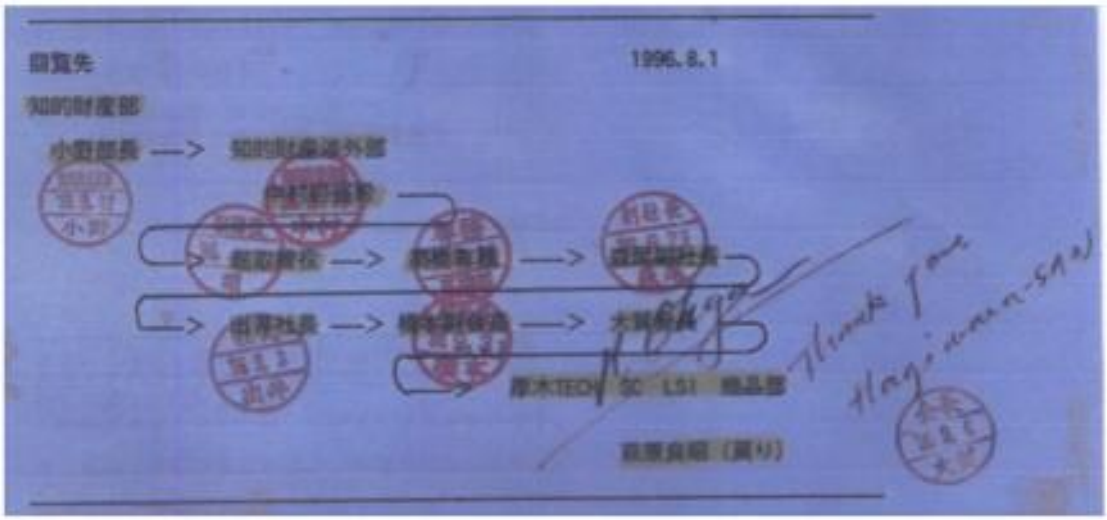
1996 年 7 月　日刊工業新聞記事から

（2000 年 1 月米国最高裁で最終決着ソニー勝訴）

In January 2000, the US supreme court made the final judgement favoring Sony claims. And the long SONY-Fairchild Patent War on the PDD with the built-in vertical overflow drain (VOD) ended.

Sony_Top_Managements_finally_acknowledged_Hagiwara

Sony won the Fairchild-Sony Patent War in the 1996 New York State Court, and Hagiwara received a Thank_YOU_NOTE from SONY TOP Managements, including Mr.Ohga(Sony Chairman) and Mr.Idei (Sony President).



The final US Supreme Court decision was made in 2000, finally after ten years of pains.

Hagiwara protected SONY Image Sensor Business by Hagiwara 1975 patents on the Pinned Photo Diode with the vertical Overflow Drain Structure.

Sony_Top_Managements_finally_acknowledged_Hagiwara_1975_Patents_on_PPD.


SONY

2000年度

発明考案実施褒賞

1級

萩原 良昭 殿

特許第1215101号

固体撮像装置

貴発明は卓越した創造性および先見性により
会社に対し顕著な貢献がありましたので
発明考案規定に基づき
ここに本賞を贈りこれを賞します

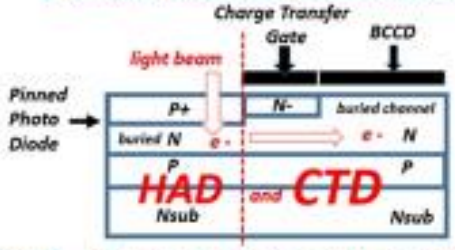
2001年4月26日

ソニー株式会社
社長

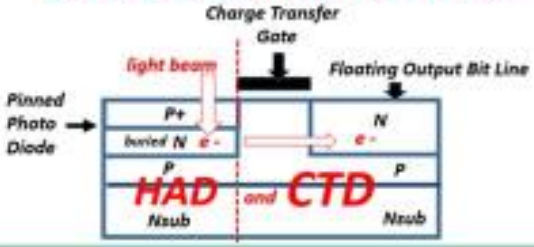
Sony Patent Acknowledgement Certificate given to Hagiwara in 2000 after the patent-war.

Hagiwara Japanese Patent (1975-134985) on the P+NPNsub junction (thyristor) type Pinned Photo Diode with the Vertical Overflow Drain (VOD) built-in Structure

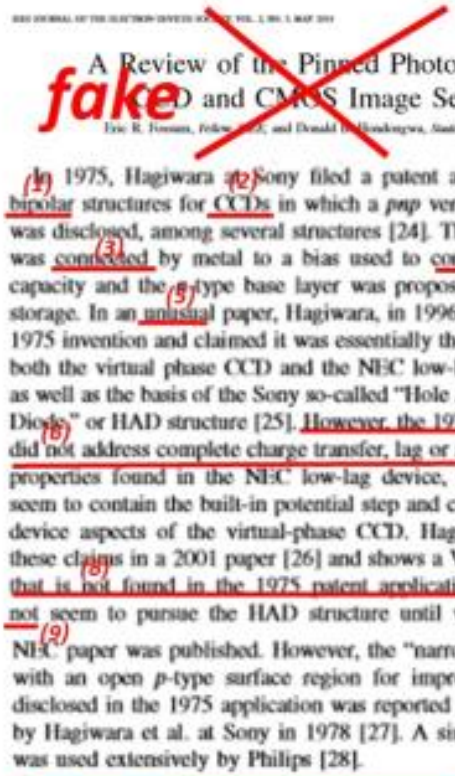
Case(1) *Hagiwara Diode 1975 (Sony HAD) Application with a Charge Transfer Device (a CCD type CTD case) defined in Hagiwara 1975 Japanese Patent 58-1215101*



Case(2) *Hagiwara Diode 1975 (Sony HAD) Application with a Charge Transfer Device (a CMOS type CTD case) defined in Hagiwara 1975 Japanese Patent 58-1215101*



Fossum 2014 fake paper attacking Hagiwara Patents


fake

A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, Fellow, IEEE, and Donald B. Hondongwa, Student Member, IEEE

In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top *p* layer was connected by metal to a bias used to control full-well capacity and the *n*-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called "Hole Accumulation Diode" or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the "narrow-gate" CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

This is a fake paper.

These (1) thru (9) statements are all biased and false . Many corrections are requested Fossum is insulting Hagiwara and SONY by making many false statements.

This is the most serious false statement.

Yes, Hagiwara 1975 addressed the Complete Charge Transfer and Image Lag and anti-blooming, by drawings of Fig.5 and Fig.6 in Hagiwara 1975 patent on the original pinned photo diode.

Evidently, Fossum has never seen Hagiwara 1975 patent. In Fossum 2014 biased fake paper, Fossum did not quote the Fig.5 and Fig.6 of 1975 Hagiwara Patent invention

See Hagiwara Japanese Patent Application (50-134985, 1975)

****

Questions by Prof. Albert Theuwissen were :

- who invented and developed the stitching technology
for large area image sensors ?

- who owns the world record in low-noise
in the voltage domain for CMOS Image Sensor (CIS) ?

****

Hagiwara believes that

Hagiwara invented it, in the Japanese 1975 patent (1975-134985) as the P+NPNsub junction (Thyristor) type Light Detecting Picture Cell Structure, and Sony diligent engineers, including Hagiwara, developed, the stitching technology for large area image sensors. SONY called it as the SONY original HAD sensor technology in SONY business. Naturally, the technical world did not use the SONY business Brand Name HAD, and called it by another name, the Pinned Photo Diode. But the Pinned Photo Diode and SONY original HAD technology are the same thing, both invented by Hagiwara in 1975.

At least, Teranishi did not invent the Pinned Photo Diode.
Hagiwara is the inventor of the Pinned Photo Diode.

Sony diligent engineers developed and now Sony owns the world record in low-noise in the voltage domain for CMOS Image Sensor (CIS) with the Pinned Photo Diode with the Back Light Illumination, that was also invented by Hagiwara of SONY in 1975 the Japanese 1975 patent (1975-127647).

At least, Fossum is not the inventor of the active image sensor picture element.Peter Noble is the inventor of the active image sensor picture element. http://www.pjwn.co.uk/

In the Fossum 2014 fake paper, Fossum attacked Hagiwara 1975 patent with lies, insulting Sony and Hagiwara honor and pride on purpose. I could not understand Fossum motivation. But I am now convinced that Fossum wanted Fossum himself to be recognized by the world, with false explanations on Fossum friend Teranishi as the TRUE inventor of the Pinned Photo Diode, NOT Hagiwara.

Fossum wanted to convince the world that Fossum himself developed the modern CMOS digital camera. But now I understand that Peter and SONY diligent engineers, including Hagiwara. This is not fair at all. It is all lies. The world should know the truth.

Until last June I did not know what is the Pinned Photo Diode. I knew SONY HAD. But I did not know myself that SONY HAD and the Pinned Photo Diode are the same thing. My friends in Sony informed me that Teranish received awards from Queen Elizabeth and Japanese Emperor as the inventor of the Pinned Photo Diode. SONY diligent engineers were not happy at all. So I began to study what is Pinned Photo Diode last June. Then I found the Fossum 2014 fake paper.

Besides, SONY won the SONY-NEC Patent war by Hagiwara 1975 patent against the Teranishi1979 patent a long time ago. So Teranish should know that Hagiwara is the inventor even though Teranishi published his work in IEDM1982. Teranishi work was just a copy of Hagiwara 1975 patents that defined as one example case of Interline CCD image sensor with the complete charge transfer mode (no image lag) P+NPNsub junction type photon detector structure, which is now called as the Pinned Photo diode.

But it is now more than four years after Fossum 2014 fake paper publication. I found this fake paper, really too late. I was very, very late since I do not belong to the image sensor community any more.

Yes, with my interests in the intelligent image sensors included, but my current major interests are in the AIP (Artificial Intelligent Partner) systems, including AI software and AI digital circuit system applications.

I try to be calm, but cannot be silent. I feel that the world should know, at least, what is the truth. I don't think I can change the past history. But people can learn the truth anytime, now and in future. Yes, many people contributed. Their diligence and efforts must be much worth recognitions.

****

http://www.aiplab.com/Hagiwara_at_Sony_is_the_true_inventor_of_Pinned_Photo_Diode.html

http://www.aiplab.com/Story_of_Pinned_Photo_Diode.html

http://www.aiplab.com/

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