A Snap-Shot CMOS Active Pixel Imager for Low-Noise, High-Speed Imaging

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Abstract

Design and performance of a 128x128 snap-shot imager implemented in a standard single-poly CMOS technology is presented. A new pixel design and clocking scheme allow the imager to provide high-quality images without motion artifacts at high shutter speeds (< 75 μsec. exposure), with low noise (< 5 e^-), immeasurable image lag, and excellent blooming protection.

Introduction

Recent advances in CMOS imager technology have enabled the development of highly integrated, ultra-low power, camera-on-a-chip with impressive imaging performance [1, 2]. However, most CMOS imagers do not support simultaneous integration of all pixels in the imager, the imager being read out in a "rolling shutter" mode. Non-simultaneous exposure leads to image distortion whenever there is relative motion between the imager and the scene. Snap-shot mode of operation (simultaneous integration) has been demonstrated with photodiode-type CMOS imager by incorporating a switched storage node inside the pixel [3, 4]. However, incomplete charge transfer leads to image lag and increased noise in these imagers. Snap-shot mode of operation is also possible with pinned photodiode pixels [5],. However, requiring non-trivial modification of the standard CMOS process.

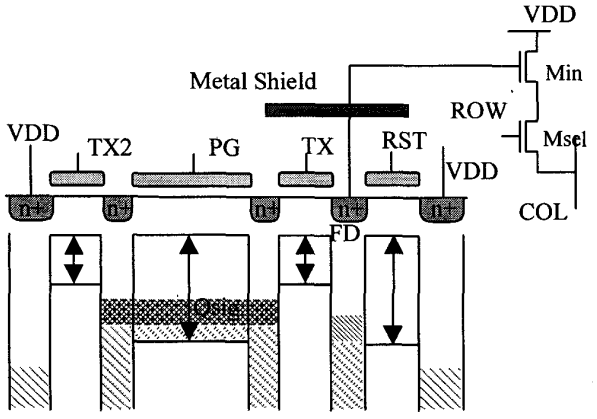

Fig. 1: Schematic of the snap-shot APS pixel. Hatched areas represent electrons

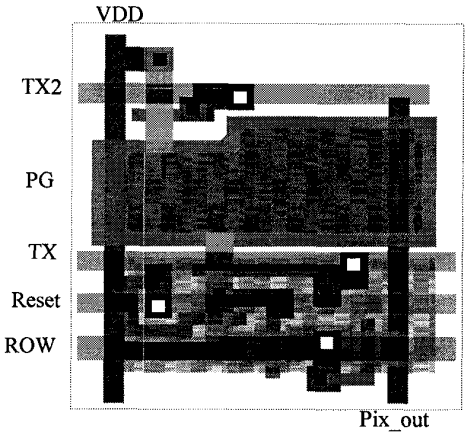

Fig. 2: Pixel layout in a single-poly CMOS process

Pixel Design & Operation

Fig. 1 shows the schematic of the snap-shot imager pixel, along with the potential well diagram. The pixel consists of a photogate (PG), two transfer gates (TX and TX2), a reset gate (RST), a metal-shielded sense node (FD), source follower input transistor (Min), and the row-select transistor (Msel). TX and TX2 are common to the entire chip and are pulsed. Snap-shot imaging (or concurrent exposure of all pixels) is achieved by simultaneously transferring the integrated charges under PG to the sense node (FD) within each pixel by momentarily pulsing TX. The sense node provides intermediate storage for the time taken by the array complete readout in row-at-a-time manner. Thus, the imager can operate with simultaneous high-speed exposure independent of the frame read time. Since FD is isolated following a charge transfer, an additional gate (TX2) is added for providing lateral anti-blooming. The resultant pixel architecture preserves the row-wise random access feature.

Fig. 2 shows the layout of a snap-shot pixel of 14.4 μm pitch, and 27% fill factor. Implementation of the pixel in single poly-silicon technology implies that the transfer gates are flanked by floating diffusions. Charge leakage from these nodes can cause excess noise and image lag. Fig. 3 shows the clocking sequence that eliminates the excess noise and image lag. In addition, minimization of floating diffusion areas also help reduce these effects.

The imager operates as follows. During exposure ($t=t_1$), both

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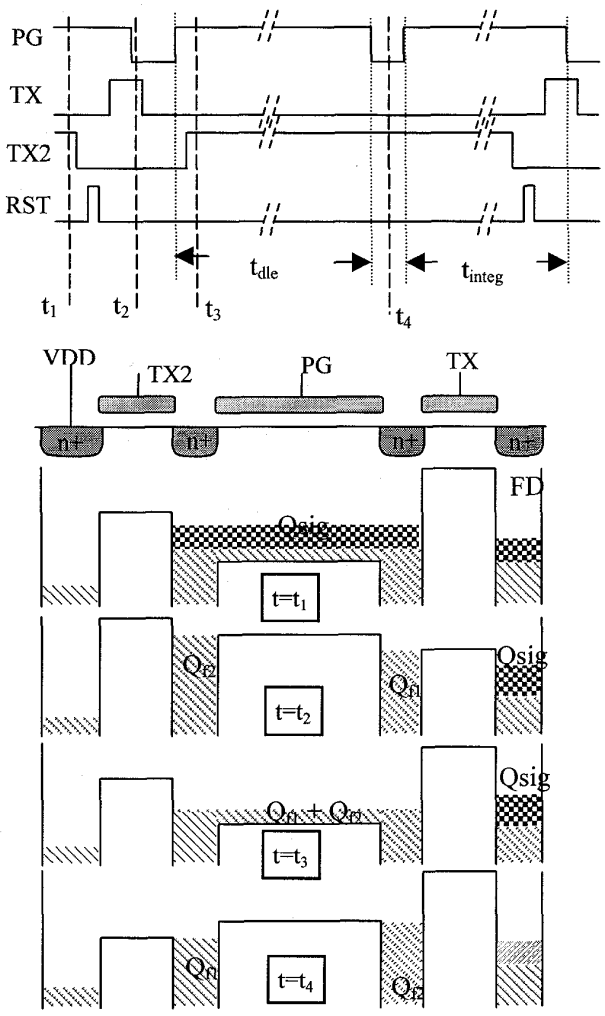

Fig. 3: Timing sequence and the potential well-diagrams during exposure, charge transfer, idling, and immediately prior to beginning an exposure

PG and TX2 are high, and TX is low. This allows the photocharges to integrate under PG, while TX provides electrical isolation to the sense node that may be storing signal charges from the previous frame. TX2 high provides anti-blooming. The exposure time is defined by the pulse duration of PG. For charge transfer ($t=t_2$), TX2 is pulsed low, TX is pulsed high just above threshold, followed by PG pulsed low. This causes the integrated charges to transfer only into the sense node, FD. The idle state ($t=t_3$) is similar to the exposure state, except that at the end of the idle state ($t=t_4$), TX2 is pulsed high to drain out the unwanted charges collected during the idle state.

The charges (Q_{f2} and Q_{f1}) left behind on floating diffusions following a charge transfer are the sources of image lag and excess noise. In order to eliminate image lag and excess noise, sum of charges in the floating diffusions at the beginning of exposure phase and at the end of charge transfer phase ($t=t_2$) must remain the same. This is ensured in two ways. First, during idle state, PG is held high so that the loss of charges through subthreshold leakage is eliminated. Secondly, pulsing PG low at the end of the idle state allows the potential profiles at $t=t_4$ (end of the idle state), and at $t=t_2$ (end of the charge transfer to the sense node) to mirror each other, ensuring that the sum of charges under the floating diffusion remains constant. In order to preserve mirror symmetry of potential profiles and to increase the signal swing, the high level of TX2 and TX are made equal, and the low level of PG is made lower than the high level of TX.

Results

The performance of a 128x128 format snap-shot active pixel imager, fabricated through the standard 0.5 μm single-poly CMOS process, has been evaluated. Chip power dissipation is very low - only 3 mW at 2 Mpixels/sec. This is to be expected, since the analog signal chain is similar to other active pixel sensors [1]. Fig. 4 shows the measured optical transfer curve. The transfer curve exhibits excellent linearity, with maximum integral non-linearity (INL) over 85 % of the range being less than 0.7 %.

Even though it is photogate-type pixel, snap-shot mode of operation precludes true on-chip correlated double sampled readout. In other words, imager read noise is primarily determined by the reset noise inherent to reset of the sense node floating diffusion (FD). However, since FD is reset with the reset transistor biased in weak inversion, the read noise is significantly less than that obtained from the familiar kTC expression. Experimentally, the reset noise was found to be of the form:

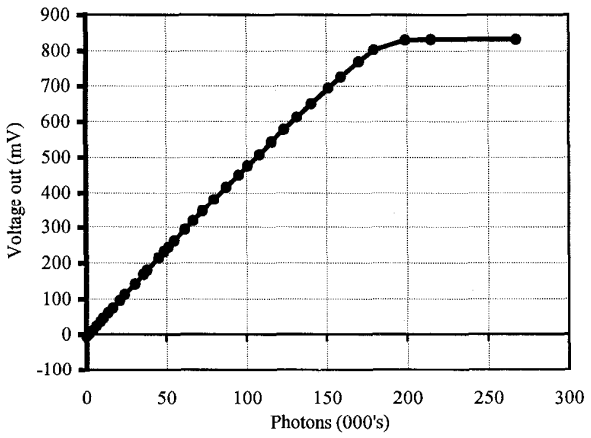

Fig. 4: Optical response transfer curve

$$\langle N_e \rangle = \frac{1}{m \cdot q}\sqrt{kTC_{FD}} \qquad (1)$$

where N_e is the input-referred read noise in electrons, C_{FD} is the floating diffusion capacitance, and m is the non-ideality factor. The measured value of the non-ideality factor is quite high - around 7.5, making the imager read noise extremely small. Measured read noise of the imager chip operated in snap-shot mode is only 4.5 electrons r.m.s.

Excess noise under low-light conditions has been observed only for large PG clock swings. If the low level of PG clock (PG-low) is more than 200 mV smaller than the TX high level (TX-high), total noise is increased by a factor of 2. The excess noise is due to formation of charge pockets under floating diffusions during transfer of charges into the sense node, and can be eliminated by appropriately setting the PG-low. No excess noise is observed when PG-low level is held close to TX-high. Furthermore, no residual image is observed when a dark frame immediately follows a bright frame. Absence of excess noise and an immeasurable image lag indicate that the floating diffusion potentials are well-behaved – there are no potential pockets or charge leakage through sub-threshold conduction.

For purposes of comparison, the imager has been operated both in snap-shot and "rolling-shutter mode". Fig. 5 shows the low-light level snap-shot image captured with the imager. No degradation in still image quality is observed in snap-shot mode compared to that in the rolling shutter mode of operation. Responsivity measurements indicate that the addition of the anti-blooming gate and optical-shield over the sense node results in an approximately 12 % reduction in quantum efficiency over conventional photogate APS pixels.

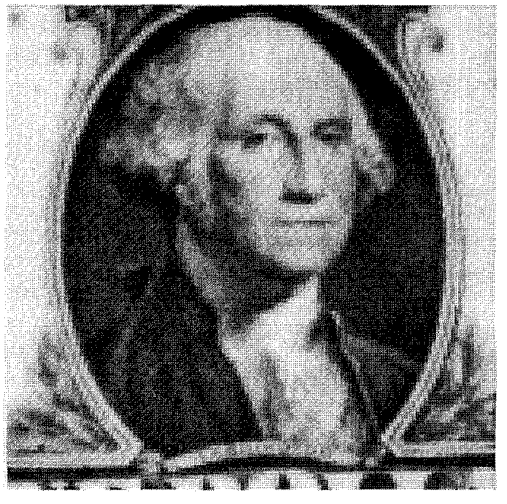

Fig. 5: Captured image of "George" from the dollar bill with the snap-shot imager operated at video rate

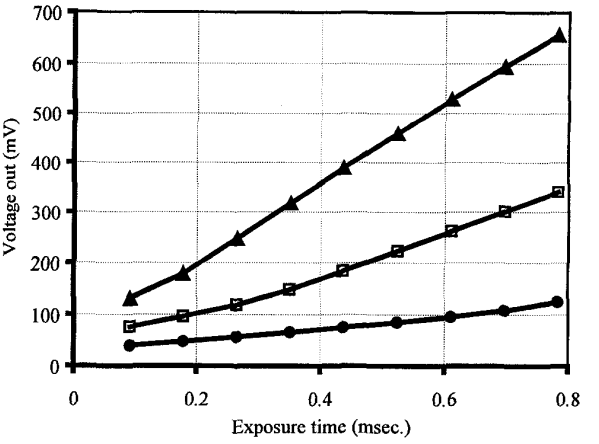

Fig. 6: Exposure control of snap-shot imager at short exposure times (each curve represents a different light intensity, larger outputs corresponding to higher light intensities)

In snap-shot mode of operation, the exposure time is independent of the frame read time. Fig. 6 shows the dependence of the imager output on the exposure time for different light intensity levels, smallest exposure time used in measurement being 75 μsec. The exposure control is linear over most of the range. However, the output exhibits an offset at small exposures, indicating light leakage into the sense node. The insufficient optical isolation results from the use of level-3 metal as the light-shield. Experimentally, the extent of light leakage is measured to be less than 5%. Vastly improved optical isolation is possible with poly-silicon and lower level metals used as light shields.

Fig. 7 shows the snap-shot mode image of a three-blade fan rotating at a high speed of 1800 r.pm. with a short exposure of 75 μsec. With such short exposures, the captured image virtually freezes the rotation of the fan, clearly showing the

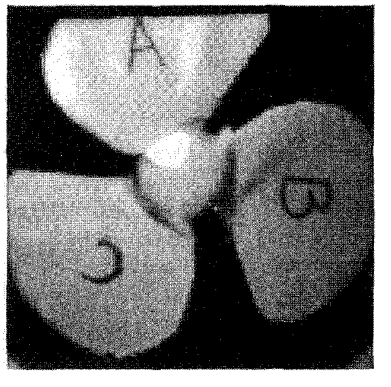

Fig. 7: Captured image of a 3-blade fan rotating at 1800 r.p.m. with simultaneous short exposure of 50 μsec.

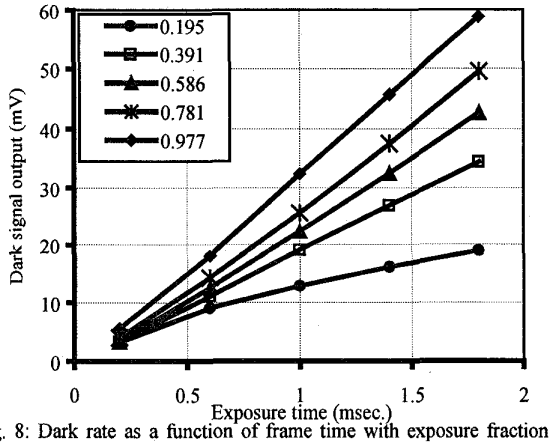

Fig. 8: Dark rate as a function of frame time with exposure fraction as a parameter (all data is collected at 23.5 deg. C)

three blades. Compared to imager operation in "rolling shutter" mode, snap-shot mode of imaging has eliminated row-wise distortion due to motion.

Experimental results indicate that the imager exhibits no blooming, even when the scene is spot-illuminated at levels 40 dB higher than saturation. Excellent anti-blooming performance results from the incorporation of the extra lateral anti-blooming gate (TX2) in the pixel.

The imager dark rate depends both on the exposure time and the frame time, since the photogate accumulates dark current only during exposure. Fig. 8 shows the dependence of the dark rate on the frame time for parametric variation of the exposure fraction (ratio of exposure to frame time) from 0.195 to 0.977. The change in the dark current slope with varying exposure fraction is due to changes in the relative dark current contributions from the sense node and the photogate, with the sense node contribution dominating only for short exposures. The data in fig. 8 indicates that the dark rate at room temperature is very low. The computed dark rate, normalized to the pixel area, is 77 pA/cm^2 for the photogate, and 28 pA/cm^2 for the sense node.

Conclusions

The paper reports successful operation of a 128x128 snap-shot photogate CMOS imager. Table 1 lists the measured imager performance values. Measurements indicate that it is capable of imaging at high shutter speeds, producing high quality images free from motion artifacts. The read noise is extremely low (4.5 e$^-$), despite the absence of true on-chip correlated double sampling. Image lag and excess noise associated with the incorporation of a blooming control gate in a single poly-silicon CMOS technology has been eliminated through the use of a new pixel timing and clock biases, as well as through layout optimization,. Test results

Table 1. Summary of snapshot imager performance characteristics

Characteristics	Values
Array format	128x128
Technology	0.5 μm CMOS, 1-poly, 3-metal
Pixel size	14.4-μm x 14.4-μm
Pixel type	Photogate
Pixel complexity	6 transistors per pixel
Power	< 3 mW @ 1 Mpix./sec
Max. frame rate	400 frames/sec.
Min. Exposure Time	75 μsec (measured)
Conversion Gain	25 μV/e$^-$
Linearity	99.3 % over 90% range
Fixed Pattern Noise	0.1% after DDS correction
Read Noise	4.5 electrons
Full Well	37,000 electrons
Dynamic range	78.3 dB
Peak QE	19%
Dark Rate	30 – 77 pA/cm^2 @ R.T.
Image lag	Immeasurable
Blooming	None observed at 40 dB above sat.

verify that a snap-shot imager, implemented in a single poly-silicon CMOS technology, reproduces high quality, motion-artifact-free images at high shutter-speeds, without compromising other imaging performance that are achieved with state-of-the-art CMOS imagers.

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