Yoshiaki Hagiwara @SONY invented the Pinned Photo Diode in 1975.

For the original document, visit and search the Japanese Official Patent Web :

https://www4.jplatpat.inpit.go.jp/eng/tokujitsu/tkbs_en/TKBS_EN_GM101_Top.action

Document No.（1975-134985） on the P+NPNsub junction type PPD and

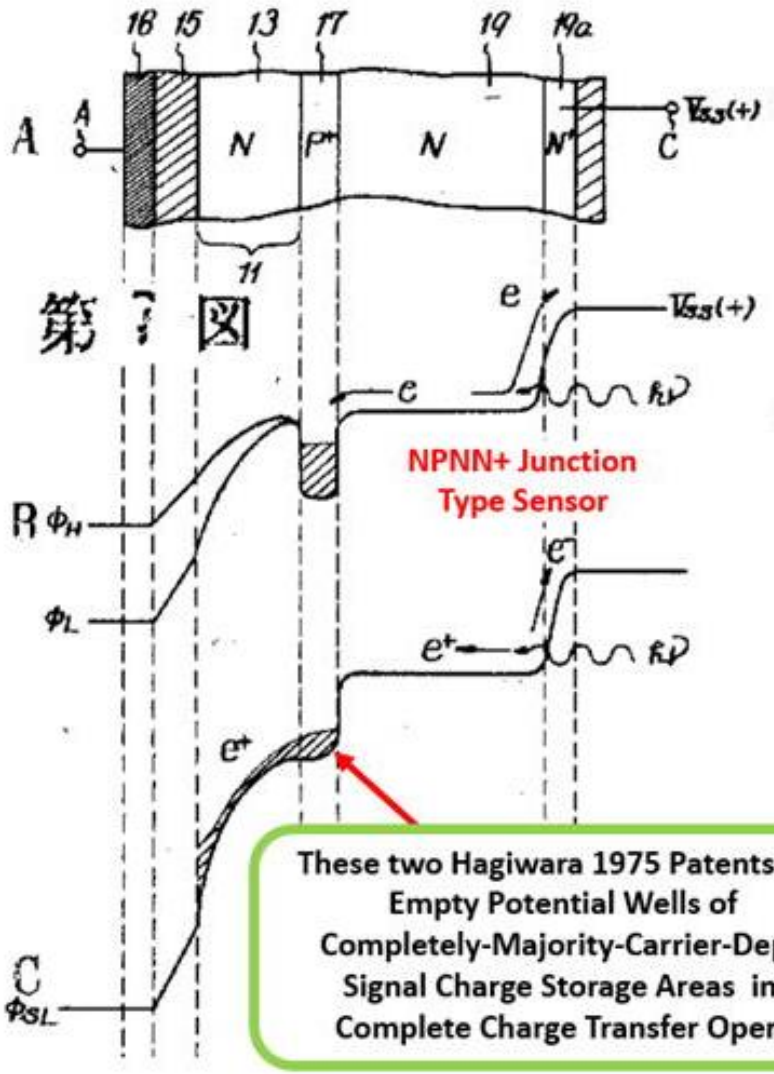
Document No.（1975-127647）on the NPNN+ junction type PPD、

Both filed by Yoshiaki Hagiwara in 1975 at Sony.

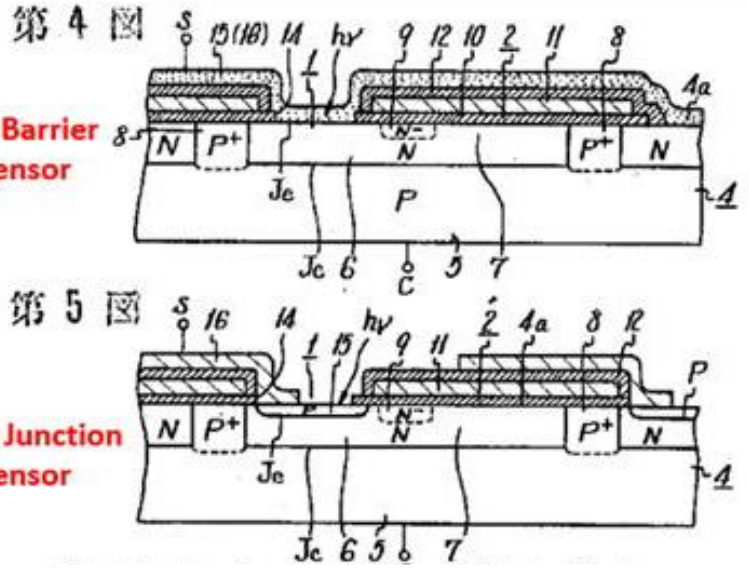
SONY original HAD and Pinned Photo Diode are the same thing.

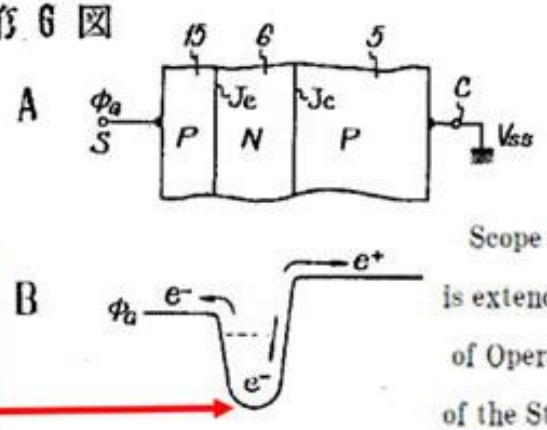
Both were invented and defined in these two Japanese Patents by Hagiwara at SONY in 1975.

NPNN+ Junction type Pinned Photo Diode
See Japanese Patent (1975- 127647)



P+N-Psub Junction type Pinned Photo Diode
See Japanese Patent (1975-134985)





These two Hagiwara 1975 Patents showed Empty Potential Wells of Completely-Majority-Carrier-Depleted Signal Charge Storage Areas implying Complete Charge Transfer Operations.

Scope of Patent Right is extended over all kinds of Operations and Usage of the Structure defined in the Patent Claims.

A Pinned Photo Diode of the NPNN+ junction type

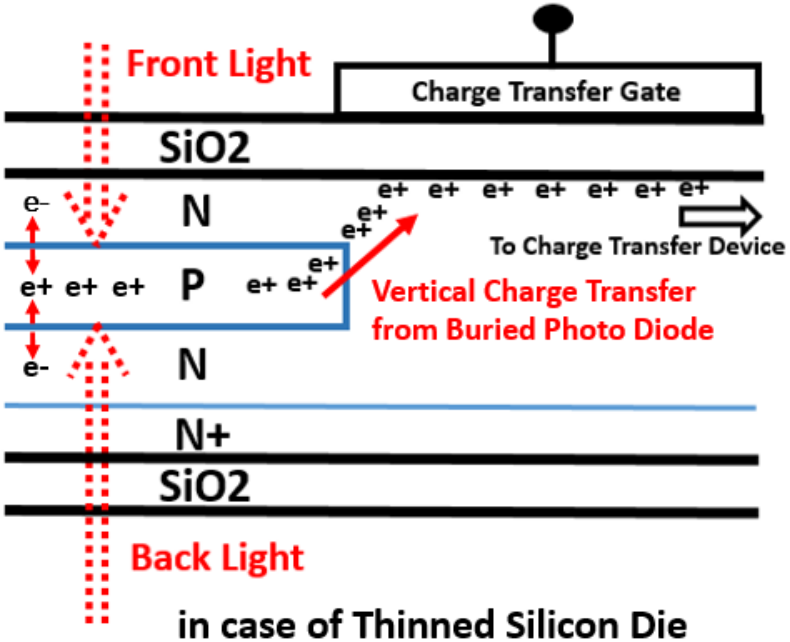
with vertical charge transfer function.

See Japanese Patent Document Number (1975-127647)

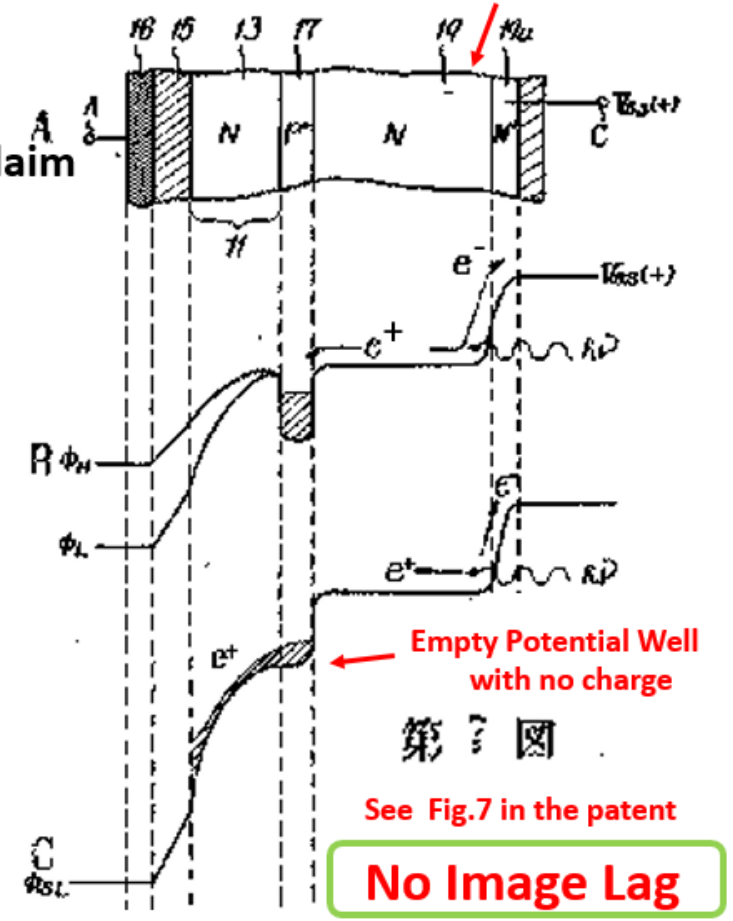
File	1975-127647	Filed	1975/10/23
Public	1975-051816	Public	1977/04/26

A Pinned Photo Diode defined in the Patent Claim

The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.



in case of Thinned Silicon Die



No Image Lag

SONY HAD and PPD are the same thing !

PPD in Complete Charge Transfer Mode

A Pinned Photo Diode of the P+N-PNsub junction (thyristor) type

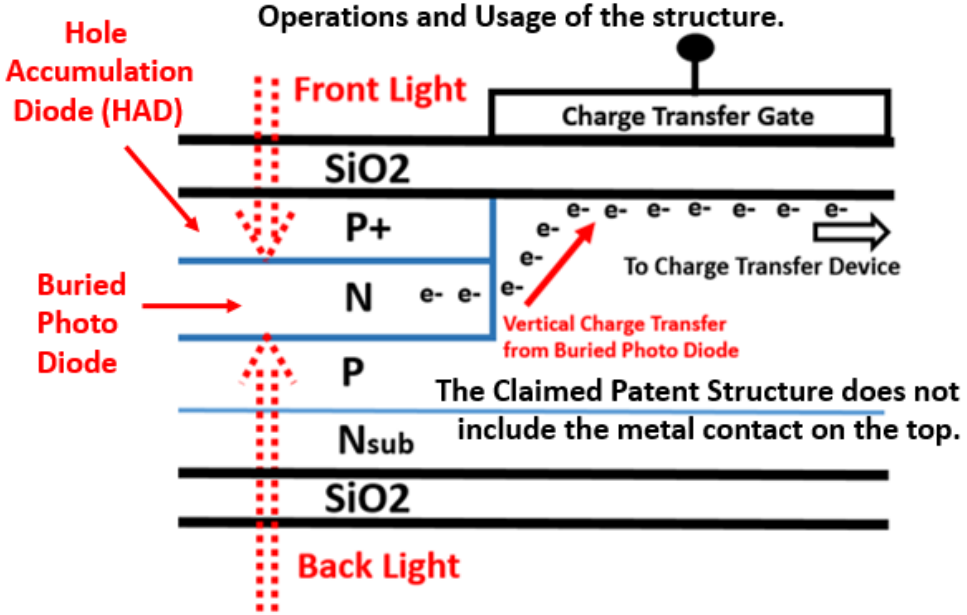
with vertical overflow drain function invented by Hagiwara 1975

See Japanese Patent Document Number (1975-134985)

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

A Pinned Photo Diode defined in the Patent Claims

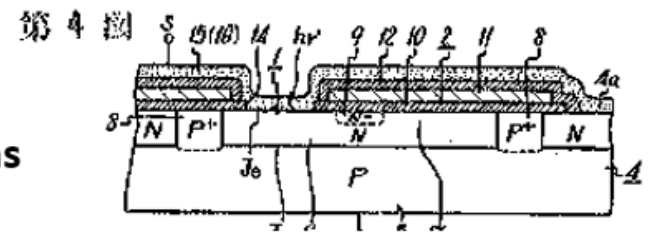
The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.



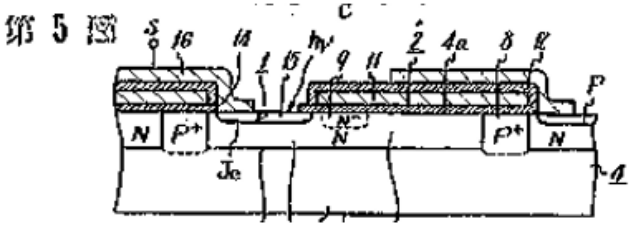
The Claimed Patent Structure does not include the metal contact on the top.

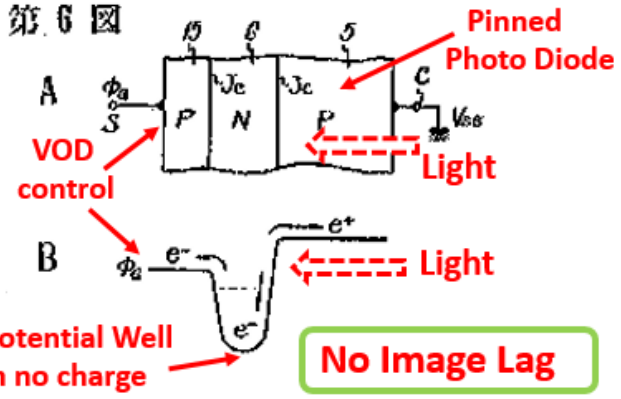
in case of Thinned Silicon Die

One Schottky Barrier Image Sensor Application



One Pinned Photo Diode Image Sensor Application





No Image Lag

SONY HAD and PPD are the same thing !

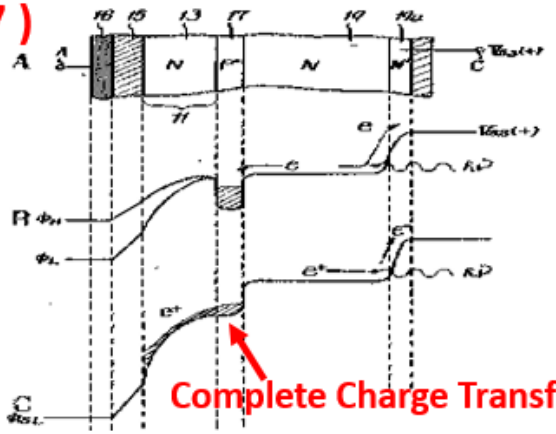
PPD in Complete Charge Transfer Mode

A Pinned Photo Diode of the N+NPNN+ junction type

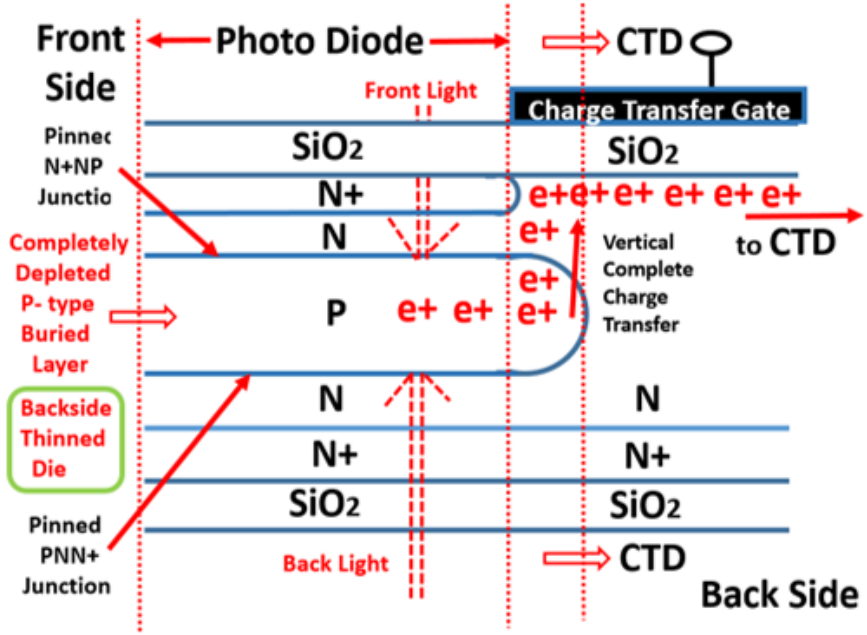
See Japanese Patent Document Number (1975-127647)

with Vertical Complete Charge Transfer Function.

File	1975-127647	Filed	1975/10/23
Public	1975-051816	Public	1977/04/26



A Pinned Photo Diode defined in the Patent Claim



特許請求範囲

(1)半導体基体の一方の主面側に、
(2)絶縁膜を介して電荷転送用電極が被着配列される
(3)1の導電型の転送領域が形成され、
(4)之より上記半導体基体の他方の主面側に
(5)上記転送領域に接する他の導電型の領域と
(6)該領域に接する1の導電型の領域とより成る
(7)受光領域が形成され、
(8)上記転送用電極に所要の電圧を印加することにより、
(9)上記受光領域に蓄積した電荷を
(10)上記転送領域に転送し、上記電荷転送用電極に
(11) 上記所要の電圧とは異るクロック電圧を印加して
(12)上記基体の上記一方の主面に沿って
(13)電荷の転送を行うようにしたことを
(14)特徴とする固体撮像装置。

Patent Claims defined in Japanese

The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

SONY HAD and PPD are the same thing !

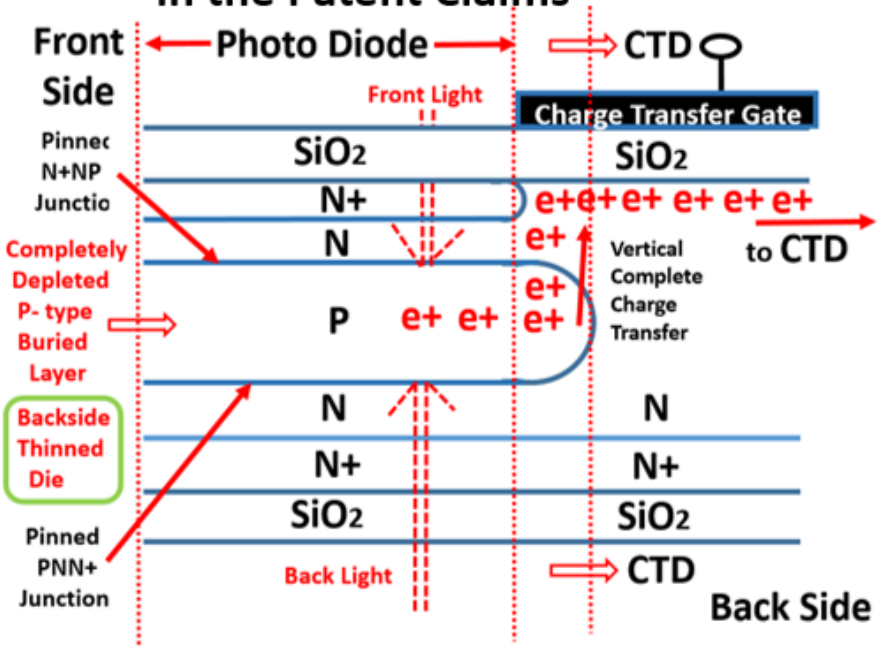
PPD in Complete Charge Transfer Mode

A Pinned Photo Diode of the N+NPNN+ junction type

See Japanese Patent (1975-127647)
with Vertical Complete Charge Transfer Function.

File	1975-127647	Filed	1975/10/23
Public	1975-051816	Public	1977/04/26

A Pinned Photo Diode defined in the Patent Claims



The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

SONY HAD and PPD are the same thing !

Patent Claims

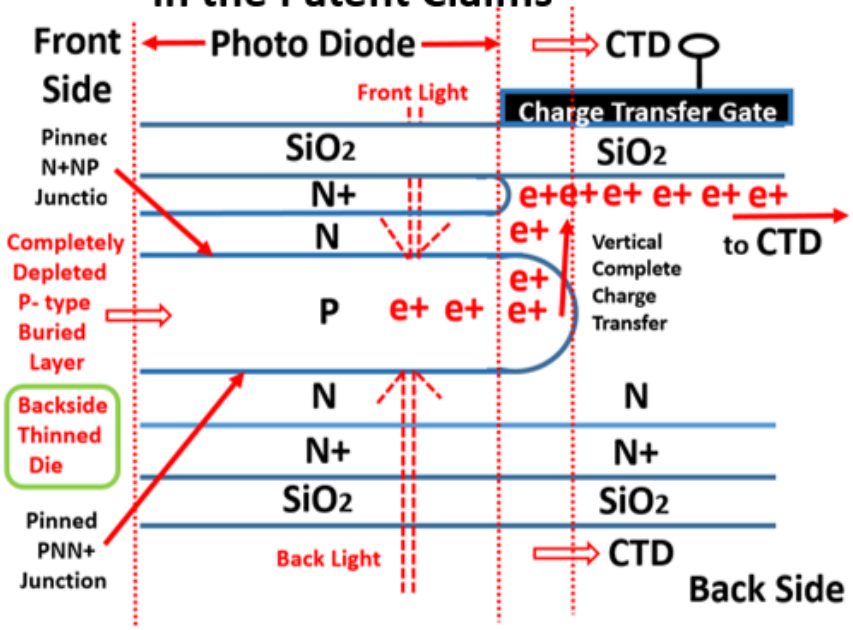
(1)On the front side surface of the semiconductor substrate die, (which can be either Nsub, Psub or an intrinsic one. But here Nsub is chosen as a simple example.
(2)the charge transfer gate (CTG) is formed with the oxide insulator (SiO2) layer in between.
(3)The first region N of the first doping type is formed to transfer signal charges under the CTG. (The first region can be an N-well in a Psub case, but in this simple example, the Nsub is chosen so that the first region N can be the Nsub itself.)
(4)Besides that, along the backside surface of the semiconductor substrate Nsub,
(5) another region P of doping type is formed in the substrate die, which is placed adjacent to the charge transfer region under the CTG.
(6)This second region P in the substrate die makes an NPNsub junction structure,
(7) which forms the photo sensing diode and photo signal charge carrier storage region, (which is an NPNsubN+ type Pinned Photo Diode in the final device fabrication stage).

A Pinned Photo Diode of the N+NPNN+ junction type

See Japanese Patent (1975-127647)
with Vertical Complete Charge Transfer Function.

File	1975-127647	Filed	1975/10/23
Public	1975-051816	Public	1977/04/26

A Pinned Photo Diode defined in the Patent Claims



The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

SONY HAD and PPD are the same thing !

Patent Claims

(8) By applying a proper voltage of one-shot pulse to the CTG electrode,
(9) the photo signal charge carriers stored in the photo storage region, (that is, in the NPN type Pinned Photo Diode),
(10) are transferred to the adjacent charge storage region under the oxide layer of the CTG.
(11) Then, by applying on the CTG electrode different clock voltage, which is not the one-shot pulse applied before, the signal charge carriers under the CTG are transferred further along to the nearby charge transfer device (CTD) which can be either a CCD type or a CMOS type charge transfer device (CTD).
(12) Along the front side surface of the semiconductor substrate (Nsub) ,
(13) the signal charge carriers are to be transferred in a proper manner.
(14) The combined solid state image sensor structure, with these features, including all its usage and operations of the Photo Diode and Charge Transfer Device defined above is in the scope of the patent claims defined above.

A Pinned Photo Diode of the P+N-PNsub junction (thyristor) type

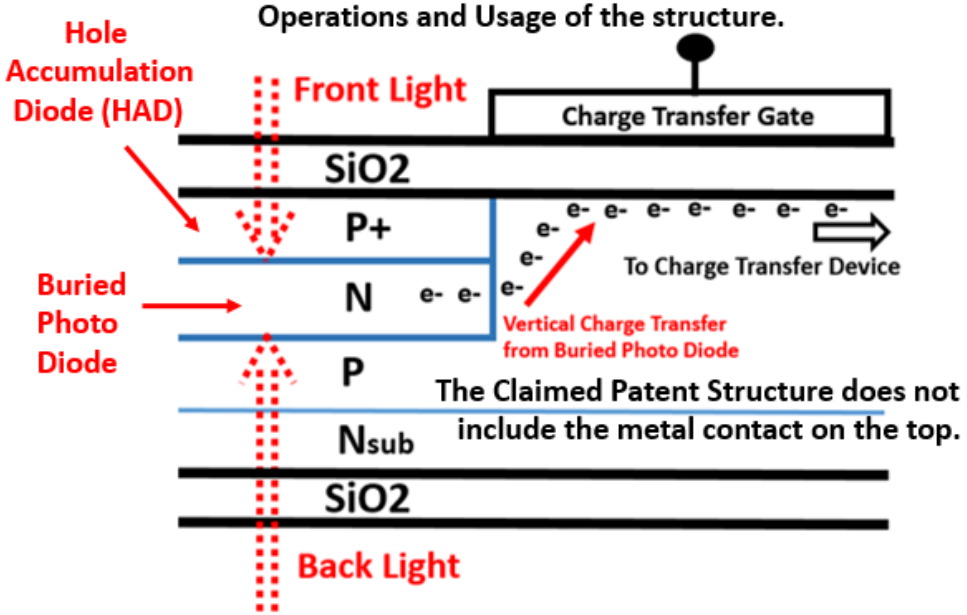
with vertical overflow drain function invented by Hagiwara 1975

See Japanese Patent Document Number (1975-134985)

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

A Pinned Photo Diode defined in the Patent Claims

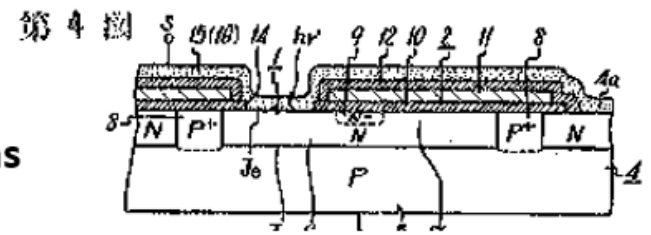
The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.



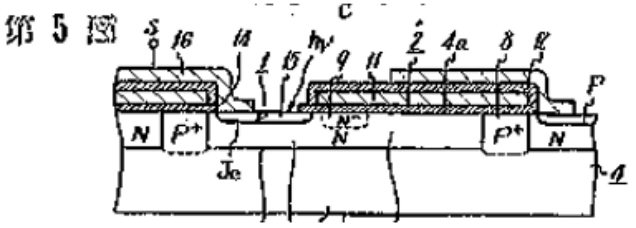
The Claimed Patent Structure does not include the metal contact on the top.

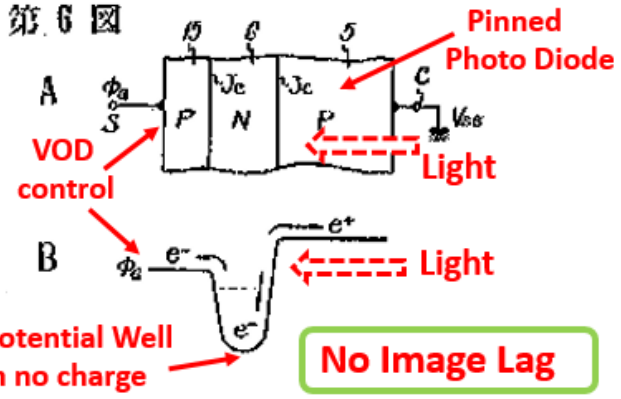
in case of Thinned Silicon Die

One Schottky Barrier Image Sensor Application



One Pinned Photo Diode Image Sensor Application





No Image Lag

SONY HAD and PPD are the same thing !

PPD in Complete Charge Transfer Mode

A Pinned Photo Diode of the P+N-PNsubN+ junction (thyristor) type

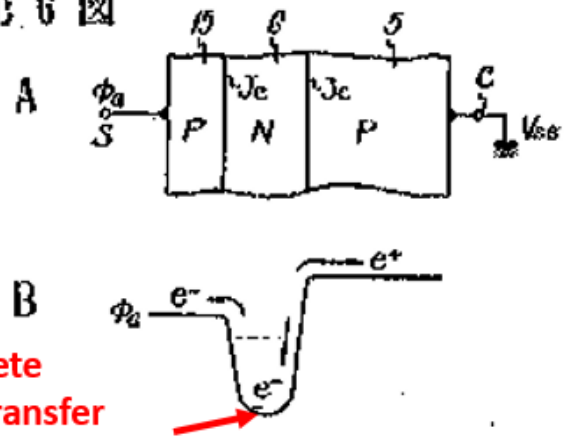
with vertical overflow drain function

invented by Hagiwara 1975

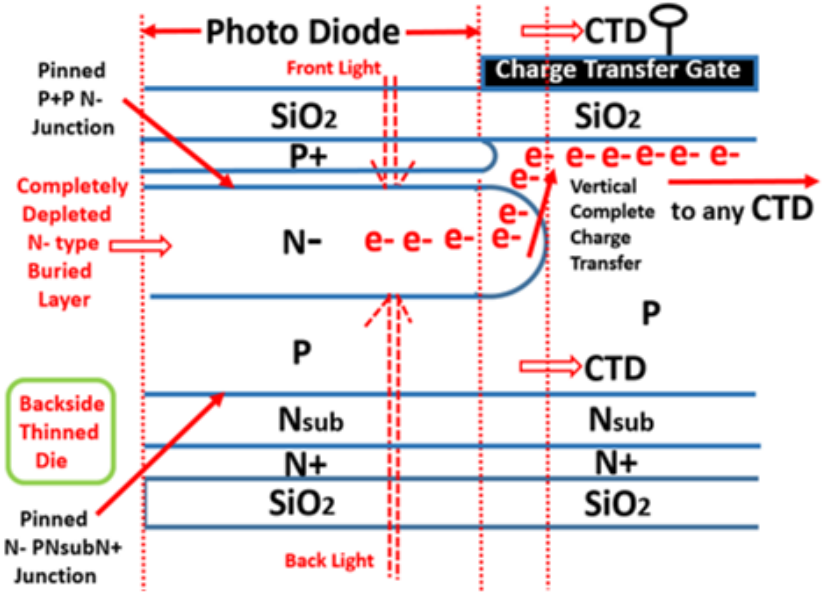
See Japanese Patent Document Number (1975-134985)

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

第 6 図



A Pinned Photo Diode defined in the Patent Claims



Complete Charge Transfer

Empty Potential Well with completely majority-carrier depleted base signal charge storage area.

The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

SONY HAD and PPD are the same thing !

特許請求範囲

(1)半導体基体に、
(2)第1の導電型の第1半導体領域と、
(3)その上に形成された第2導電型の第2半導体領域
(4)とが形成されて光感知部と
(5)その上の電荷を転送する電荷転送部とが
(6)上記半導体基体の主面に沿う如く配置されて成る
(7)固体撮像装置に於いて、
(8)上記光感知部の上記第2半導体領域に
(9)整流性接合が形成され、
(10)該接合をエミッタ接合とし、
(11)上記第1及び第2半導体領域間の接合を
(12)コレクタ接合とするトランジスタを形成し、
(13) 該トランジスタのベースとなる上記第2半導体領域に
(14) 光学像に応じた電荷を蓄積し、
(15)ここに蓄積された電荷を上記転送部に移行させて、
(16)その転送を行うようにしたことを
(17)特徴とする固体撮像装置。

Patent Claims defined in Japanese

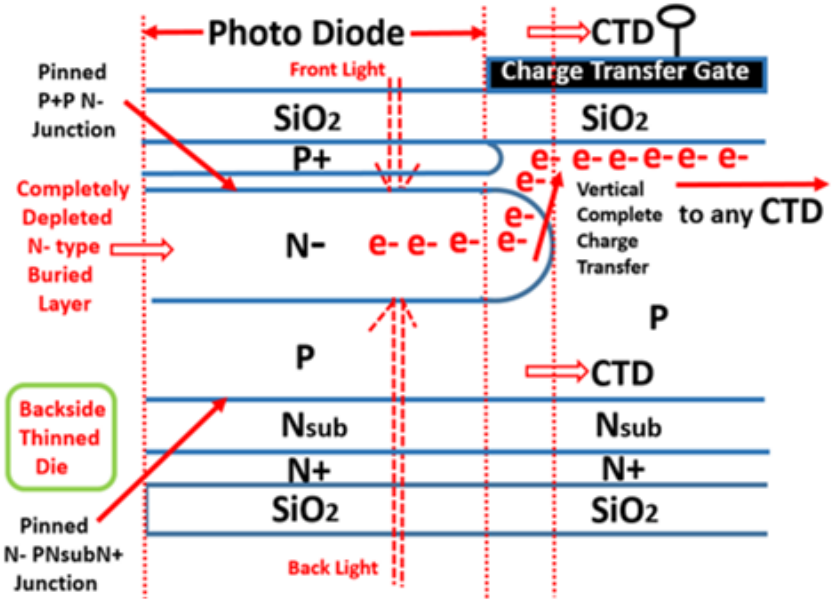
A Pinned Photo Diode of the P+N-PNsubN+ junction (thyristor) type

with vertical overflow drain function invented by Hagiwara 1975

See Japanese Patent Document Number (1975-134985)

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

A Pinned Photo Diode defined in the Patent Claims



The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

SONY HAD and PPD are the same thing !

Patent Claims

(1) In a semiconductor substrate die (Nsub),

(2) the first type semiconductor region P is formed. A region P can be a P-well.

(3) And the second region N of the second type is formed on the first region P .

(4) The N and P regions together form a photo sensing structure of an NP junction.

(5) A charge transfer structure (CTD), receiving the photo charge from the NP junction,

(6) is formed along the front surface of the semiconductor substrate die (Nsub).

(7) In so-defined solid state image sensor,

(8) on the second region N of the photo sensing element structure NP,

(9) another rectifying junction P+N is formed.

(10) This junction P+N can be called as an emitter junction of the P+NP junction.

A Pinned Photo Diode of the P+N-PNsubN+ junction (thyristor) type

with vertical overflow drain function invented by Hagiwara 1975

See Japanese Patent Document Number (1975-134985)

File	1975-134985	Filed	1975/11/10
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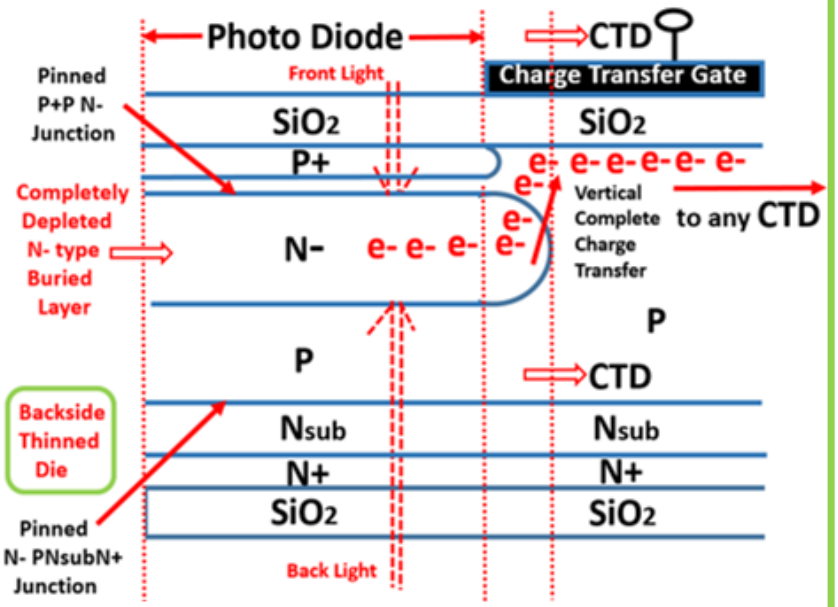
A Pinned Photo Diode defined in the Patent Claims



The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

SONY HAD and PPD are the same thing !

Patent Claims

(11) And the junction composed of the first region P and the second region N

(12) can be called as a collector junction of the P+NP junction type transistor structure.

(13) The second region N, which can be now called as the base region of the P+NP junction type photo transistor structure,

(14) is the photo-charge storage area of the majority carriers, generated according to the illuminated optical image information.

(15) After transferring the photo signal charge stored here in the N base region to the adjacent charge transfer structure (CTD),

(16) the adjacent charge transfer structure (CTD) further performs the subsequent proper charge transfer operations to the final chip outlet.

(17) The combined solid state image sensor structure, with these features, including all its usage and operations of the Photo Diode and Charge Transfer Device defined above is in the scope of the patent claims defined above.

Yoshiaki Hagiwara at Sony invented Pinned Photo Diode in 1975.

In the semiconductor base substrate(Nsub), placing the first type layer(P) and the second type(N) on the first type(P) forming a photo sensor(NP), the (NP) photo sensor and the CTD part are places along the substrate (Nsub) surface. Form an Emitter junction(P+N) on the second type layer(N) forming a P+NP junction transistor. Light beam is exposed into the second layer(N), which corresponds to the base (N) of the P+NP transistor structure.

For the original document, visit and search the Japanese Official Patent Web :
https://www4.jplatpat.inpit.go.jp/eng/tokujitsu/tkbs_en/TKBS_EN_GM101_Top.action
Document No.（1975-134985） on the P+NPNsub junction type PPD and
Document No.（1975-127647）on the NPNN+ junction type PPD、

（1）半導体基体(Nsub)に、

(1) In the semiconductor base substrate (N sub),

Yoshiaki Hagiwara at Sony invented Pinned Photo Diode in 1975.

In the semiconductor base substrate(Nsub), placing the first type layer(P) and the second type(N) on the first type(P) forming a photo sensor(NP), the (NP) photo sensor and the CTD part are places along the substrate (Nsub) surface. Form an Emitter junction(P+N) on the second type layer(N) forming a P+NP junction transistor. Light beam is exposed into the second layer(N), which corresponds to the base (N) of the P+NP transistor structure.

(2)第1導電型(P)の
第1半導体領域(P)と、

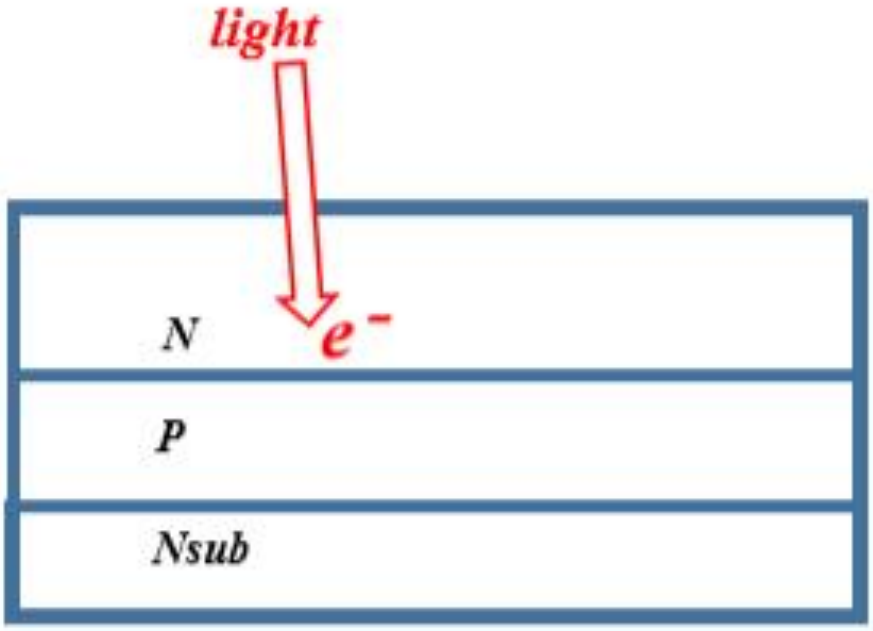
(2) placing the first type layer(P) and

Yoshiaki Hagiwara at Sony invented Pinned Photo Diode in 1975.

In the semiconductor base substrate(Nsub), placing the first type layer(P) and the second type(N) on the first type(P) forming a photo sensor(NP), the (NP) photo sensor and the CTD part are places along the substrate (Nsub) surface. Form an Emitter junction(P+N) on the second type layer(N) forming a P+NP junction transistor. Light beam is exposed into the second layer(N), which corresponds to the base (N) of the P+NP transistor structure.

(3)之の上に形成された第2導電型(N)の
第2半導体電領域(N)とが形成されて、

(3) and the second type layer (N)
on the first type layer (P),
forming a photo sensor (NP),

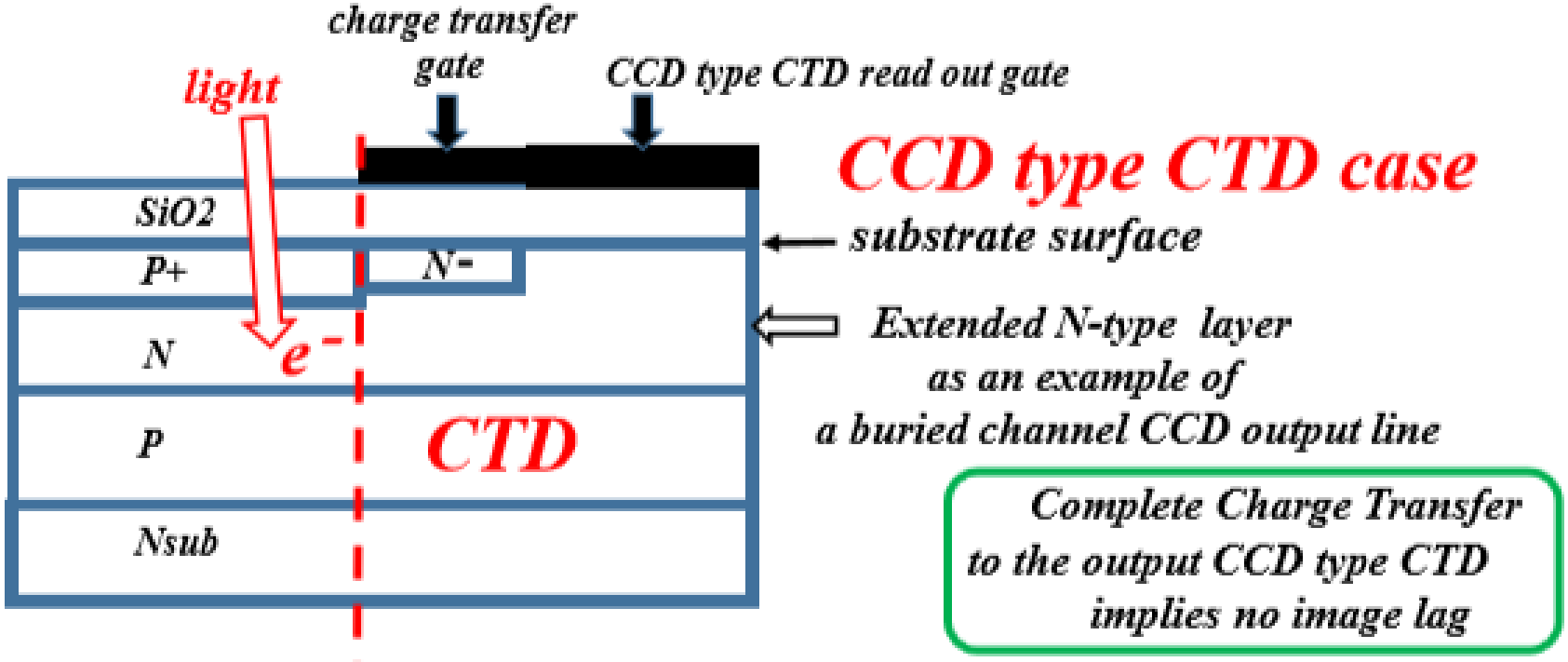


Yoshiaki Hagiwara at Sony invented Pinned Photo Diode in 1975.

In the semiconductor base substrate(Nsub), placing the first type layer(P) and the second type(N) on the first type(P) forming a photo sensor(NP), the (NP) photo sensor and the CTD part are places along the substrate (Nsub) surface. Form an Emitter junction(P+N) on the second type layer(N) forming a P+NP junction transistor. Light beam is exposed into the second layer(N), which corresponds to the base (N) of the P+NP transistor structure.

(4)光感知部(NP)と、之(NP)よりの電荷を
転送する電荷転送部(CTD)とが、
半導体基体(Nsub)の主面(Main Surface)
に沿う如く配置されてなる固体半導体装置に於いて、

(4) The (NP) photo sensor and the CTD part are placed along the substrate (Nsub) surface.



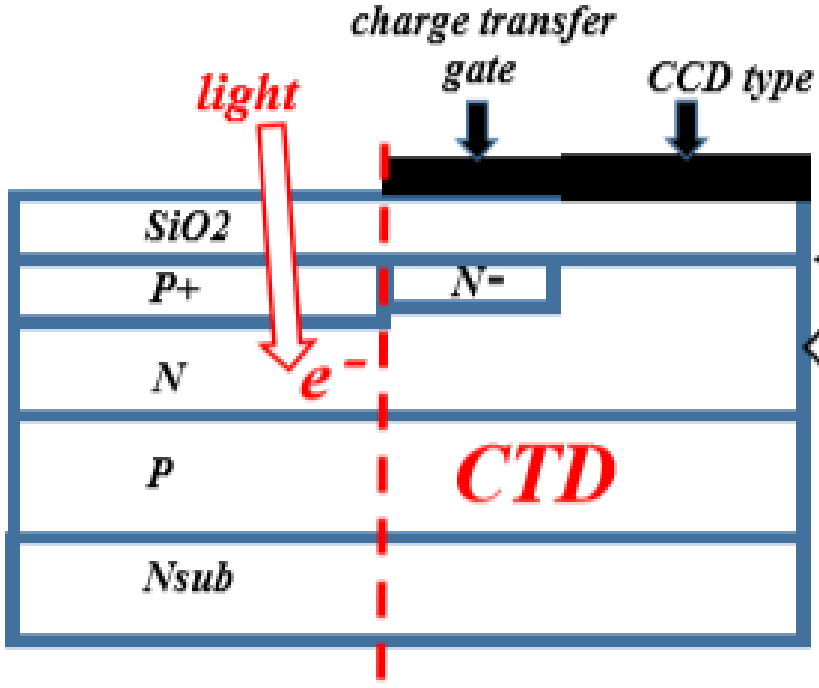
Complete Charge Transfer
to the output CCD type CTD
implies no image lag

Yoshiaki Hagiwara at Sony invented Pinned Photo Diode in 1975.

In the semiconductor base substrate(Nsub), placing the first type layer(P) and the second type(N) on the first type(P) forming a photo sensor(NP), the (NP) photo sensor and the CTD part are places along the substrate (Nsub) surface. Form an Emitter junction(P+N) on the second type layer(N) forming a P+NP junction transistor. Light beam is exposed into the second layer(N), which corresponds to the base (N) of the P+NP transistor structure.

(5)上記光感知部(N-P photo sensor)の
上記第2半導体電領域(N)に
整流性接合(P+N)が形成され、
該接合(P+N接合)をエミッタ接合(P+N)とする
トランジスタ(P+NP)を形成し、

form an Emitter junction (P+N)
on the second type layer(N),
forming a P+NP junction transistor



CCD type CTD case

substrate surface

Extended N-type layer
as an example of
a buried channel CCD output line

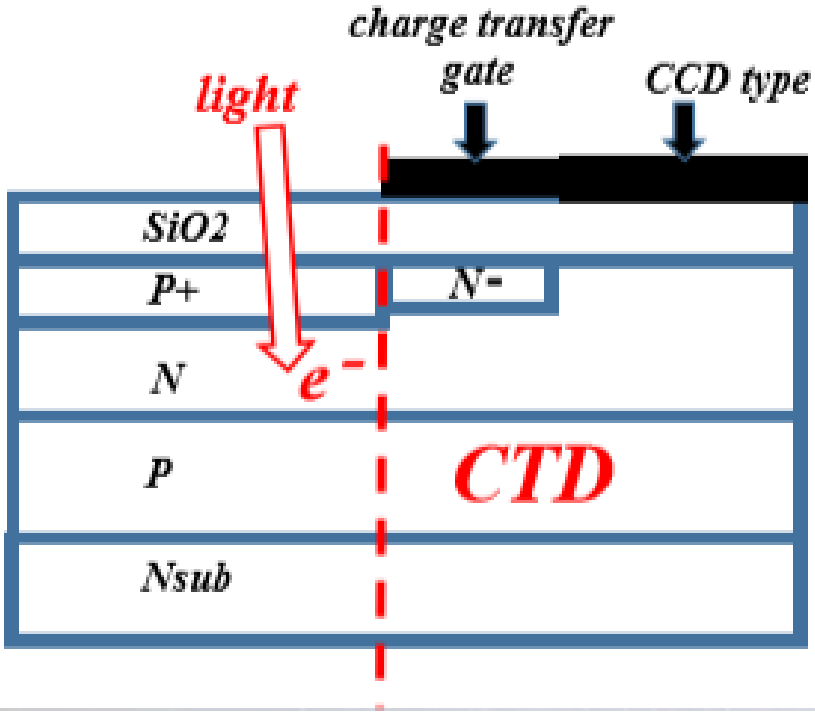
Complete Charge Transfer
to the output CCD type CTD
implies no image lag

Yoshiaki Hagiwara at Sony invented Pinned Photo Diode in 1975.

In the semiconductor base substrate(Nsub), placing the first type layer(P) and the second type(N) on the first type(P) forming a photo sensor(NP), the (NP) photo sensor and the CTD part are places along the substrate (Nsub) surface.
Form an Emitter junction(P+N) on the second type layer(N) forming a P+NP junction transistor.
Light beam is exposed into the second layer(N), which corresponds to the base (N) of the P+NP transistor structure.

(6)該トランジスタ(P+NP)のベース(N)となる
上記第2半導体電領域　に光学象に
応じた電荷(光電変換された電子)を蓄積し、

Light beam is exposed into the second layer(N), which corresponds to the base (N) of the P+NP transistor structure.



CCD type CTD case

substrate surface

Extended N-type layer
as an example of
a buried channel CCD output line

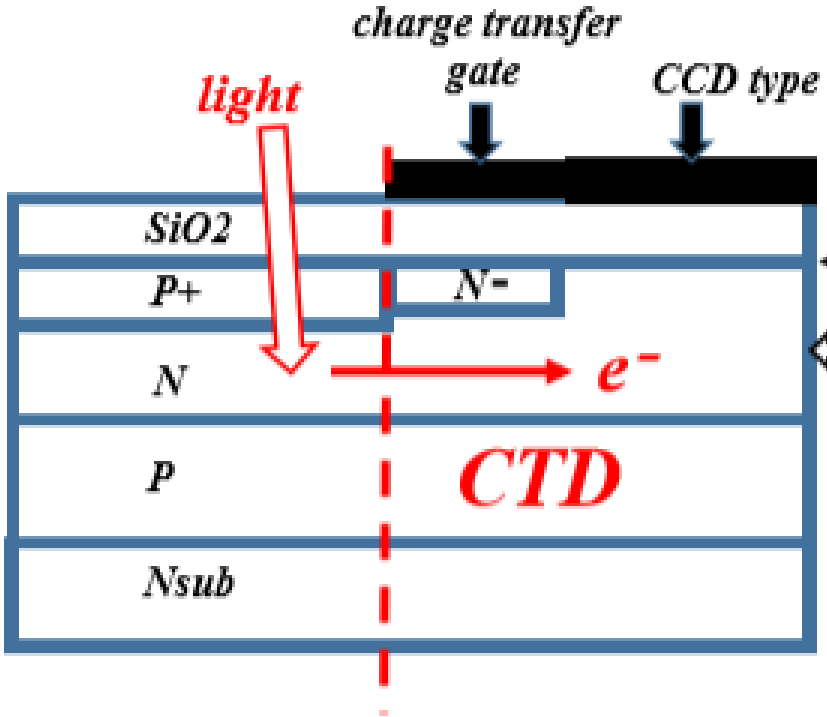
Complete Charge Transfer to the output CCD type CTD implies no image lag

Yoshiaki Hagiwara at Sony invented Pinned Photo Diode in 1975.

In the semiconductor base substrate(Nsub), placing the first type layer(P) and the second type(N) on the first type(P) forming a photo sensor(NP), the (NP) photo sensor and the CTD part are places along the substrate (Nsub) surface. Form an Emitter junction(P+N) on the second type layer(N) forming a P+NP junction transistor. Light beam is exposed into the second layer(N), which corresponds to the base (N) of the P+NP transistor structure.

(7) ここ に蓄積された電荷を
上記転送部(CTD)に移行させて、
その転送を行うようにしたことを
特徴とする固体撮像装置

(7) And the photo electrons are transferred from the base(N) to the CTD as placed next to the base(N) layer.



CCD type CTD case

substrate surface

Extended N-type layer as an example of a buried channel CCD output line

Complete Charge Transfer to the output CCD type CTD implies no image lag

Digital CMOS image sensor consisting of three basic blocks.

Block (1) Retina Nerve Cells (Hagiwara 1975 Retina Photo Diode)

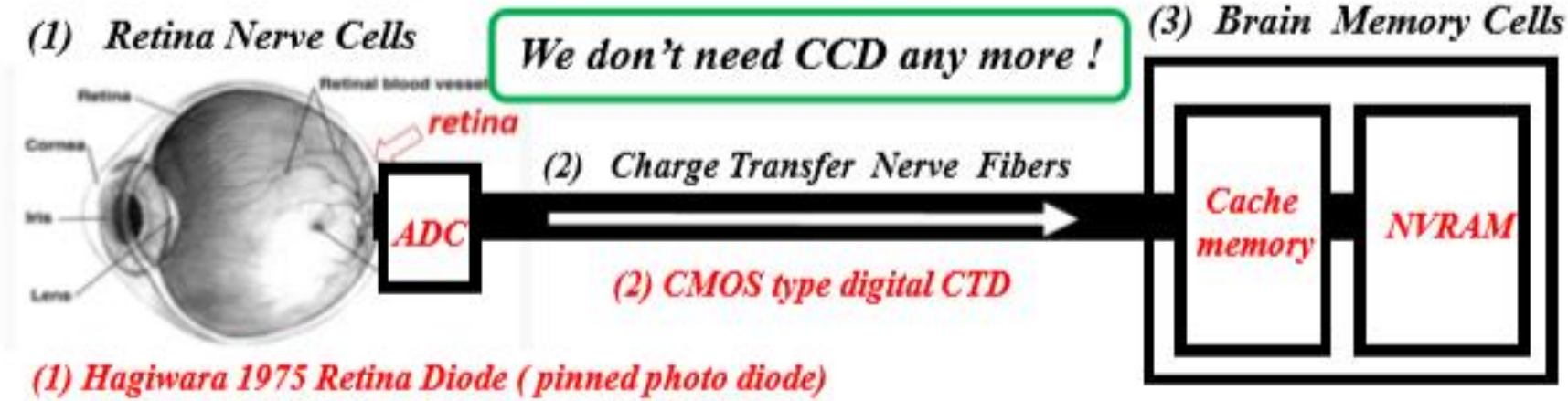
Block (2) Charge Transfer Nerve Fibers (CMOS type digital CTD)

Block (3) Brain Memory Cells (Fast Cache SRAM and Slow NVRAM)

Digital CMOS image sensor

with highly sensitive and no image lag Hagiwara Diode (pinned photo diode)

We need also an AD convertor absolutely !!!

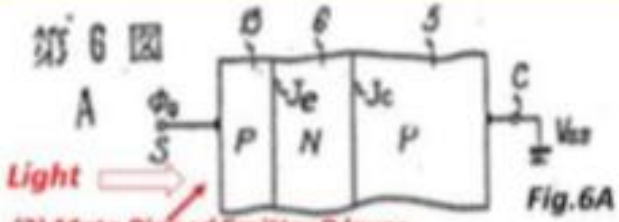


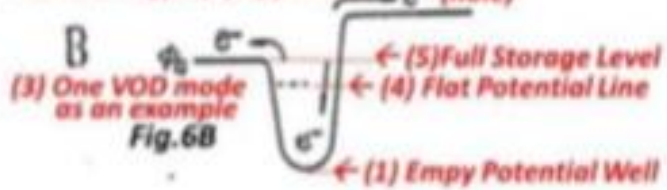
But we still need Hagiwara Diode to achieve high sensitivity and no image lag.

Yoshiaki (Daimon) Hagiwara

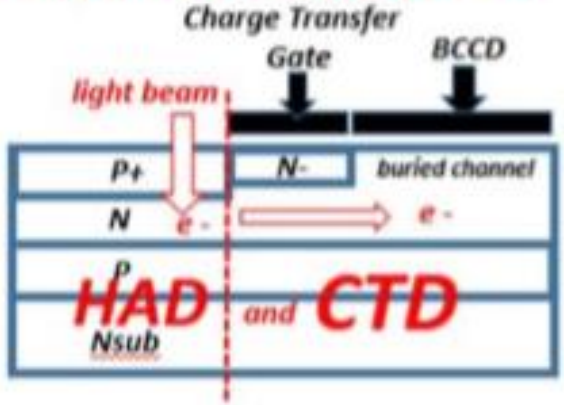
Hagiwara 1975 Retina Diode (pinned photo diode)

Hagiwara diode, defined in Japanese Patent App 50 - 134985, 1975 and pinned photo diode are the same thing with the same structure.





Hagiwara 1975 patent defines
Hagiwara Diode(HAD) + CTD



Hagiwara diode invented by Hagiwara at Sony in his 1975 patent has the following five important features. They are (1) low CkT noise (2) low trap noise (3) low image lag and (4) good light sensitivity which are the same features of pinned photo diode, and more over (5) built-in VOD . The important features of (3) and (5) are shown by the empty potential well in his patent Fig.6B.

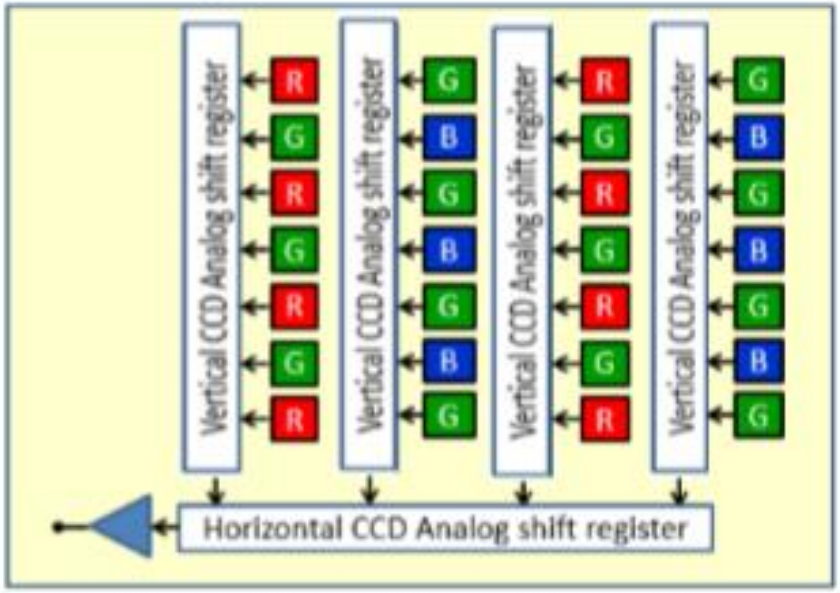
Hagiwara invented the pinned photo diode in 1975.

Block (2) Charge Transfer Nerve Fibers （信号電荷転送用神経線）

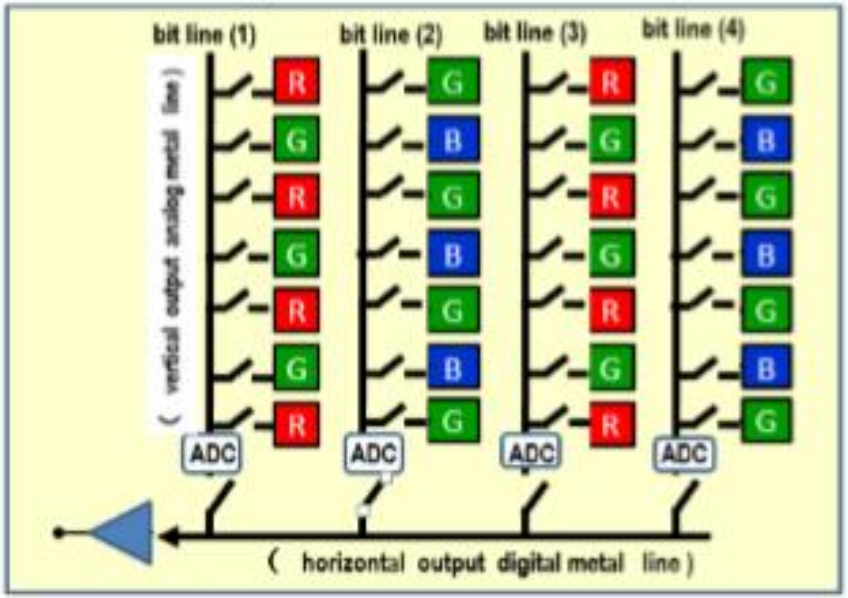
Historically, CTD includes MOS type , BBD, CCD and CMOS type charge transfer devices.

CTD (charge transfer device) ; BBD(Bucket Brigate Device) ; CCD (charge coupled device) ;

CCD type CTD in 1970～2010



CMOS type CTD in 2010 ~ present



We don't need CCD any more !

Hagiwara invented the pinned photo diode in 1975.

Yoshiaki (Daimon) Hagiwara

Block (2) Charge Transfer Nerve Fibers （信号電荷転送用神経線）

IEDM1998 paper (pp.2.7.1-2.7.4)

A Snap-Shot CMOS Active Pixel Imager for Low-Noise, High-Speed Imaging

Guang Yang, Orly Yadid-Pecht, Chris Wrigley, and Bedabrata Pain

Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109, USA

Abstract

Design and performance of a 128x128 snap-shot imager implemented in a standard single-poly CMOS technology is presented. A new pixel design and clocking scheme allow the imager to provide high-quality images without motion artifacts at high shutter speeds (< 75 μsec. exposure), with low noise (< 5 e⁻), immeasurable image lag, and excellent blooming protection.

Introduction

Recent advances in CMOS imager technology have enabled the development of highly integrated, ultra-low power, camera-on-a-chip with impressive imaging performance [1, 2]. However, most CMOS imagers do not support simultaneous integration of all pixels in the imager, the imager being read out in a "rolling shutter" mode. Non-simultaneous exposure leads to image distortion whenever there is relative motion between the imager and the scene.

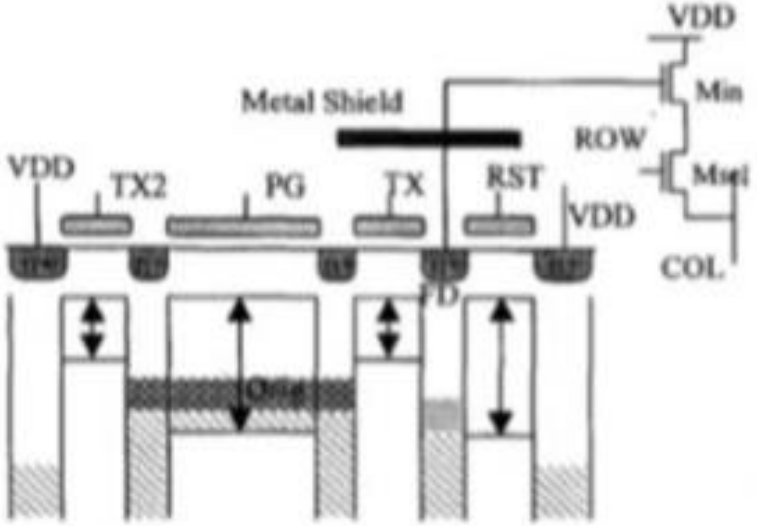


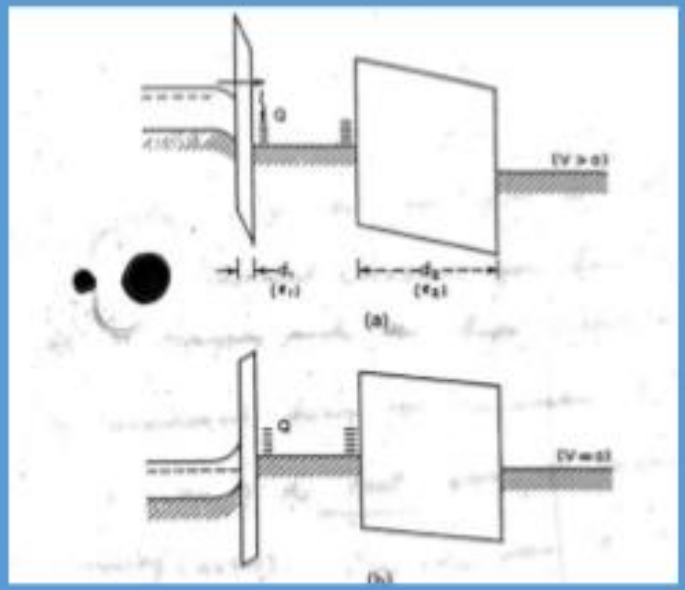
Fig. 1: Schematic of the snap-shot APS pixel. Hatched areas represent electrons

Important Contribution to the Modern Digital CMOS Image Sensor Technology

Yoshiaki (Daimon) Hagiwara

Block (3) the brain nervous cells that store the image information.

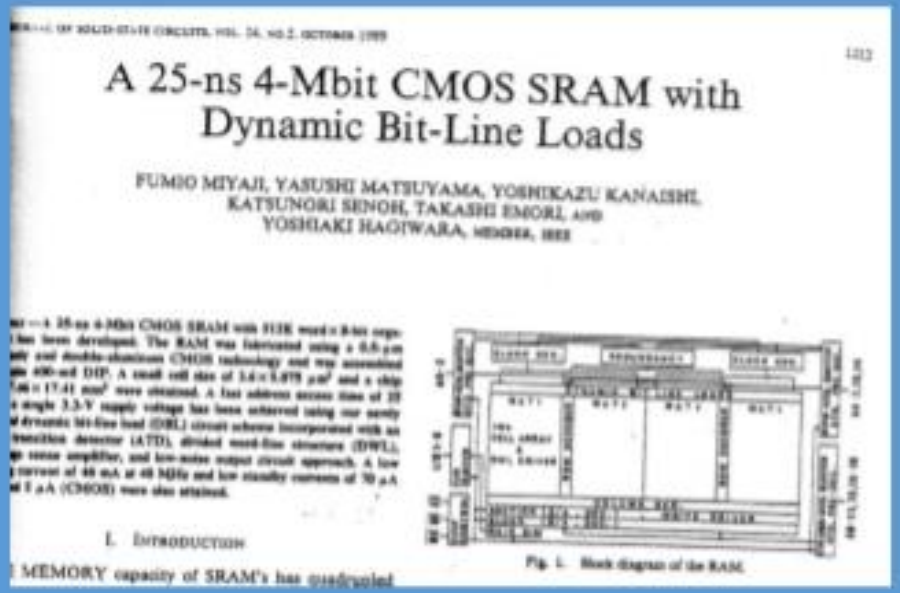
NVRAM by Prof. S.M.Sze and Cache SRAM by Sony Hagiwara are original important digital media for handy digital cameras.



A Floating Gate and Its Application to Memory Devices *

By D. KAHNG and S. M. SZE

Bell System Tech. J. 46, 1288 (1967).



A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads

FUMIO MIYAJI, YASUSHI MATSUYAMA, YOSHIKAZU KANAISHI, KATSUNORI SENOH, TAKASHI EMORI, AND YOSHIAKI HAGIWARA, MEMBER, IEEE

I. INTRODUCTION

MEMORY capacity of SRAM's has quadrupled

Fig. 1. Block diagram of the RAM.

ISSCC1989

After the CCD work, Hagiwara and his team worked on the fast cache 25 nsec CMOS 4M bit SRAM silicon chip.

Important Contribution to the Modern Digital CMOS Image Sensor Technology

Yoshiaki (Daimon) Hagiwara

AIPS Digital CMOS image sensor consisting of three basic blocks.

Block (1) Retina Nerve Cells (Hagiwara 1975 Retina Photo Diode)

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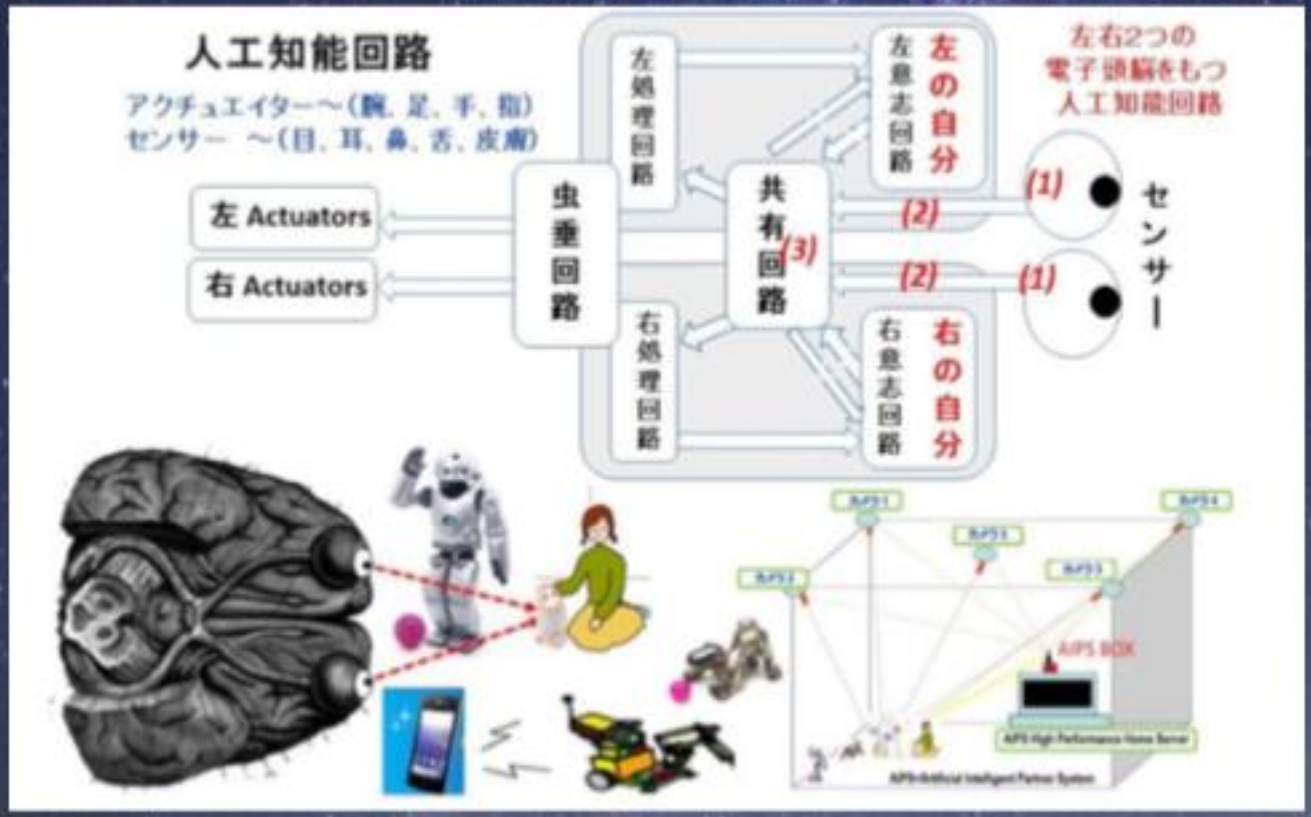
Block (3) Brain Memory Cells (Fast Cache SRAM and Slow NVRAM)



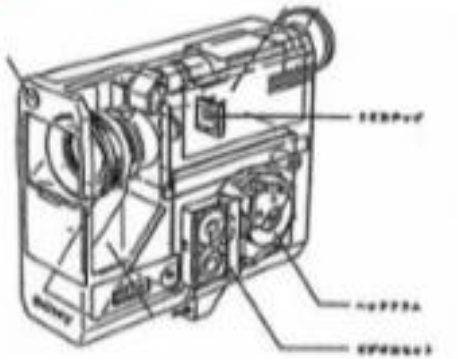
AIPS (Artificial Intelligent Partner System)

Yoshiaki (Daimon) Hagiwara

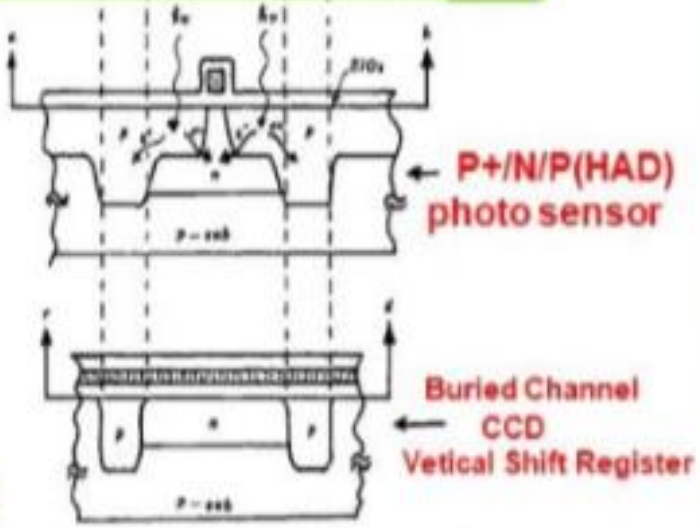
In 1978 for the first time in the world Sony published FT CCD image sensor with Hagiwara Photo Diode which was very highly light sensitive, with low noise and no image lag, which was the origin of the pinned photo diode as seen below.

570H x 498V One-Chip FT CCD Color Imager with P+/N/P HAD sensor , 1978

@ Tokyo Press Conference 1978 by Kazuo Iwama (Sony)



Sony announced the Video Camera and 8 mm Video Recorder in One Boc



But the world misunderstood that CCD imager is highly light sensitive. The truth is that Hagiwara Photo Diode is very highly light sensitive. Although CCD imagers had disappeared in the market, the Hagiwara Phodo Diode (which is also called now as the pinned photo diode) is still active and working well in digital CMOS image sensors.

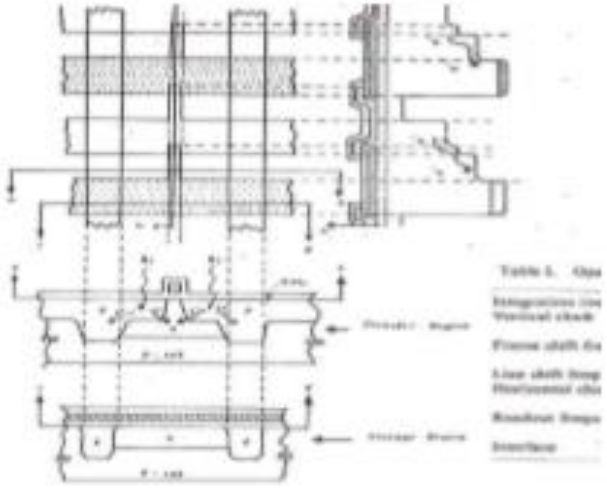
Hagiwara invented the pinned photo diode in 1975.

Hagiwara Diode, which is now called the pinned photo diode, was first introduced in CCD79 at University of Edinburgh, Scotland, UK.

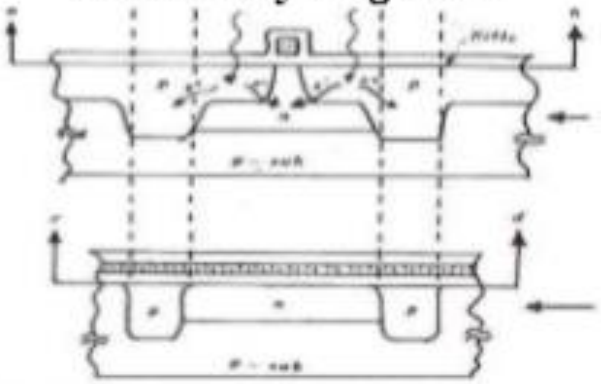
ADVANCES in CCD IMAGERS

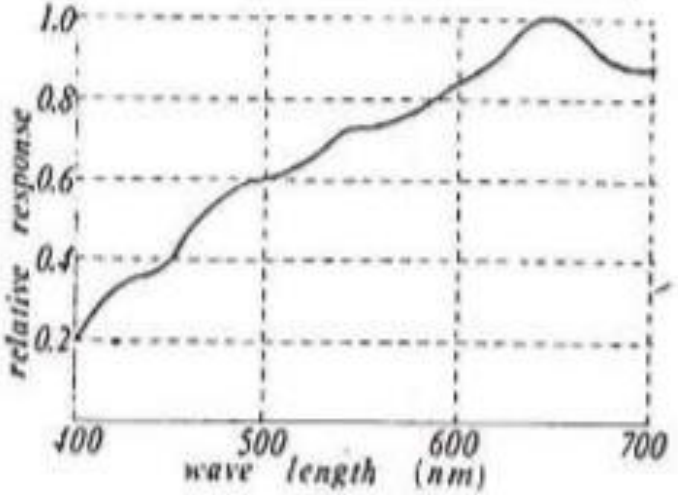
ABSTRACT

This paper provides a review of progress made in Sony on the technology and performance of CCD imagers for color video cameras. There are two basic approaches to realize a CCD image sensor, namely interline transfer organization and frame transfer organization. Sony has undertaken the design and fabrication of both types of the CC imagers, and the development effort resulted in four different version of CCD imagers. They are (1) a $242^H \times 494^V$ interline transfer CCD image with high density structure, (2) zigzag-transfer CCD with checker-patte sensing sites, (3) a $242^H \times 490^V$ CCD imager with SiO_2 exposed photo-sens arrays in frame transfer organization and (4) a $380^H \times 488^V$ F.T. CCD ima with narrow channel transfer gates. In this paper, the designs and operations of these CCD imagers and their camera systems are described detail.



the pinned photo diode invented by Hagiwara





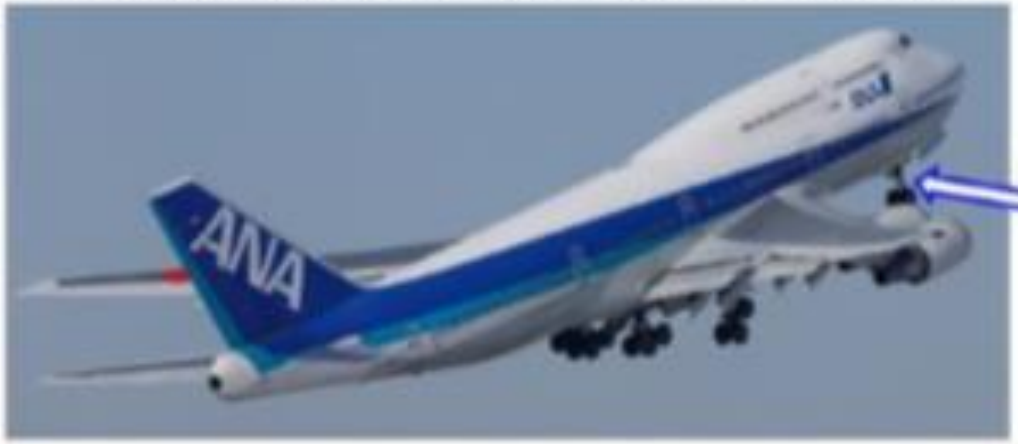
Hagiwara invented the pinned photo diode in 1975.

shiaki (Daimon) Hagiwara

In 1980 SONY also announced the Two Chip ILT CCD image sensor.

●イメージセンサーの開発背景（感度が命）

全日空ジャンボ機に2チップ構成カメラとしてソニーが商品化
ジャンボ機の離着時のもようを機内スクリーンに映し出す



XC-1 1980
Two-Chip Color Video Camera

ジャンボ機の
コックピットに搭載

Technical Report represented at Japan SSD conference Tokyo, May 1978

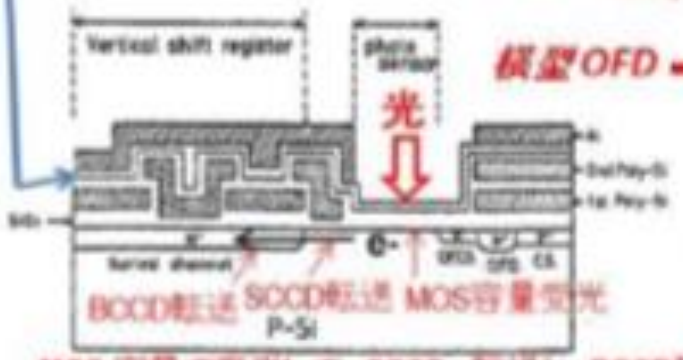
all solid state = robustness

透明電極(SnO2)露出型 の **MOS**型受光構造を採用、その後高感度**HAD**構造を採用しソニーの1人勝ちとなる

<ICX008>

2/3 Inch 120K Pixcel IT CCD Imager designed

one pixel = one picture element cell (画素)



縦型OFD

MOS 容量で受光して SCCD 転送と BCCD転送を使う

しかし受光窓が小さい(涙)

In 1984 SONY announced the SONY original HAD sensor, which is Hole Accumulation Photo Diode , another name for Hagiwara Diode 1975.

Origin of SONY HAD Sensor

Sony HAD (Hole Accumulation Diode) sensor is based on the dynamically operated P+NPNsub junction photo sensing structure invented by Yoshiaki Hagiwara and revealed in his patent in November 10, 1975

EXview HAD CCD II

Sonyのグローバルシャッターccdによりカメラの感度を向上

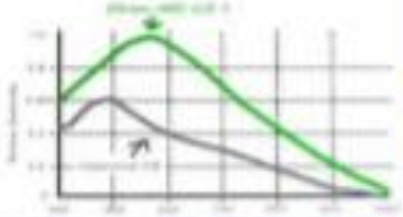
- 近赤外線を含む優れた感度
- 卓越した画像品質
- 拡張されたダイナミックレンジ
- 高速のシャッタースピードによる最小の輪郭線ぶれで鮮明な画像を提供

Sony EXview HAD CCDテクノロジーにより感度が向上し、他のCCDに比べて高い量子効率、少ないスミア、近赤外線領域でも高い感度を提供します。

Sonyは、光ダイオードの表面積拡大およびセンサーの深度を最適化し、独自のマイクロレンズを各ダイオードに設置して光をより多く集め、焦点を合わせることで、これを実現しています。

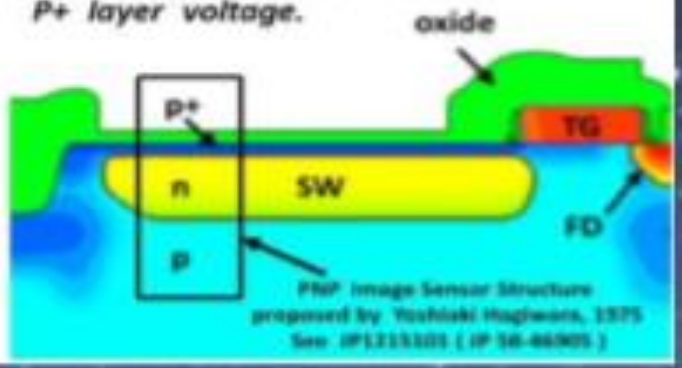
アプリケーション

- 照明条件が制御できない屋外アプリケーション
- 一般的に低光量である科学アプリケーション
- 高解像度または赤外線を必要とする工場の自動化



SONY HAD Sensor and pinned photo diode are the same thing.

This P+NPNsub (HAD) sensor was also named later as the pinned photo diode because the accumulated majority carrier holes in P+ layer pins the P+ layer voltage.

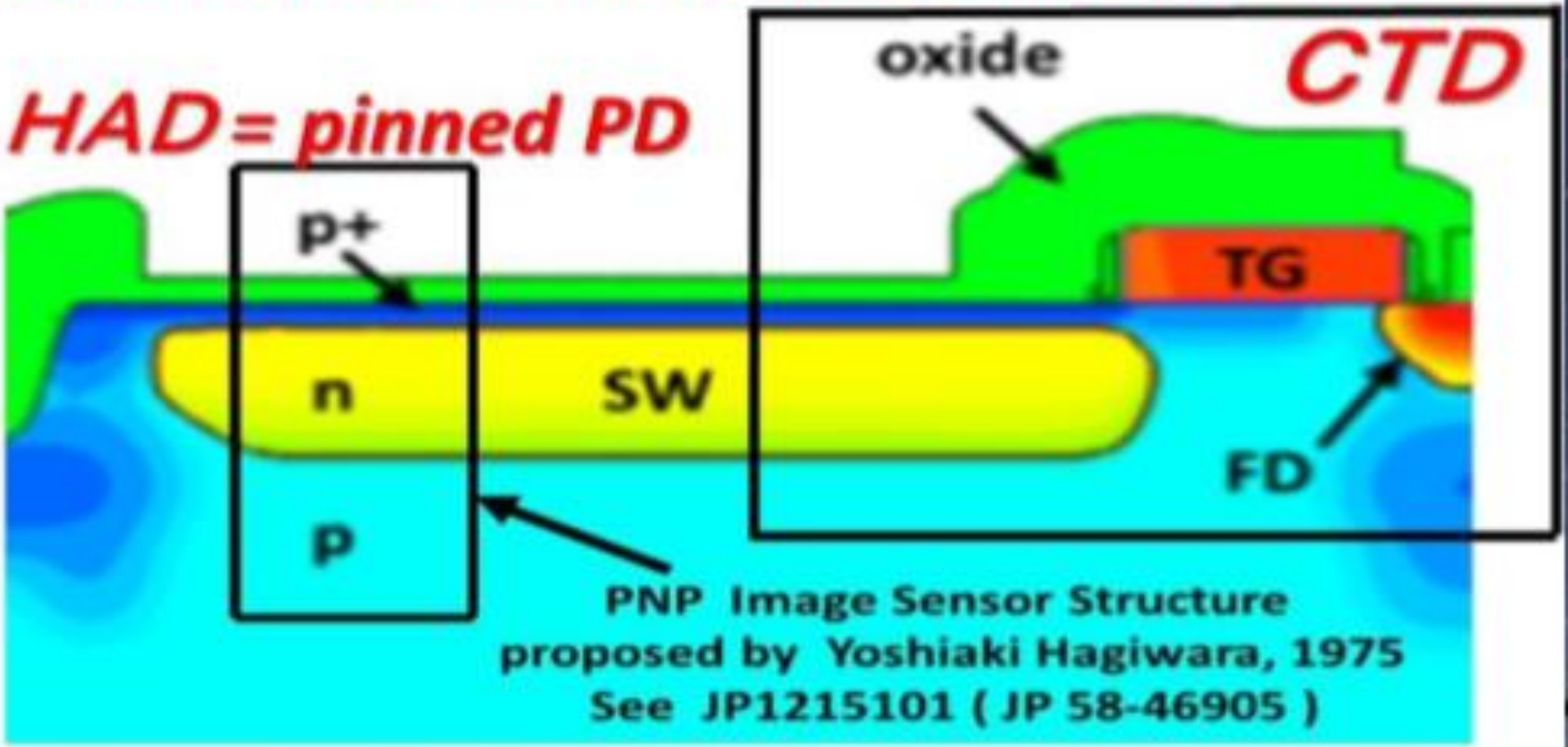


And later the pinned photo diode appeared widely in the world, another name for Hagiwara Diode 1975.

Teranish did not invent the pinned photo diode: Hagiwara at Sony did.

The pinned photo diode seen in Fossum 2014 paper, which is shown below, is the same as the SONY original HAD sensor invented by Yoshiaki Hagiwara at Sony in his 1975 patent.

Hagiwara invented the pinned photo diode in 1975.



After the CCD work, Hagiwara and his team worked on the fast cache 25 nsec CMOS 4M bit SRAM silicon chip with the dynamic bit line load for the first time in the world

...AL OF SOLID-STATE CIRCUITS, VOL. 24, NO. 5, OCTOBER 1989

A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads

FUMIO MIYAJI, YASUSHI MATSUYAMA, YOSHIKAZU KANAISHI, KATSUNORI SENOH, TAKASHI EMORI, AND YOSHIAKI HAGIWARA, MEMBER, IEEE

...—A 25-ns 4-Mbit CMOS SRAM with 512K word × 8-bit orga- ... has been developed. The RAM was fabricated using a 0.5-μm ...ly and double-aluminum CMOS technology and was assembled ... 400-mil DIP. A small cell size of 3.6 × 5.875 μm² and a chip ...46 × 17.41 mm² were obtained. A fast address access time of 25 ... single 3.3-V supply voltage has been achieved using our newly ...d dynamic bit-line load (DBL) circuit scheme incorporated with an ...transition detector (ATD), divided word-line structure (DWL), ...ge sense amplifier, and low-noise output circuit approach. A low ... current of 46 mA at 40 MHz and low standby currents of 70 μA ...d 5 μA (CMOS) were also attained.

I. Introduction

...E MEMORY capacity of SRAM's has quadrupled

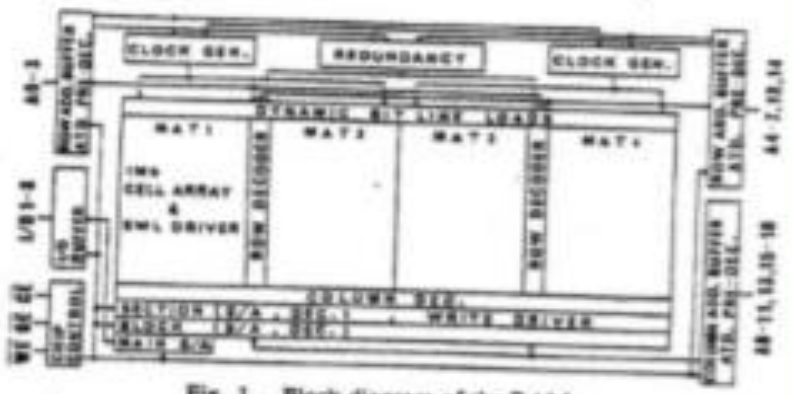


Fig. 1. Block diagram of the RAM.

ISSCC1989 paper

After the CCD work, Hagiwara and his team worked on the fast cache 25 nsec CMOS 4M bit SRAM silicon chip with the dynamic bit line load for the first time in the world

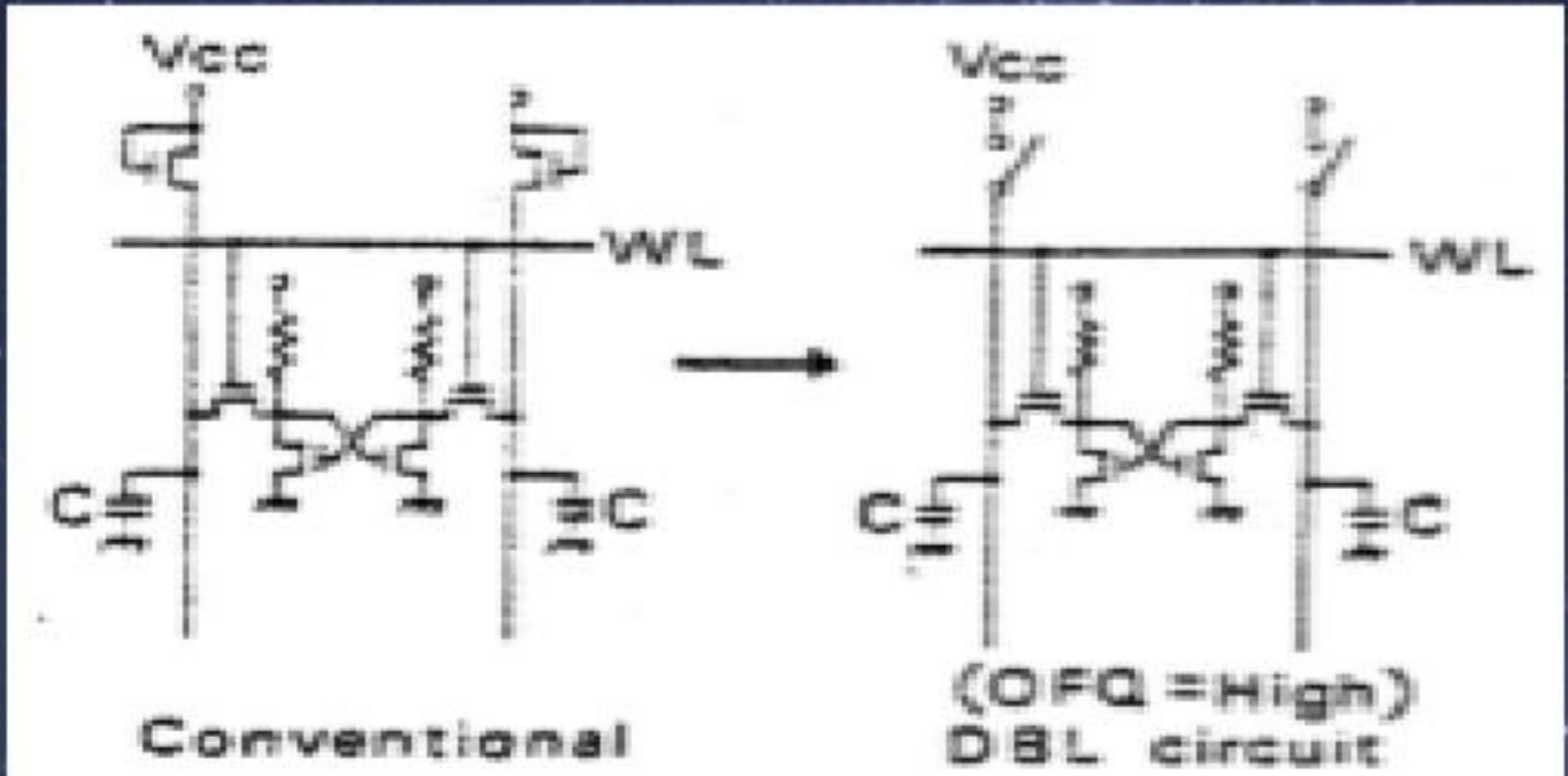


Fig. 6. Concept of DBL.

ISSCC1989 paper

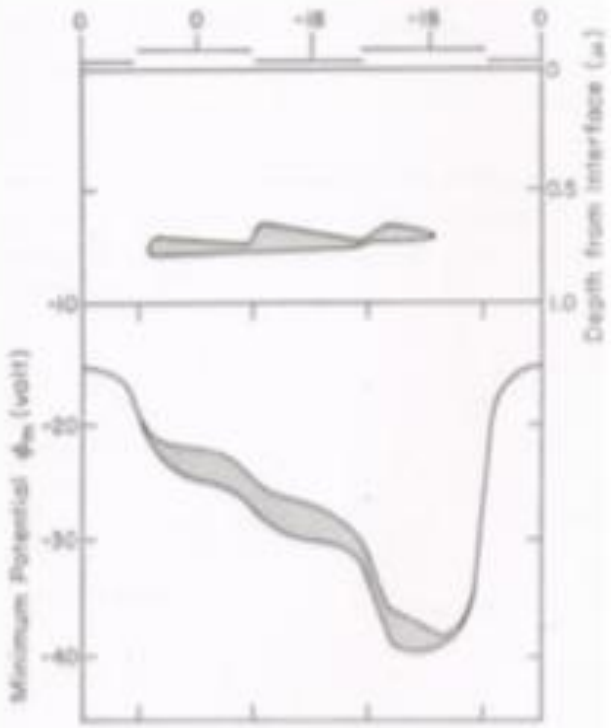
Hagiwara was working on the buried channel type CCD charge transfer analysis, using IBM360 computers for his device simulation, which was published in ISSCC1974 in Philadelphia.

Charge-Coupled Devices and Applications

Chairman

Lewis M. Terman

My PhD thesis paper
on buried channel CCD
at ISSCC1974, in Philadelphia, USA

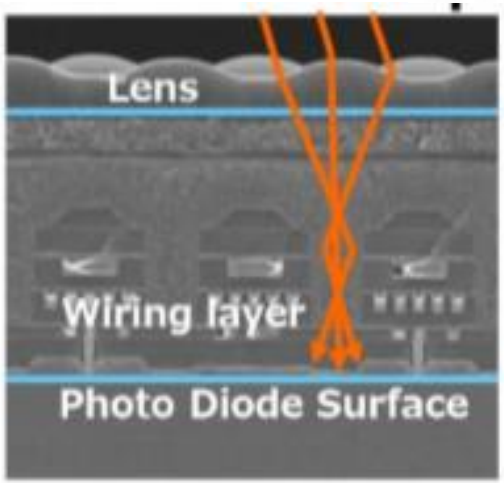


Prof. T. C. McGill

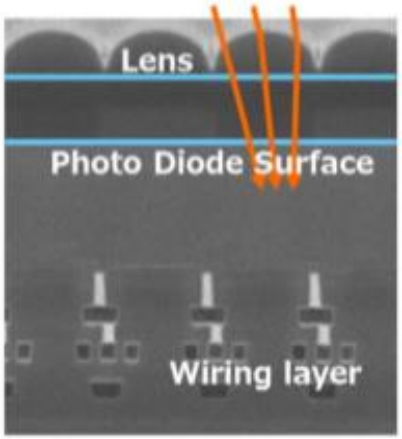
Prof. C. A. Mead

Sensitivity

Cross-sectional photos



(Light guide)

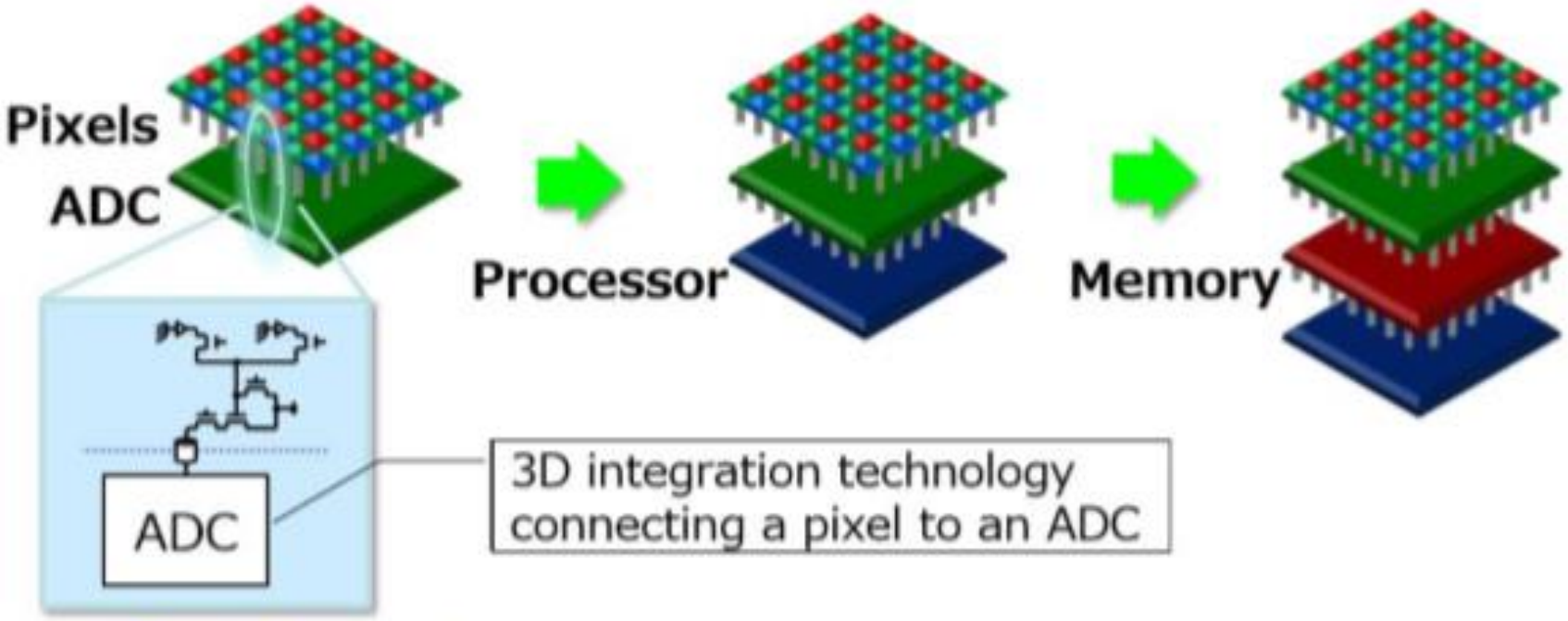


Back-illuminated CIS

Front-illuminated CIS
(without light guide)

Back-illuminated CIS

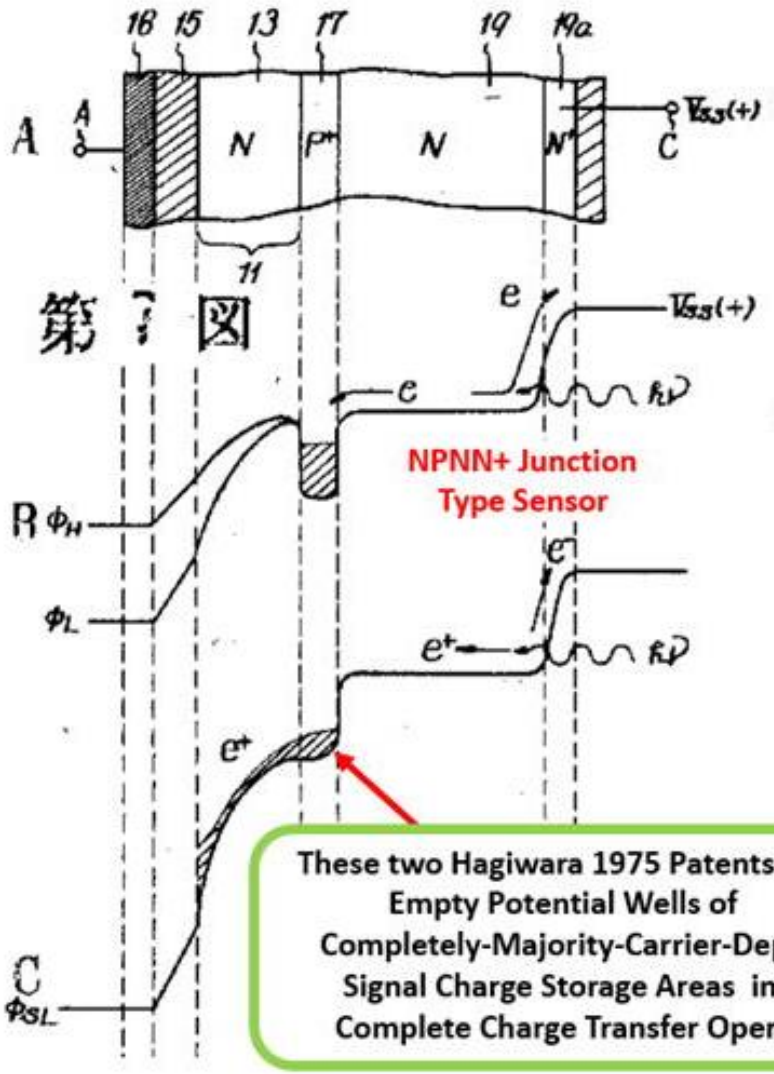
Multi-functionality of Image Sensors



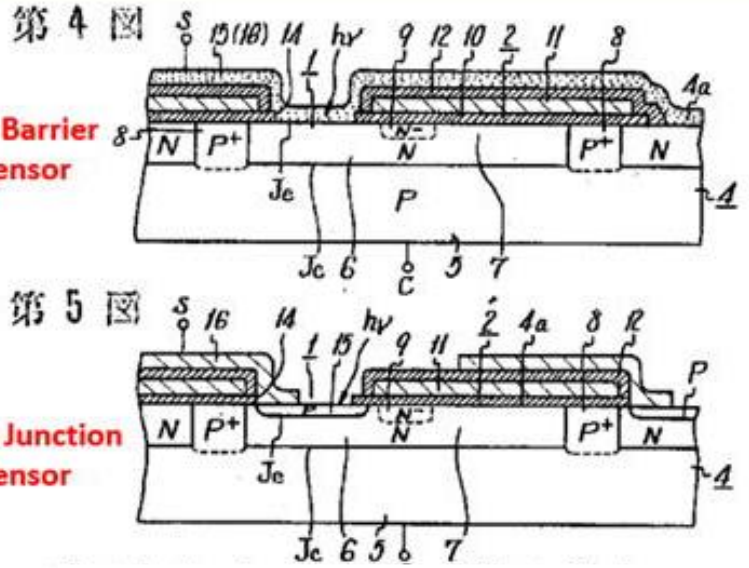
Requirements

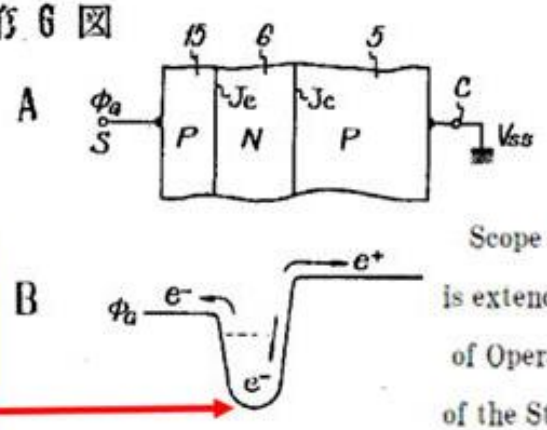
- Advancement in three-dimensional LSI technology

NPNN+ Junction type Pinned Photo Diode
See Japanese Patent (1975- 127647)



P+N-Psub Junction type Pinned Photo Diode
See Japanese Patent (1975-134985)





These two Hagiwara 1975 Patents showed Empty Potential Wells of Completely-Majority-Carrier-Depleted Signal Charge Storage Areas implying Complete Charge Transfer Operations.

Scope of Patent Right is extended over all kinds of Operations and Usage of the Structure defined in the Patent Claims.

Yoshiaki Hagiwara @SONY invented the Pinned Photo Diode in 1975.

For the original document, visit and search the Japanese Official Patent Web :

https://www4.jplatpat.inpit.go.jp/eng/tokujitsu/tkbs_en/TKBS_EN_GM101_Top.action

Document No.（1975-134985） on the P+NPNsub junction type PPD and

Document No.（1975-127647）on the NPNN+ junction type PPD、

Both filed by Yoshiaki Hagiwara in 1975 at Sony.

SONY original HAD and Pinned Photo Diode are the same thing.

Both were invented and defined in these two Japanese Patents by Hagiwara at SONY in 1975.