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Two Phase CCD with Narrow-Channel Transfer Regions

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When the channel width of a FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of threshold voltage is observed. This narrow-channel effect has been applied successfully in creating an asymmetrical potential well under an electrode for two phase CCD operations. The basic performance of this new structure has been evaluated in a 242 element analog delay line with 60 μm channel width and 36 μm element length. Observed inefficiencies per transfer are in the low 10^{-4} for surface channel versions and in the low 10^{-5} for buried channel versions.

§1. Introduction

When the channel width of a FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of threshold voltage is observed.[1,2] This narrow channel effect has been applied successfully in creating an asymmetrical potential well under an electrode for two phase CCD operations. Figure 1 shows cross sectional views of the electrode for two phase CCD structure. For the structure fabricated, each electrode has one large storage region of 60 μm width and six narrow-channel transfer regions of 4 μm width. In the bottom part of the figure, the cross section of one of the narrow-channel transfer regions is illustrated. The channel stop regions (p) surrounding the narrow channel can be formed by self-aligned ion implantation. The actual potential rise of this restricted region with respect to the wide-channel storage region can be controlled by the amount of the ion implantation dose and subsequent anealing conditions.

In Fig. 2, the actual measured channel potentials are plotted against the gate voltage for the structure fabricated. Both surface and buried channel versions of the device can be built with the same fabrication process, and are compared in the figure.

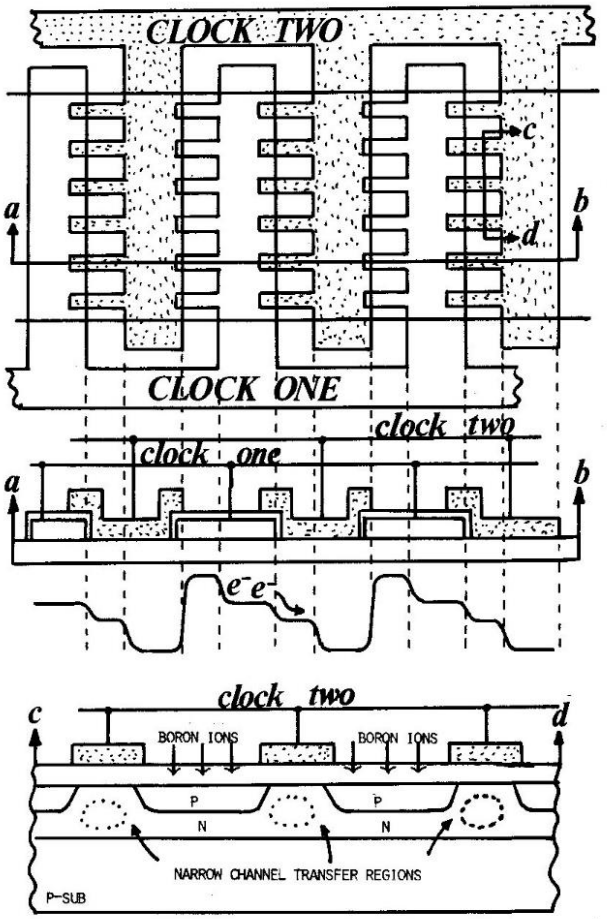

Fig. 1. Top and crosssectional views of the electrode structure for two phase CCD with narrow-channel transfer regions.

§2. Device Fabrication

The structure is fabricated on a *p*-type silicon substrate of a doping level of about 5×10^{14} cm^{-3}. A first level of phosphorus-doped polysilicon is deposited onto an oxidized silicon wafer and defined to form the firt set (clock one) of electrodes. The exposed oxide is then removed and a new gate oxide is thermally grown. Subsequently, the second set (clock two) of electrodes are formed by the second level of polysilicon deposition. Then, using the polysilicon patterning as an ion implantation mask, boron ions are implanted into the silicon substrate through the exposed portions of the thermally grown oxide. This

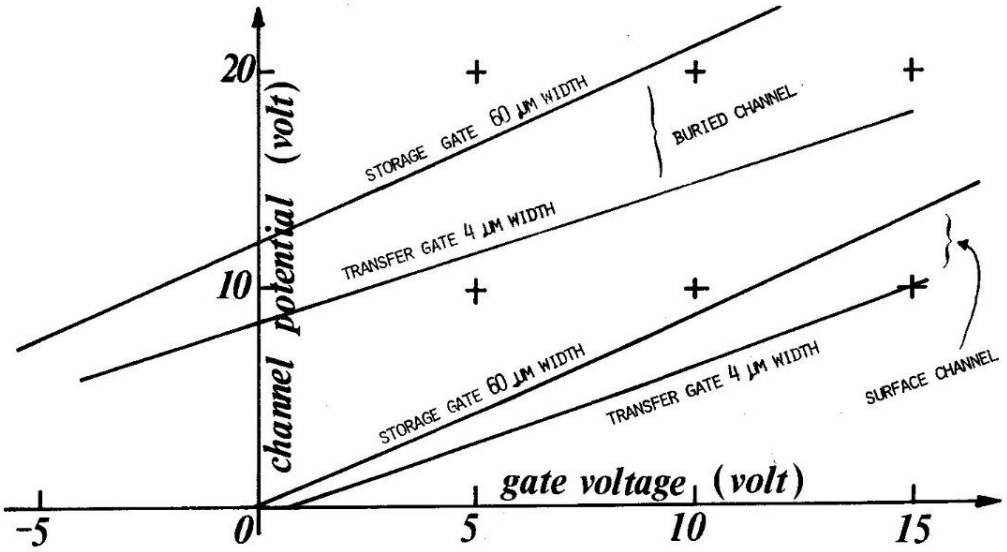

Fig. 2. The actual measured channel potentials plotted against the gate voltage for both surface and buried channel versions.

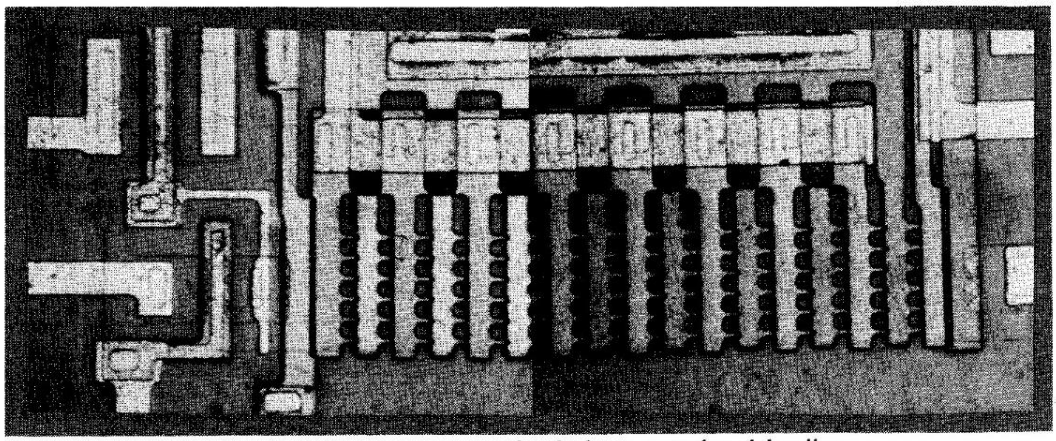

Fig. 3. The end sections of 242 element analog delay line.

step provides self-aligned channel stops which surround the narrow-channel transfer part of each electrode. The side-diffusion effect of the implanted boron ions in the subsequent annealing steps works on towards narrowing the actual transfer channel width further down from the value of 4 μm, which was originally fixed by the polysilicon electrode definitions. The oxide thickness under the both sets (clock one and two) of electrodes is 0.13 μm, and the ion implantation dose for the buried channel is taken to be 1.5×10^{12} cm^{-2} for the particular device reported in Fig. 2.

§3. Device Characteristics

Both surface channel versions and buried channel versions of the described structure have been built. Figure 3 shows the end sections of a 242 element analog delay line with 36 μm element length. The channel length of the transfer and storage electrode are 6 μm and 12 μm respectively. The channel width of the storage part is 60 μm while each storage part is connected to the next by six transfer channels of 4 μm width, which are positioned in 10 μm pitch. The input and output wave forms are shown in Fig. 4 for a typical device fabricated in buried channel version. The transfer inefficiencies per transfer of less than 5×10^{-4} for surface channel versions and less than 2×10^{-5} for buried channel versions have been measured at element rate of 5 MHz and clock voltage of 12 volts. They may be frequency independent up to frequencies corresponding to the limitations imposed by the speed of the free charge transfer.

§4. Summary

A new electrode structure for two phase CCD is introduced. The built-in directionality

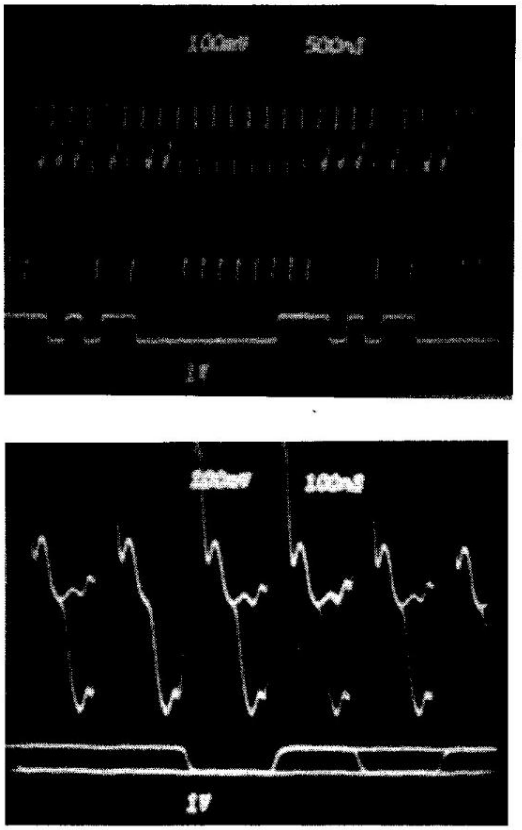

Fig. 4. Input and output wave forms for 242 analog delay line in buried channel version.

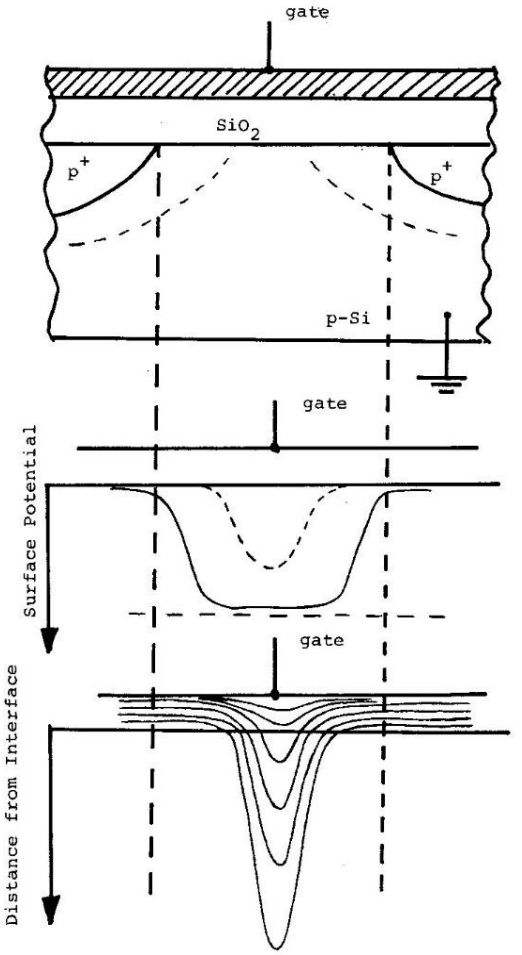

Fig. 5. Electrode structure and channel potential profile of narrow-channel CCD structure in surface channel version.

is achieved by narrowing the transfer channels of each electrode, effectively producing narrow-channel transfer regions for each storage electrode. The basic performance of this new structure has been evaluated in a 242 element analog delay line with 60 μm channel width and 36 μm element length. Observed inefficiencies per transfer are in the low 10^{-4} for surface channel versions and in the low 10^{-5} for buried channel versions.

APPENDIX

A.1 Electrostatic Potentials of Narrow Channel CCD's

(a) Surface Channel

This work originated from the simple speculations on the question of how small a CCD can be built in principle. When the channel is relatively wide, the channel potential at the center of the channel is very close to the value calculated by one dimensional analysis. However, as the CCD structure becomes smaller and the channel width becomes narrower, the potential well becomes shallower due to the two dimensional electrostatic effects as illustrated in Fig. 5. This potential rise is calculated and the results are plotted as the equipotential curves. For the substrate doping level of 5×10^{14} cm^{-3} and the gate voltage of 10 volt, the channel potential is normally about 9.5 volt according to one dimensional calculation and the corresponding depletion width is about 5 μm. However, as seen in Fig. 6, when the channel width becomes 5 μm, the channel potential becomes about 7.7 volt, and this narrow channel effect decreases the depletion width drastically to the value of 2 μm.

In this calculation, the side diffusion effect of channel stops are also included, and hereby the value of the parameter ΔR_p indicates the degree of the side diffusion effect of the channel stops. In Figs. 7 and 8, the equipotential curves of the narrow channel potential profiles are illustrated for the case in which the side diffusion effects are increased as the parameter ΔR_p

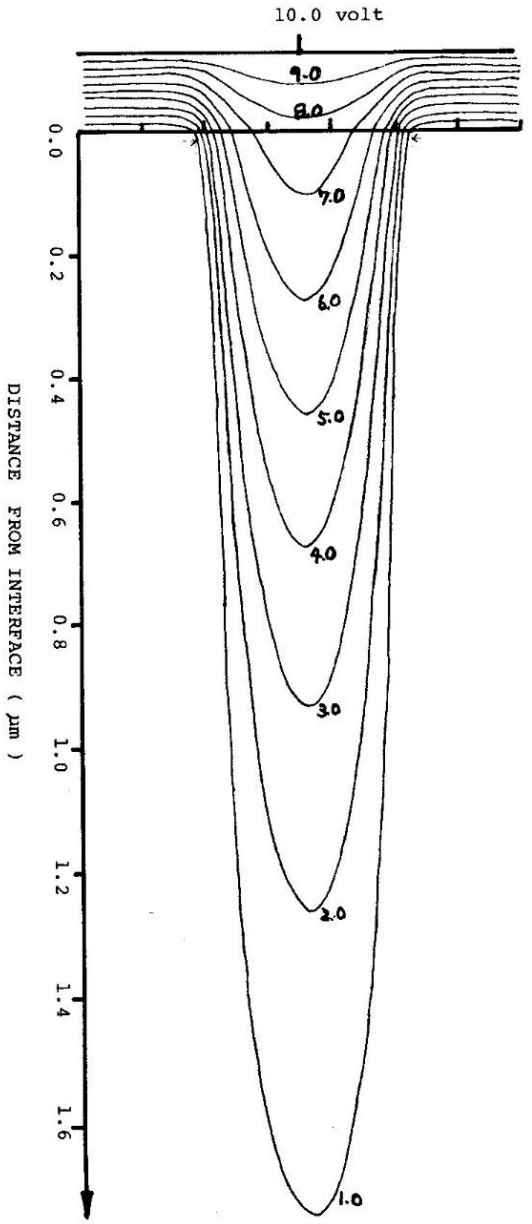

Fig. 6. Equipotential curves of the electrostatic potential profile of narrow channel CCD with $X_0=0.13\ \mu m$, $NA=5\times10^{14}\ cm^{-3}$, $W=5\ \mu m$, $NS=5\times10^{18}\ cm^{-2}$, $\Delta R_p=0.4\ \mu m$ and $\phi_{gate}=10.0$ volt.

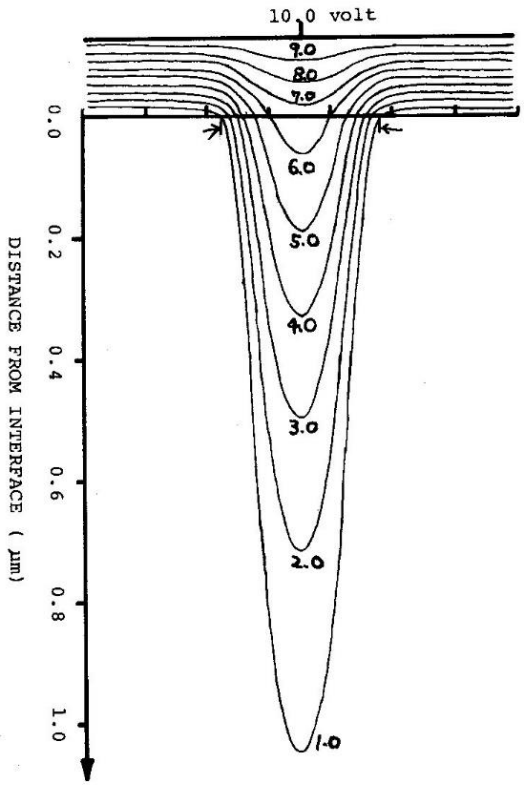

Fig. 7. Equipotential curves of the electrostatic potential profile of narrow channel CCD with $X_0=0.13\ \mu m$, $NA=5\times10^{14}\ cm^{-3}$, $W=5\ \mu m$, $NS=5\times10^{18}\ cm^{-2}$, $\Delta R_p=0.6\ \mu m$ and $\phi_{gate}=10.0$ volt.

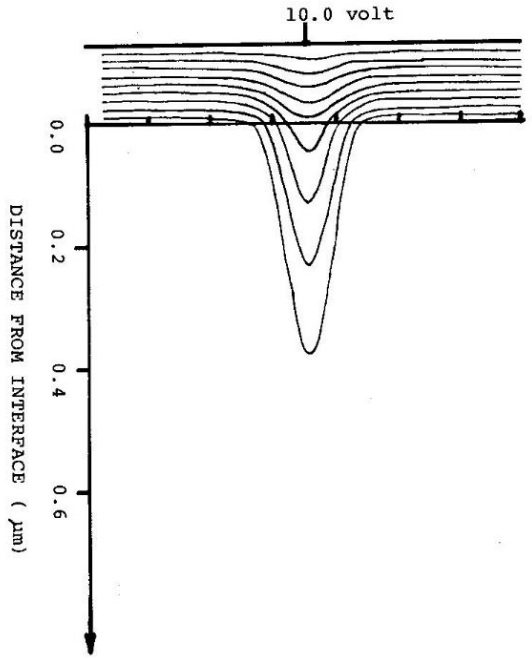

Fig. 8. Equipotential curves of the electrostatic potential profile of narrow channel CCD with $X_0=0.13\ \mu m$, $NA=5\times10^{14}\ cm^{-3}$, $W=5\ \mu m$, $NS=5\times10^{18}\ cm^{-2}$, $\Delta R_p=0.8\ \mu m$ and $\phi_{gate}=10.0$ volt.

indicates the actual increase. Figure 9 summarizes the results reported in Fig. 6 through Fig. 8. For $\Delta R_p=0.0\ \mu m$, the value 8.58 volt corresponds to the channel potential of the idealized step or rectangular profile of the channel stops. These results were obtained by actual numerical calculations of two dimensional Poisson's equation. When the model is further simplified and idealized as seen in Fig. 10, the potential rise of the narrow channel effect can be calculated analytically. The boundary conditions at $z=0.0$, $z=W$, and $x=X_D$

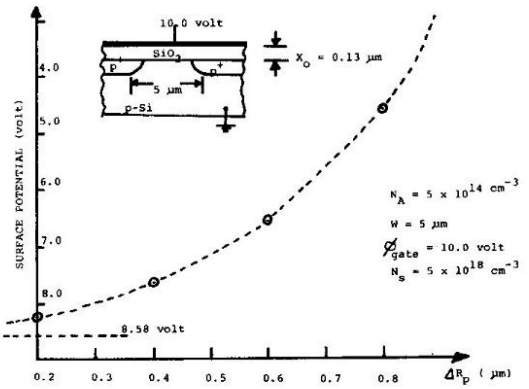

Fig. 9. The surface potential plotted against the side diffusion parameter ΔR_p of the channel stops for the channel width W of 5 μm.

are taken to be $\psi = 0.0$ in this analysis. The results are plotted in Fig. 11 through Fig. 13 to obtain the qualitative dependences of the narrow channel effects.

(b) Buried Channel

For the buried channel case, the same two dimensional numerical calcutions were performed for the structure indicated in Fig. 14 and the channel potentials are plotted along the z-direction perpendicular to the direction of the charge flow as seen in Figs. 15 and 16. The results are summarized in Fig. 17. For these calculations, the channel width of 7 μm is assumed. As seen in these results, the narrow channel effects are more prevailing in buried channel CCD's.

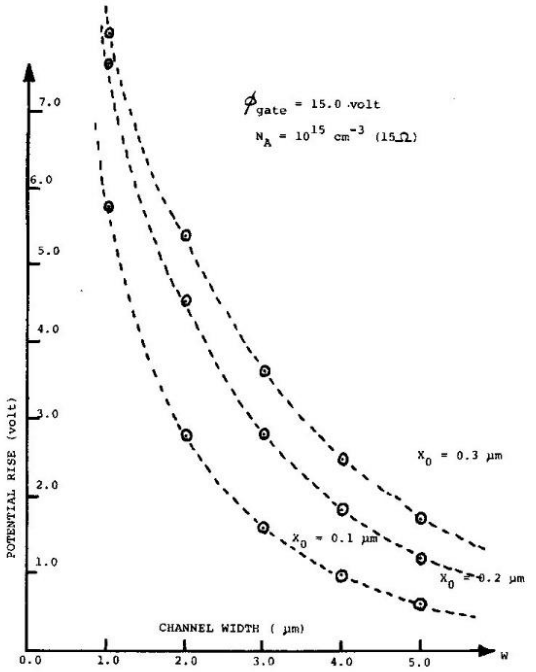

Fig. 11. The potential rise plotted against the idealized channel width for the substrate doping level NA of 10^{15} cm^{-3}.

References

1) K. E. Kroell and G. K. Ackermann: "Threshold Voltage of Narrow Channel Field Effect Transistors," Solid-State Electronics **19** (1976) 77.
2) K. O. Jeppson: "Influence of the Channel Width on the Threshold Voltage Modulation in MOSFETS," Electronics Letters, 10th of July (1975) vol. 11, No. 14.

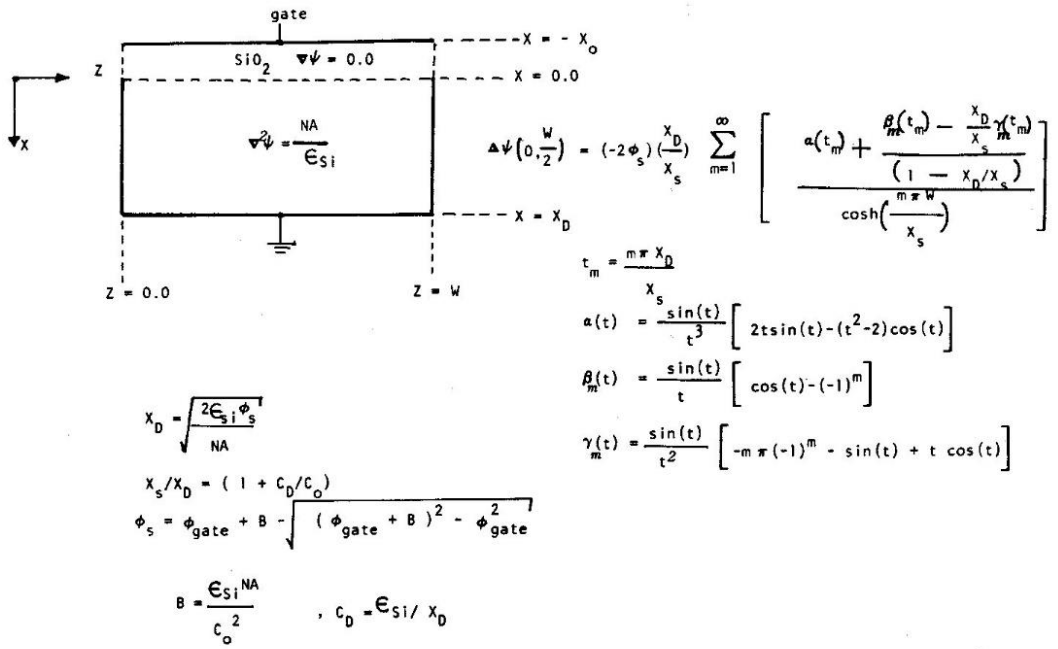

Fig. 10. The simplified and idealized model of two-dimensional narrow-channel effect calculation.

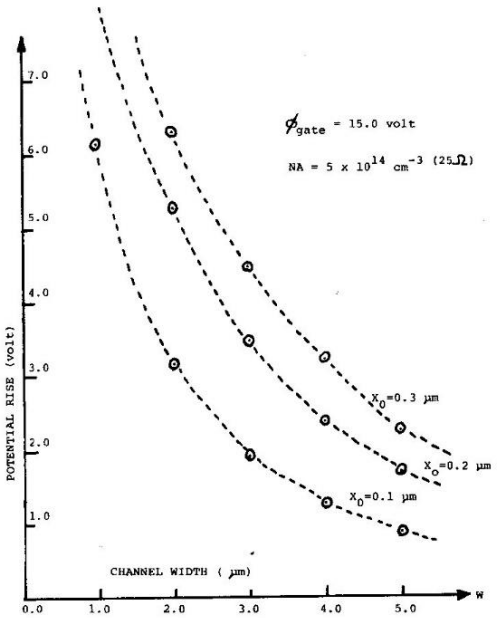

Fig. 12. The potential rise plotted against the idealized channel width for the substrate doping level NA of 5×10^{14} cm^{-3}.

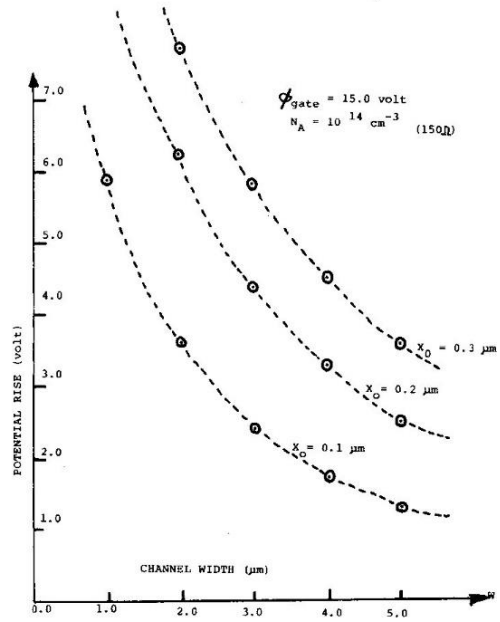

Fig. 13. The potential rise plotted against the idealized channel width for substrate doping level NA of 10^{14} cm^{-3}.

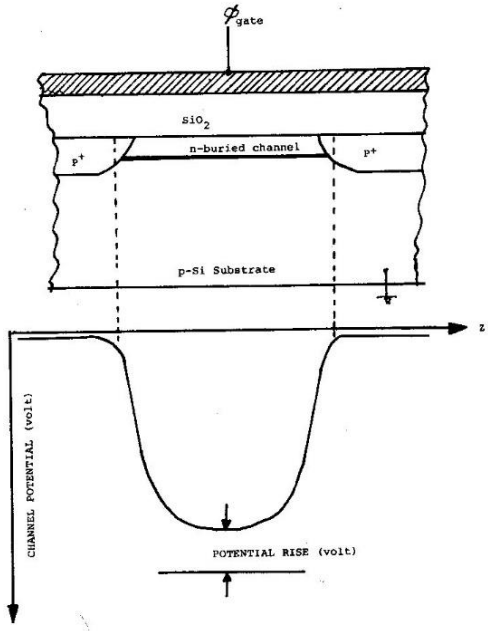

Fig. 14. Electrode structure and electrostatic potential of narrow channel buried channel CCD's.

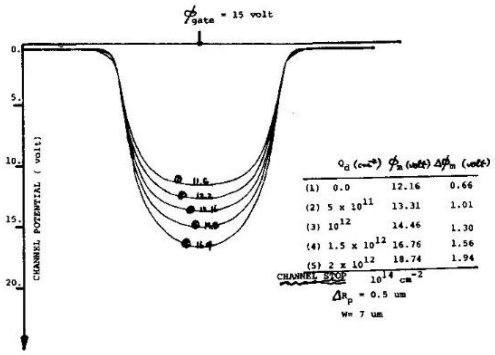

Fig. 15. The channel potentials of narrow-channel BCCD's with the buried channel ion implantation dose Q_d as the parameter for the channel stop dose of 10^{14} cm^{-2}.

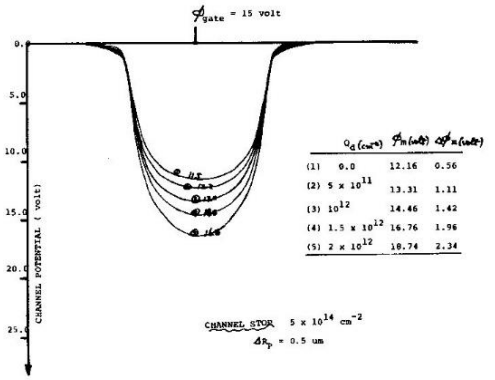

Fig. 16. The channel potentials of narrow-channel BCCD's with the buried channel ion implantation dose Q_d as the parameter for the channel stop dose of 5×10^{14} cm^{-2}.

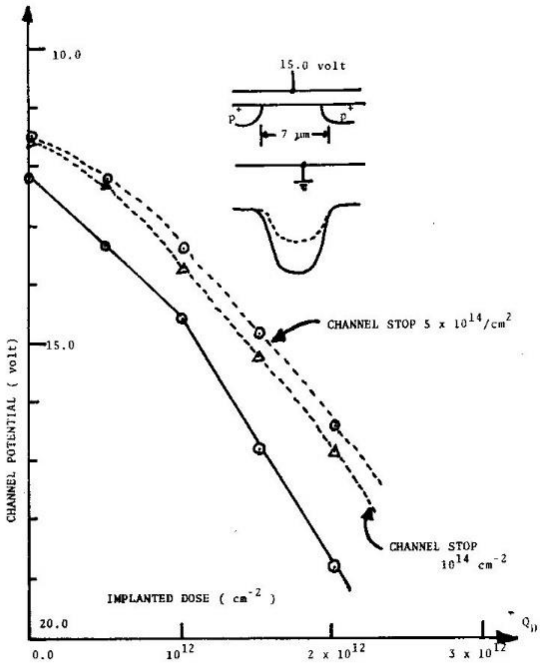

Fig. 17. The channel potentials of narrow-channel BCCD's plotted against the buried channel implantation dose Q_d with the channel stop dose as a parameter for the case of the 7 μm channel width.