Chapter 3

APPENDIX II : Influence of Interface States on Incomplete Charge Transfer in Overlapping Gate CCDs

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The Influence of Interface States on Incomplete Charge Transfer in Overlapping Gate Charge-Coupled Devices

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***Abstract*—A simple and accurate model is used to estimate the incomplete charge transfer due to interface states trapping in the overlapping gate charge-coupled devices. It is concluded that trapping in the interface states under the edges of the gates parallel to the active channel limits the performance of the devices at moderate and low frequencies. The influence of the device parameters, dimensions, and clocking waveforms on the signal degradation is discussed. It is shown that increasing the clock voltages, increasing the signal charge, or using push clocks reduces the incomplete charge transfer due to interface state trapping.**

I. Introduction

THE incomplete charge transfer due to trapping in interface states at the semiconductor-oxide interface imposes limitations on the performance of charge-coupled devices at moderate and low frequencies, where the incomplete free charge transfer is very small [1]–[5]. Several authors [6]–[8] have studied the effects of interface state trapping. Carnes and Kosonocky [7] have measured the large signal losses due to the interface states trapping in charge-coupled devices. Tompsett [8] has also calculated the transfer inefficiency and the reduction in the signal-to-noise ratio (SNR) of the output signal due to interface states for three-phase charge-coupled devices.

This paper presents a study of the incomplete charge transfer due to trapping in interface states in overlapping gate charge-coupled devices[1] operated with a background charge and its dependence on frequency, device parameters, dimensions, and clocking waveforms, to establish guiding design rules for the operation of these devices with optimum performance. Section II describes how trapping in interface states results in incomplete transfer. Section III presents the theoretical model and the basis of our approximations. Sections IV–VII derive expressions for the net charge trapped in the interface states under the storage gates, the transfer gates, and the edges of the gates. Section VIII calculates the signal degradation due to trapping in interface states for a two-phase overlapping gate charge-coupled device. A discussion of the results and conclusions is presented in Sections IX and X.

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[1] We have considered the overlapping gate structure as it seems presently to be the most technically promising CCD structure for the potential large scale applications of these devices [2], [4]. However, most of the analysis, discussion, and conclusions given in this paper apply also to the other CCD structures.

II. Incomplete Charge Transfer Due to Trapping in Interface States

In Fig. 1, one unit cell of an overlapping gate charge-coupled device using silicon gate technology is shown [9]. If a voltage is applied to one of the storage electrodes, a potential well is created at the interface where signal charge can be stored. Some of this charge will be trapped in interface states. During the first stages of the transfer of charge to the next storage site, some carriers will also be trapped in interface states under the transfer gates. In the latter stages of the transfer process, the relatively large fringing fields under the transfer gates sweep out the mobile carriers very rapidly and the interface states then start to emit the captured carriers. According to the Shockley–Read–Hall rate equations [10] the emission time constant τ_e of the interface states varies exponentially with their energy level relative to the band edge. If the emission time constant of the interface states in a given energy range is smaller than the transfer time, then most of the trapped carriers in these

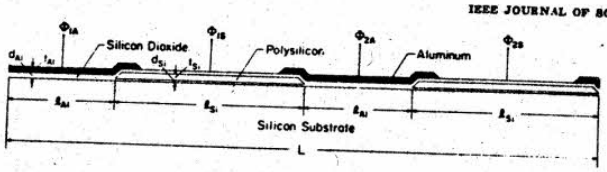

Fig. 1. One unit cell of the overlapping gate structure using the silicon gate technology.

states are emitted and can join the main packet. Interface states with an emission time constant equal or larger than the transfer time will emit only a fraction of the trapped carriers. Since the storage gate is longer and has a thinner oxide than the transfer gate, the fringing fields under it are much smaller than under the transfer gate. The residual charge under the storage gate, in the latter stages of the charge transfer process, decreases exponentially with a time constant that depends on thermal diffusion and the small fringing fields [1]–[3], [14]. Interface states continue to capture carriers from the residual signal charge until the residual charge becomes so small that emission from the traps becomes dominant. The nonemitted trapped carriers under the storage gate and the transfer gate are thus lost from the signal charge and will be emitted in the succeeding packets. If the next signal samples do not contain any charge, the interface states continue to emit the captured carriers until a signal sample containing charge passes. Then the empty interface state fill by capturing carriers from that signal sample. After its transfer, the trapped carriers are emitted and so on.

The charge captured by interface states from a large charge packet passing through the device is larger than the charge emitted into that packet, unless it has been preceded by an equal or larger charge packet. But the charge captured by interface states from a small charge packet passing through the device is smaller than the charge emitted into that packet, unless it has been preceded by an equal or smaller charge packet. Thus the interaction of the signal charge with the interface states results in incomplete transfer of charge from one storage site to another and imposes limitations on the performance of the overlapping gates charge-coupled devices.

The signal degradation due to the trapping of carriers in the interface states can be considerably reduced by using the fat zero scheme. In this scheme the zero signal is represented by a small background charge or "fat zero," so that charge packets are always flowing across the device [6]. Hence the interface states under the storage and transfer electrodes are filled every cycle. The net charge trapped from a signal charge packet will then be the difference between the captured charge it lost at each transfer and the charge emitted into that packet, by the interface states under the storage and transfer gates, which was trapped from the preceding charge packets. Since for a sufficiently large fat zero charge the capture time constant of the interface state is very small (as discussed later), the interface states will be almost completely filled during each cycle and similar net trapping occurs during every cycle. The incomplete transfer due to trapping in interface states is consequently reduced by orders of magnitude.

III. Model and Approximations

The interface states at the semiconductor-oxide interface are characterized by their density $N_{ss}(E)$ and capture cross section $\sigma_h(E)$. The capture and release of charge from these states is described by the Shockley–Read–Hall equation [10]. Assuming a p-channel[2] device and assuming that the interface is always kept under depletion to exclude the majority carrier and suppress any recombination between the trapped holes and electrons, the rate equation describing the occupation of the interface states at any energy E above the valence band is given by

$$\frac{dn_{ss}}{dt} = K_1(N_{ss} - n_{ss})p - K_2 n_{ss} \exp(-E/KT) \quad (1a)$$

$$K_1 = \sigma_h V_{th}/d \quad (1b)$$

$$K_2 = \sigma_h V_{th} N_v, \quad (1c)$$

where N_{ss} is the interface state density (states/cm^2 · eV), n_{ss} the density of filled interface (states/cm^2 · eV), and p the density per unit area of the mobile holes in the valence band at the interface. σ_h is the trap capture cross section for holes and V_{th} the average thermal velocity of the mobile carriers. d is the average thickness of the inversion layer at the interface, N_v the density of states in the valence band, and KT the electron-volt equivalent of temperature.

The first term describes the rate of capture of the mobile carrier and is proportional to the density p of the available mobile carriers and the density of the empty traps ($N_{ss} - n_{ss}$). The second term describes the rate of emission of the trapped carrier. This term is proportional to the density of the filled interface states and decreases exponentially as the trap energy increases.

The total rate of capture of the mobile carrier is then given by

$$\text{rate of capture} = -\frac{dp}{dt}\bigg|_{\text{capture}} = \int_0^{E_v} \frac{dn_{ss}}{dt}\, dE, \quad (2)$$

[2] The same discussion and analysis given below holds for n-channel devices. In this case the mobile electrons interact mostly with interface states near the conduction band edge.

where E_g is the energy gap. The mobile carrier continuity equation that describes the performance of the device must be modified to include this capture rate [2] (neglecting thermal generation currents):

$$\frac{\partial q}{\partial t} = -\nabla_x \cdot (J) - e\frac{dp}{dt}\bigg|_{\text{capture}} \tag{3}$$

where q is the surface charge density of the mobile carrier, e the electronic charge, J the sheet current density, and x the distance along the interface.

Thus, from the rigorous standpoint, the continuity equation (3) should be solved simultaneously with the nonequilibrium rate equations (1a) and (2) in the regions under the source and receiving storage gates and transfer gate. While a rigorous treatment is conceptually possible, the uncertainty in the parameters characterizing the interface states makes such an elaborate calculation unwarranted. However, with suitable approximations one can make calculations that give qualitatively reliable and quantitatively suggestive estimates of the incomplete transfer due to interface state trapping.

When charge-coupled devices are operated with the circulating background charge, interface states having an emission time constant larger than the cycle time remain almost completely filled all the time. These states capture carriers every cycle and do not get a chance to reemit an appreciable fraction of the captured carriers during the cycle time. Interface states with an emission time constant much less than the cycle time will be emptying and filling every cycle. These interface states have an energy of a few KT above the valence band edge (as shown later). Hence the interface states that make a substantial contribution to the incomplete transfer will be those with a time constant of the order of the clock cycle period and will lie within an energy range of the order of the thermal voltage. For the low interface state density obtainable with the present thermally grown oxide [11]–[13] the rate of capture or emission is quite small compared to the other terms in (3). Thus, one can obtain an accurate solution by the following procedure. First, the term in (3) due to trapping is neglected, and the continuity equation is solved to obtain the free charge transfer characteristics. The surface charge density profiles $q(x, t)$ are then used with the rate equations (1) and (2) to calculate the incomplete charge transfer due to trapping in interface states.

The precise values of the interface state density N_{ss} and capture cross section σ_A of the interface states; their distribution in energy over the bandgap; and their dependence on temperature, normal and tangential surface fields are not well known, and vary strongly with the type and preparation of the oxide over the active channel of the device [11]–[13]. For our purposes here, we will take N_{ss} and σ_A independent of all the previously mentioned parameters. However, if the exact energy dependence of N_{ss} and σ_A in the relevant part of the bandgap is accurately known, it can be easily incorporated in this model. Consistent with the same order of accuracy of the previous assumptions, we can also use average values of the mobile carrier concentration and neglect the effect of their spatial distribution under the electrodes, to further simplify the numerical calculation.

IV. Trap Occupation in Steady State and Transient

In steady state, the trap occupation can be obtained from (1a) and is given by

$$n_{ss} = \frac{N_{ss}}{\left(1 + \dfrac{K_2 \exp(-E/KT)}{K_1 p}\right)}. \tag{4}$$

The interface states are in equilibrium with the mobile carriers. Their occupation is described by the same quasi-Fermi level as the mobile carriers.

$$E_f = KT \ln \frac{K_2}{K_1 p} = KT \ln \frac{N_s \cdot d}{p}. \tag{5}$$

Following a sudden abrupt change in the mobile carrier concentration, say p_0 to p_1, the trap occupation changes to the new steady-state value corresponding to the new mobile carrier concentration p_1 with an effective time constant given by

$$\tau_{eff} = \frac{1}{K_1 p_1 + K_2 \exp(-E/KT)}. \tag{6}$$

If the effective time constant of the interface states τ_{eff} is smaller than the time constant τ measuring the variation of the mobile carrier density, then the trap occupation reaches steady state very rapidly and effectively equilibrates with the varying carrier density. That is, if $\tau > \tau_{eff}$, then

$$n_{ss}(t) = N_{ss} \Big/ \left[1 + \frac{K_2 \exp(-E/KT)}{K_1 p(t)}\right]. \tag{7}$$

Thus, the quasi-Fermi levels of the traps follows the quasi-Fermi level of the mobile carriers

$$E_f(t) = KT \ln \frac{N_s \cdot d}{p(t)}. \tag{8}$$

On the other hand, if $\tau < \tau_{eff}$, then the trap occupation fails to follow the variation of the mobile carrier. If we let $K_1 p(t) \gg K_2 \exp(-E/KT)$, then this occurs when the mobile carrier density falls to a level such that

$$K_1 \tau p(t) < 1. \tag{9}$$

For charge transfer from under a gate, we can define two regimes. First, when $K_1 p(t)\tau > 1$, the mobile charge is in effective equilibrium with the trapped charge. The total number of trapped carriers p_{tr} is given by

$$p_{tr}(t) = N_{ss}\left[E_s - KT \ln \frac{K_2}{K_1 p(t)}\right]. \tag{10}$$

Second, when $K_1 p(t)\tau < 1$, the mobile charge is no longer in equilibrium with the trapped charge. If we let t_4 be the time the emission mechanism becomes dominant,

then for $t > t_4$ the trap occupation is given by

$$n_{ss}(t) = \frac{N_{ss}}{1 + \dfrac{K_2 \exp(-E/KT)}{K_1 p(t_4)} \cdot \exp[-(t - t_4)K_2 \exp(-E/KT)]}; \quad (11)$$

and the interface states start to empty with a time constant that increases exponentially with the trap energy. The total number of trapped carriers is given by

$$p_{ss}(t) = N_{ss}\left[E_s - KT \ln K_2(t - t_4) - \frac{KT}{(t - t_4)K_1 p(t_4)}\right], \quad t > t_4. \quad (12)$$

So in this case the interface states above $E_f = KT \ln K_2(t - t_4)$ are almost full and those below it are nearly empty. The last terms in (10) and (12) show the dependence of the interface state occupation on the mobile carrier density.

V. Trapping in Interface States Under the Storage Gates

When a signal charge packet is stored under the storage gate, all the interface states trap carriers and are filled very rapidly down to a quasi-Fermi level given by (5). As the charge transfers to the next storage site, the residual charge decreases. In the complete charge transfer mode[3] the transfer of charge at the end of the charge transfer process (say after a time t_3) becomes limited by thermal diffusion and fringing fields. The residual charge under the storage gate is then given by

$$p(t) = p(t_3) \exp[-(t - t_3)/\tau], \quad t > t_3, \quad (13)$$

where the characteristic time constant τ depends on diffusion and fringing fields [2], [14].

Since the fringing fields under the storage gate are relatively small giving a rather large value of τ and the charge $p(t_3)$ is relatively large, the inequality

$$\tau K_1 p(t_3) > 1 \quad (14)$$

is satisfied at the beginning of this time interval. Hence, the mobile charge is in equilibrium with the trapped charge. However, at later times the free carrier density may fall to such a value that the interface states are no longer in equilibrium with the free carriers and the interface states begin to simply emit the charge trapped in them. This state pretains for times t such that

$$t > t_4 = t_3 + \tau \ln(K_1 p(t_3)\tau). \quad (15)$$

If the clock frequency f_0 is such that the charge transfer ends at a time t less than t_4, then the interface states will remain filled down to an energy defined by (8). When the next charge packet arrives, it fills all the interface states, and after it transfers the total number of trapped carriers is given by (10) with the proper value of $p(t)$. So, when the device is operated with a circulating background charge, or fat zero, the net charge trapped from a signal charge packet is maximum when it is preceded by a fat zero and is given by

$$\Delta q_{ss} = eA_{ss}N_{ss}KT \ln \frac{p_s(t)}{p_0(t)}, \quad (16)$$

where Δq_{ss} is the net charge trapped per transfer, A_{ss} the area of the storage gate, $p_0(t)$ and $p_s(t)$ are the residual charge under the storage gate at the end of the transfer time t for the fat zero charge and the signal charge, respectively. When the difference between $p_s(t)$ and $p_0(t)$, is relatively small, then

$$\Delta q_{ss} = eA_{ss}N_{ss}KT \frac{(p_s(t) - p_0(t))}{p_0(t)}. \quad (17)$$

It follows from (13) and (17), that the net charge trapped is almost independent of frequency. In addition all the interface states above an energy E_1 where

$$E_1 = KT \ln \frac{K_2}{K_1 p(1/2f_0)} \quad (18)$$

will always be filled with captured holes. If the charge transfer ends after a time $t > t_4$, then in the complete charge transfer the interface states under the original storage gate continue to emit the trapped charge for one whole transfer (or $(m - 1)$ transfer times for m transfers/cycle). This released charge is added to the next packet transferred into this storage bucket. When the next charge packet comes along, all the interface states are filled again. After this charge packet transfers, the interface states start to emit and so on. So when the device is operated with a circulating background charge, the net charge trapped from a signal charge packet at each transfer, for transfer time $t > t_4 + \tau$, is also maximum when preceded by a fat zero and can be obtained directly from (12).

$$\Delta q_{ss} = eRA_{ss}N_{ss}KT \frac{1}{(t - t_4)K_1}\left[\frac{1}{p_0(t_4)} - \frac{1}{p_s(t_4)}\right] \quad (19)$$

where $p_0(t_4)$ and $p_s(t_4)$ are the residual charge under the storage gate after a time t_4 [as defined in (15)] for the fat zero charge and the signal charge, respectively, and R is a fraction given by

$$R = \frac{(m - 1)t}{mt - t_4} = \frac{m - 1}{m} \cdot \frac{1}{1 - f_0 t_4}, \quad (20)$$

where m is the number of transfers/bit. If t_4 is smaller than the cycle time, then $t_4 f_0 < 1$ and for $m = 2$, $R \simeq \frac{1}{2}$. If the difference between $p_s(t_4)$ and $p_0(t_4)$ is relatively small, then

$$\Delta q_{ss} = \tfrac{1}{2}eA_{ss}N_{ss}KT \frac{\tau}{(t - t_4)} \cdot \frac{[p_s(t_4) - p_0(t_4)]}{p_0(t_4)}. \quad (21)$$

Thus, for transfer times $t > t_4 + \tau$, the net charge trapped/transfer decreases almost directly with the clock

[3] In the complete charge transfer mode all the charge under the storage gate is transferred to the following gates; none is deliberately retained. (See [2] and [5].)

frequency. Also, all the interface states above an energy E_1 are filled with captured holes. E_1 is almost independent of the signal charge and is given by

$$E_1 = KT \ln K_2(mt - t_4). \tag{22}$$

VI. Trapping in Interface States Under the Transfer Gates

The surface potential and the surface potential gradient under the gates of an overlapping gate charge-coupled device along the silicon-silicon oxide interface are plotted in Fig. 2. These plots are obtained from a solution of the two-dimensional Poisson equation for substrate doping of 8×10^{14}/cm^3 and 10^{14}/cm^3 [14]. The electrode voltages correspond to the latter stages of the charge transfer with a signal charge in the receiving storage gate. Since the transfer gate is shorter and has a thicker oxide than the storage gate, the fringing fields under it are much larger than under the storage gate. Typical values of single carriers transit time under the transfer gate are of the order of a few nanoseconds.

When a signal charge packet transfers from one storage site to the next, interface states under the transfer gate trap some of the charge during the first stages of the transfer process. Since fringing fields under the transfer gates are relatively large, the mobile carriers are swept out very rapidly and the emptying of the interface states begins earlier in the transfer process. Thus for all transfer times t of interest

$$t > t_{4tr}. \tag{23}$$

The trapped carriers emitted before the transfer ends will join the main packet. During the latter times of the cycle, a larger fraction γ of the emitted carrier will drift backwards to join the succeeding packet of charge, and a smaller fraction $(1 - \gamma)$ will drift forward to join the original packet of charge. Because of the asymmetrical surface potential distribution γ is greater than one half. Then in the next cycle, during the transfer of the next packet of charge, the interface states under the transfer gate capture some charge, and so on. From the plots of the average mobile carrier concentration under the transfer gates for a two-phase overlapping gate CCD in Figs. 3 and 5, it is clear that the interface states will capture carriers for a time interval Δt. During that time interval an average carrier concentration p_{av} may be defined. The traps fill with an effective time constant τ_{eff} given by

$$\tau_{eff} = \frac{1}{K_1 p_{av} + K_2 \exp(-E/KT)} \simeq \frac{1}{K_1 p_{av}}. \tag{24}$$

The filling probability or the fill factor F of the traps is given by

$$F = [1 - \exp(-\Delta t/\tau_{eff})]. \tag{25}$$

For transfer times $t > t_{4tr}$ the interface states empty according to (11) and the total trapped carriers is given

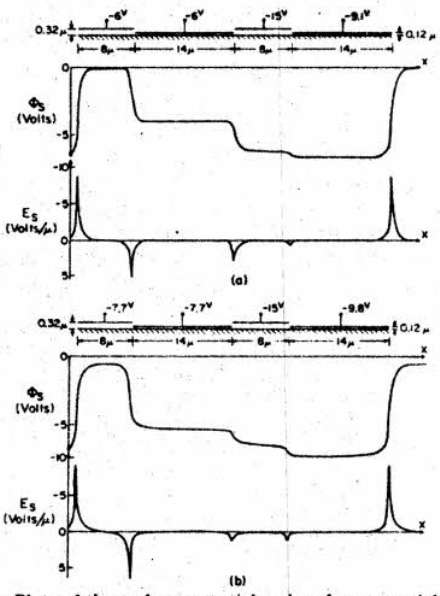

Fig. 2. Plots of the surface potential and surface potential gradient along the silicon-silicon oxide interface obtained from the solution of the two-dimensional Poisson equation of the structure in Fig. 1 with minimum geometry dimensions. $l_{s1} = 8$ μ, $l_{s1} = 14$ μ, $d_{s1} = 1200$ Å, $d_{s1} = 3200$ Å, $t_{s1} = 0.5$ μ, and $t_{s1} = 0.5$ μ. The electrode voltages correspond to the latter stages of the charge transfer, with a signal charge in the receiving storage gate. The substrate doping is 0.8×10^{15} donors/cm^3 in Fig. 2(a) and 10^{14} donors/cm^3 in Fig. 2(b).

by (12). When the device is operated with a circulating background charge or fat zero, the net charge trapped from the signal charge in interface states under the transfer gates is maximum when it is preceded by a fat zero and is given by

$$\Delta q_{tr} = \gamma e A_{tr} N_{ss} KT \cdot \left\{ \left[F_s \ln \frac{\left(\frac{1}{f_0} - t_{4tr_s}\right)}{\left(\frac{1}{mf_0} - t_{4tr_s}\right)} - F_0 \ln \frac{\left(\frac{1}{f_0} - t_{4tr_s}\right)}{\left(\frac{1}{mf_0} - t_{4tr_s}\right)} \right] + \frac{R}{\left(\frac{1}{mf_0} - t_{4tr}\right)} \left(\frac{F_0}{K_1 p_{av0}} - \frac{F_s}{K_1 p_{avs}} \right) \right\}, \tag{26}$$

where R is a fraction given by (20). p_{av0}, p_{avs} are the average mobile carrier concentration under the transfer gate during the interval Δt for a background charge and a signal charge, respectively. F_0, F_s are the filling probability as defined by (25) for a background charge and a signal charge, respectively. A_{tr} is the area under the transfer electrodes and t_{4tr_0}, t_{4tr_s} are the times at which the emptying of the interface states start for the background charge and the signal charge.

Two special cases are of interest. First, if the fill factors F_s and F_0 are less than one and unequal, then the first two

terms dominate. For $\gamma = 1$ and $t_{4,r} \approx t_{4,r-1}$, (26) reduces to

$$\Delta q_{t,r} = eA_{t,r}N_{ss}KT(F_s - F_0) \ln m \frac{(1 - f_0 t_{4,r})}{(1 - mf_0 t_{4,r})}.$$

For $f_0 t_{4,r} \ll 1$ and $m = 2$,

$$\Delta q_{t,r} = eA_{t,r}N_{ss}KT(F_s - F_0) \ln 2. \quad (27)$$

Second, if the fill factors are equal to one ($\Delta t/\tau_{eff} \gg 1$), then (26) reduces to

$$\Delta q_{t,r} = eA_{t,r}N_{ss}KT \cdot \left\{\frac{\delta(t_4)}{(t - t_{4,r})} R + \frac{R}{(t - t_{4,r})}\left(\frac{1}{K_1 p_{sv0}} - \frac{1}{K_1 p_{sv_s}}\right)\right\}.$$

For $f_0 t_4 \ll 1$, $m = 2$, $R \approx \frac{1}{2}$

$$\Delta q_{t,r} = eA_{t,r}N_{ss}KT\left\{f_0\,\delta(t_4) + f_0\left(\frac{1}{K_1 p_{sv0}} - \frac{1}{K_1 p_{sv_s}}\right)\right\}, \quad (28)$$

where $\delta(t_4)$ is the difference in the time t_4 at which the emptying of the interface states start for the signal charge and the background charge.

In the first case, the net charge trapped is almost frequency independent. While in the second case it increases almost linearly with frequency.

All the interface states under the transfer gate above an energy E_1 are filled with captured holes. E_1 is almost independent of the signal charge but depends on the clock frequency and is given by

$$E_1 = KT \ln K_2\left(\frac{1}{f_0} - t_4\right) \cong KT \ln \frac{K_2}{f_0}. \quad (29)$$

VII. Trapping in the Interface States Under the Edges of the Gates

Trapping in the interface states under the edges of the storage and transfer gates also add to the incomplete charge transfer [8]. Since the precise area covered by the charge being transferred at the interface depends upon the surface potential profiles under the gates which in turn depends on the surface charge density, the number of interface states at the edges that come in contact with the charge is dependent upon the amount of surface charge. The surface potential profile for a given surface charge density and sequence of potentials applied to the gate electrodes is obtained by solving the two dimensional Poisson equation for the CCD structure. Solutions [2], [9], [14] to this equation along and perpendicular to the active channel show that fringing fields penetrate under the edges of the gates for a distance of approximately a depletion layer thickness. The onset of these fringing fields define the spatial extent of the mobile charge. For fixed voltages applied to the gates, the depletion layer thickness and the penetration of fringing fields increase with decreasing surface charge. Hence a small surface charge is confined to a smaller area at the interface than a larger charge.

In the treatment of trapping and release of charge by these interface states, we must distinguish between the interface states at the gate edges parallel to the channel from those at the gate edges perpendicular to the channel.

In the case of the interface states at the edges perpendicular to the channel, the signal charge or the background charge flows over the interface states during every cycle. Thus the interface state can capture carrier from both the signal charge and background charge. Hence, the filling and emptying of these interface states is similar to that under the transfer gates.[4]

The net charge trapped from a signal charge in the interface state under the perpendicular edges when the device is operated with fat zeros is maximum when it is preceded by a fat zero. If the probability of filling of the interface states by the background charge is less than unity, then from (27)

$$\Delta q_{s,\perp} = eA_{s,\perp}N_{ss}KT(1 - F_0) \ln 2, \quad (30)$$

where $A_{s,\perp}$ is the area under the perpendicular edges and F_0 is the fill factor for the background charge defined by (25). In the case F_0 is almost equal to unity, then from (28)

$$\Delta q_{s,\perp} = eA_{s,\perp}N_{ss}KT\left\{f_0\,\delta(t_4) + f_0\left(\frac{1}{K_1 p_{sv0}} - \frac{1}{K_1 p_{sv\ edge}}\right)\right\}. \quad (31)$$

In the case of the interface states parallel to the edges we must distinguish between two clocking schemes, the drop clock and the push clock. With drop clocks the signal charge is stored below a gate at a holding voltage V_1 which is a fraction of the largest clock voltage V_m that the MOS structure can tolerate; charge transfer occurs when V_m is then applied to the adjacent gates, and the charge flows to the potential minimum thus created. With push clocks the charge is stored under a gate held at V_m, and transferred to a nearby gate, also at V_m, by raising the potential of the gate where the charge has been residing and thus "pushing" the charge to the next gate. Charge-coupled devices can be operated with two-phase, three-phase, or four-phase clocking schemes by push clocks, drop clocks, or a combination of push and drop clocks [2], [5], [15].

So with drop clocks, the charge transfer is effected by creating deeper potential wells under the next gates; and the background charge does not flow over the edges of the gates parallel to the channel. Thus the interface states under the parallel edges capture carriers from the signal charge but do not trap any carriers from the background charge; and the parallel edges are residual areas of the

[4] Note that in this case, since the signal charge remains under the storage electrode for one whole transfer time, the probability of filling the interface states by the signal charge F_s is equal to unity. As discussed in Section VI, we may also obtain the average mobile charge density under the edges $p_{sv\ edge}$ and p_{sv0} and the time interval Δt_{e0} for which the background charge is in contact with the edges from the charge transfer dynamics and the surface charge density profile of the signal charge under the electrodes.

active channel that the background change cannot reach. For example, after a signal charge is transferred from under the storage gate, the interface states under the parallel edges of this gate continue to emit the trapped carriers until the next signal charge passes, then the interface states fill again. The net charge trapped from the signal charge in the interface states under the parallel edges of the storage and transfer gates increases with increasing the number of fat zeros preceding it. This is unlike the net trapped charge in interface states under the storage gates, transfer gates, and the perpendicular edges that is almost independent of the number of fat zeros preceding the signal charge.

The net charge trapped in the interface states under the parallel edges increases logarithmically with the clock frequency (similar to the charge trapped when no fat zeros are used) [7]. For digital signals, the net trapped charge per transfer in the interface states under the parallel edges from the first "one bit" preceded by n_{zero} "zero bits" can be easily obtained from (12).

$$\Delta q_{ss} = eKT(N_{ss}A_{s\parallel} + N_{ss}F_sA_{t\parallel}) \cdot \ln\left[\left(\frac{n_{zero}+1/m}{f_0} - t_{s\parallel}\right)\Big/\left(\frac{1}{mf_0} - t_{s\parallel}\right)\right] \quad (32)$$

where $A_{s\parallel}$ and $A_{t\parallel}$ are the area of the edges parallel to the channel under the storage and transfer gates respectively. $t_{s\parallel}$ is the time at which the emptying of the interface states under the parallel edges start. For $f_0 t_{s\parallel} \ll 1$ and $m = 2$ (32) reduces to

$$\Delta q_{ss} = eKT(N_{ss}A_{s\parallel} + N_{ss}F_sA_{t\parallel}) \ln (2n_{zero} + 1). \quad (33)$$

In this case, all the interface states under the parallel edges above an energy E_1, where for $n_{zero} \gg 1$

$$E_1 \cong KT \ln K_2\left((n_{zero}+1)\frac{1}{f_0} - t_{s\parallel}\right), \quad (34)$$

are filled with the captured holes.

But with push clocks, the trapping effects under the parallel edges are reduced. The charge transfer characteristics and the charge profiles under the gates for the signal charge and the fat zero charge tend to be more similar with push clocks, [2], [5], [15]; hence the interaction of the traps with the mobile carriers of both charges is almost the same. For example, with the two-phase push clock, the charge transfer does not start until the surface potential under the storage gate is larger than that under the next transfer gate for both the fat zero charge and the signal charge. Hence the fat zero charge covers almost the same area covered by the signal charge at the interface under the storage gates before the charge transfer begins. Thus with push clocks, the behavior of most of the parallel edge area of the storage gates is similar to the behavior of the perpendicular edges and hence is described by (30) and (31). So the effective area of the parallel edges under the gates that interact with the mobile carriers according to (32) and (33) is much smaller with push clocks than with drop clocks.

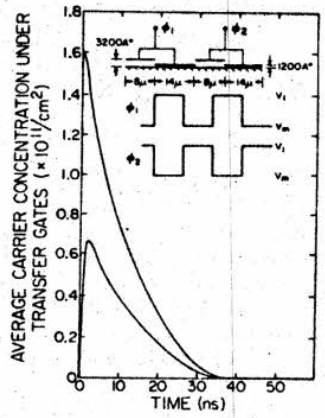

Fig. 3. Average carrier concentration under the transfer gates versus transfer time for the fat zero and signal charge. A two-phase drop clock with zero fall and rise time is used. $V_m = -15$ V, $V_i = -7$ V.

VIII. Numerical Results

When the device is operated with a circulating background charge the total net charge trapped from a large charge packet in interface states at each transfer is obtained by summing the different contributions obtained above:

$$\Delta q = \Delta q_{ss} + \Delta q_{st} + \Delta q_{s\perp} + \Delta q_{s\parallel}. \quad (35)$$

The same net charge Δq is emitted to the background charge by the interface states when it is preceded by a large signal charge. The influence of this incomplete charge transfer due to trapping in interface states on the signal degradation is best described by the signal degradation factor ϵ, defined by Berglund [16]:

$$\epsilon = \frac{\Delta q}{q_s - q_0} = \epsilon_{ss} + \epsilon_{st} + \epsilon_{s\perp} + \epsilon_{s\parallel}, \quad (36)$$

where q_s is the signal charge and q_0 is the background charge, so $q_s = eA_{st}p_s$ and $q_0 = eA_{st}p_0$. ϵ_{ss}, ϵ_{st}, $\epsilon_{s\perp}$, $\epsilon_{s\parallel}$ are the signal degradation factors due to trapping in interface states under the storage gate, transfer gate, and the perpendicular and parallel edges of the gates, respectively. p_s and p_0 are the mobile carrier densities for the signal charge and the background charge, respectively.

We have evaluated the relative magnitudes of the signal degradation factors for an overlapping gate charge-coupled device with dimensions consistent with typical layout tolerances of silicon gate technology. The storage polysilicon gates are 14 μ long and 8 μ apart. The channel width is 8 μ. The results in Figs. 3–6 are taken from a detailed numerical solution of the transport dynamics in p-channel devices with a substrate doping of 0.8 ×

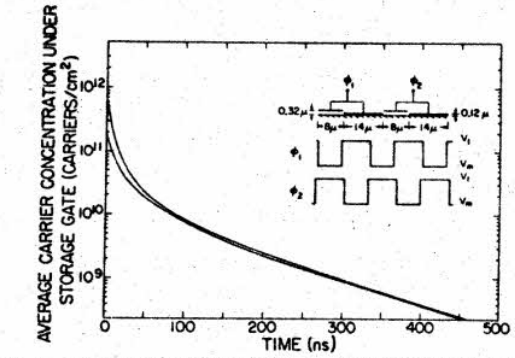

Fig. 4. Average carrier concentration under the storage gates versus transfer time for the fat zero and signal charge. A two-phase drop clock with zero fall and rise times is used. $V_m = -15$ V, $V_1 = -7$ V.

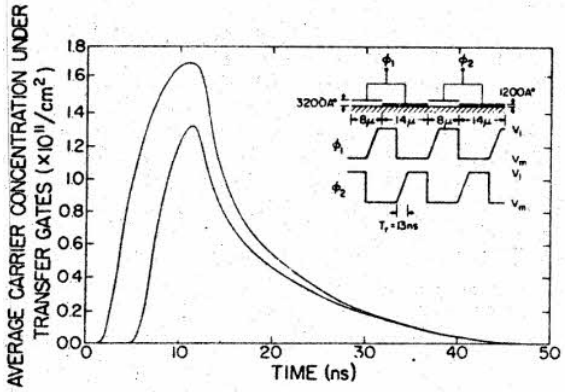

Fig. 5. Average carrier concentration under the transfer gates versus transfer time for the fat zero and signal charge. A two-phase push clock with zero fall time and 13-ns rise time is used. $V_m = -15$ V, $V_1 = -6$ V.

10^{15}/cm³ and minimum geometry dimensions operated in the complete charge transfer modes [2]. In Figs. 3 and 4 the average mobile carrier concentration under the storage and transfer gates is plotted versus time when a two-phase drop clock is used. The same plots for a two-phase push clock are shown in Figs. 5 and 6.

In Table I we have listed the values of the quantities used to evaluate the signal degradation from the previous equations. An average value of N_{ss} and σ_s was taken in agreement with the published values in the literature [11]–[13]. With a substrate doping of 0.8×10^{15}/cm³ and for the minimum geometry dimensions, fringing fields under the storage electrodes are negligible [1], [2], [14]. Hence the time constant of the exponential decrease of the residual carrier under the storage gate is the thermal diffusion time constant $\tau_d = l_{Si}^2/2.5D$. The time intervals Δt (which are the times the carriers spend under the transfer gates and the perpendicular edges) are taken from Figs. 3 and 5.

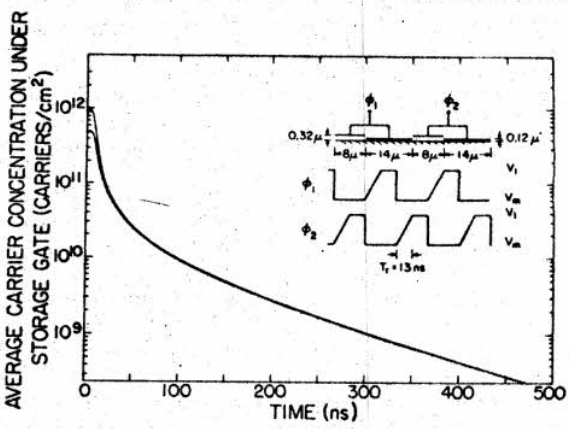

Fig. 6. Average carrier concentration under the storage gates versus transfer time for the fat zero and signal charge. A two-phase push clock is used. $T_r = 13$ ns, $V_m = -15$ V, and $V_1 = -6$ V.

Zero fall and rise time for the two-phase drop clock and zero fall time and 13-ns rise time for the two-phase push clock were used in the numerical simulation of the charge transfer characteristics shown in Figs. 3–6. For larger rise and fall times, the values of Δt are larger. The fill factors F_0 and F_s are then calculated using an average carrier density under the transfer gates during the time intervals Δt from Figs. 3 and 5. They are almost unity for the drop and push clocks. Hence 28 and 31 should be used to estimate $\Delta q_{t,r}$ and $\Delta q_{s,\perp}$. The value of n_{s,r_0} in (33) was taken as unity to give the minimum value of $\epsilon_{s,t}$. The ratio of the area of the edges to the storage gate area depends on the width of the channel W, the lengths of the storage and transfer gates, and the substrate doping concentration. The values of $A_{s,r,\parallel}/A_{s,t}$, $A_{t,r,\parallel}/A_{s,t}$, and $A_{s,\perp}/A_{s,t}$ are taken from surface potential plots of the solutions of the two-dimensional Poisson equation of the device similar to those in Fig. 2. With push clocks, the effective area of the parallel edges under the storage gates that interacts with the mobile carriers according to (32) and (33) was taken as one-tenth of the total parallel edge area under the storage gates. Actually a smaller value is expected because of the neutralization effect mentioned previously during the pushing of the charge.

In Table II we have listed the values of $\epsilon_{s,t}$, $\epsilon_{t,r}$, $\epsilon_{s,\perp}$, $\epsilon_{s,s}$, and ϵ for the drop and push two-phase clock at a frequency of 1 Mc for the minimum geometry device. In our calculations, we chose a suitable background charge to represent a fat zero ep_0 and a large charge to represent the signal charge ep_s as would be used, for example, to represent the zero and the one bit in a digital serial memory. In Figs. 7 and 8 we have plotted the signal degradation factor due to incomplete free charge transfer and due to trapping in interface state versus frequency. Several conclusions become apparent for this particular

TABLE I

Values of Parameters and Constants Used in the Calculation

$N_{ss} = 2 \times 10^{10}/cm^2 \cdot eV$
$\sigma_A = 10^{-15}\ cm^2$
$K_1 = 1/25\ cm^3/s$
$K_2 = 10^{11}\ s^{-1}$

$V_{th} = 10^7\ cm/s$
$d = 25\ Å$
$C_0 = 2.86 \times 10^{-8}\ F/cm^2$
$p(t_2) = 4.5 \times 10^9/cm^2$
$A_{s\perp}/A_{ss} = 0.156$

$t_2 \sim 150$ ns
$t_{ss} \sim 500$ ns
$\tau = 117$ ns
$A_{tr}/A_{ss} = 0.58$

Static Drop Clock

$p_s = 6.25 \times 10^{11}/cm^2$
$p_0 = 1.79 \times 10^{11}/cm^2$
$p_{avs} = 0.5 \times 10^{11}/cm^2$
$p_{av0} = 0.27 \times 10^{11}/cm^2$

$p_{av\ edge} = 1.57 \times 10^{11}/cm^2$
$\frac{p_s(t_4) - p_0(t_4)}{p_0(t_4)} = 1.75 \times 10^{-2}$
$\delta(t_4) = 6$ ns
$\Delta t_{tr} \cong 35$ ns
$\Delta t_{s0} \cong 7$ ns

$t_{str} \cong 35$ ns
$F_s = 1 - e^{-7\delta} = 1$
$F_0 = 1 - e^{-\delta 1} = 1$
$\left.\frac{A_{tres1} + A_{stst2}}{A_{ss}}\right|_{W=4\mu} = \frac{1}{10}$

Dynamic Push Clock

$p_s = 9.8 \times 10^{11}/cm^2$
$p_0 = 4.6 \times 10^{11}/cm^2$
$p_{avs} = 0.6 \times 10^{11}/cm^2$
$p_{av0} = 0.4 \times 10^{11}/cm^2$

$p_{av\ edge} = 2.45 \times 10^{11}/cm^2$
$\frac{p_s(t_4) - p_0(t_4)}{p_0(t_4)} = 1.75 \times 10^{-2}$
$\delta(t_4) = 1.5$ ns
$\Delta t_{trs} \cong 44$ ns

$\Delta t_{tr0} \cong 40$ ns
$t_{str} \cong 45$ ns
$F_s = 1 - e^{-11\delta} = 1$
$F_0 = 1 - e^{-7\delta} = 1$
$\Delta t_{s0} \cong 13$ ns

$\left.\frac{A_{tres1} + A_{stst2}|_{effective}}{A_{ss}}\right|_{W=4\mu} = \frac{1}{200}$

device. Trapping effects due to the interface states under the storage gate are larger than those under the transfer gate and under the perpendicular edges of the storage gate.[5] Trapping in interface states under the parallel edges of the gates is dominant at low frequencies. Also the incomplete charge transfer due to trapping in interface states when the device is operated with push clock is much less than when it is operated with drop clock. At low clock frequencies the signal degradation due to trapping interface states is larger than that due to incomplete free charge transfer. But at high frequency, the device performance is limited by the free charge transfer process.

It should be emphasized that the results shown in Figs. 7 and 8 are for a minimum geometry overlapping gate charge-coupled devices under a specific set of operation conditions. The specific values of the signal degradation due to trapping in interface states depend on the device geometry and the operating conditions. So care should be taken in extrapolating the specific values of the signal degradation factors in Figs. 7 and 8 to other CCD structures with other dimensions under other operating conditions. The equations derived in the previous sections should be used with the device and model parameters appropriate to each case.

[5] This is actually due to the following reasons. First, for a sufficiently large background charge, the mobile carriers during the first stages of the charge transfer process effectively equilibrate with the interface states under the transfer gates and the perpendicular edges. Second the area under the transfer gates and the perpendicular edges in the overlapping gate structure is usually smaller than the area under the storage gates. Third, because of the larger fringing fields under the transfer gates and the perpendicular edges, the mobile carriers are swept out very rapidly and the emptying of the interface state begin earlier in the transfer process. But under the storage gate the residual charge decreases with a relatively large time constant. The interface states under it continue to capture carriers from the residual charge and the quasi-Fermi level follows the quasi-Fermi level of the residual charge. When the residual charge becomes small enough, emission from the traps becomes dominant. This results in a change of the slope of the signal degradation due to trapping in interface states under the storage gates versus clock frequency as shown in Figs. 7 and 8.

IX. Discussion

The analysis and results given in the previous sections reveal some important and general features of the incomplete charge transfer due to trapping in interface states in charge-coupled devices. In this section we discuss some of these important features, such as the relative contribution to the signal degradation of the interface states under the storage and transfer gates and their edges; the influence of clocking waveforms and voltages, device dimensions, and parameters on the incomplete charge transfer due to trapping in interface states, and design features of CCD structures to reduce it.

When charge-coupled devices are operated with fat zeros, trapping in interface states under the edges of the gates parallel to the channel is the dominant effect at low frequencies. The parallel edges are the areas parallel to the channel at the interface under the storage and transfer gates that are covered by the signal charge and are not covered by the background charge. The interface states under the parallel edges capture charge from the signal charge only. The resulting signal degradation is almost frequency independent, varies inversely with the channel width, and depends on the information content of the signal. At low frequency the signal degradation due to trapping in the interface states under the storage gates, the transfer gates, and the perpendicular edges is relatively smaller. These interface states capture charge from both the signal charge and the background charge.

TABLE II
NUMERICAL VALUES OF SIGNAL DEGRADATION FACTORS FOR A P-CHANNEL MINIMUM GEOMETRY TWO-PHASE CCD AT 1-Mc CLOCK FREQUENCY

Signal Degradation Factor Due to Trapping in Interface States Under:	Equation	Value for Drop Clock	Value for Push Clock
Storage gate ϵ_{st}	(16)	8.4×10^{-3}	1.7×10^{-3}
Transfer gate $\epsilon_{t,}$	(28)	3.62×10^{-4}	0.975×10^{-4}
Perpendicular edges $\epsilon_{s\perp}$	(31)	1.33×10^{-6}	0.464×10^{-6}
Parallel edges $\epsilon_{s\parallel}$	(33)	1.64×10^{-4}	7.0×10^{-6}
Total ϵ	(36)	2.53×10^{-4}	3.54×10^{-3}

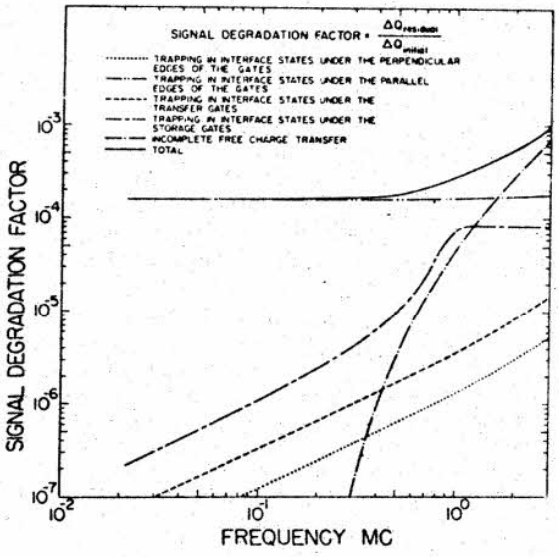

Fig. 7. Signal degradation factors versus clock frequency for the minimum geometry device operated with a two-phase drop clock.

Hence the background charge is effective in reducing the effect of trapping in these interface states on the incomplete charge transfer. For a sufficiently large background charge the effective time constant of the interface states is typically a fraction of a nanosecond. With the finite rise and fall times obtained with the practical clock drivers, and for the minimum geometry CCD devices we have considered, these interface states can equilibrate with both the signal charge and background charge. This leads to a small signal degradation that is directly proportional to frequency.

From the equations derived in Sections V–VII, and [2], [5], [15], we may conclude that increasing the clock voltage amplitude and the signal charge reduces the incomplete transfer due to trapping in interface states and the incomplete free charge transfer. Clocking waveforms that tend to reduce the incomplete free charge transfer by making the charge transfer for large and small charge similar will also reduce the incomplete charge

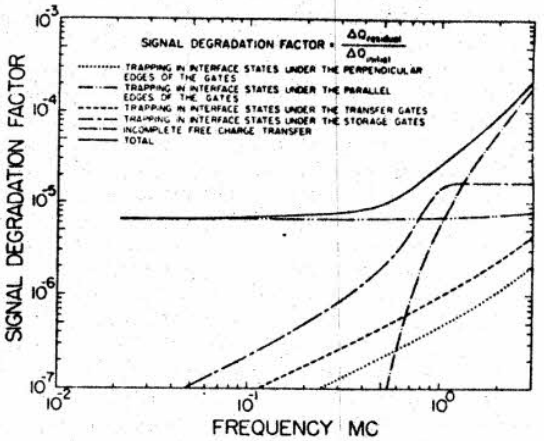

Fig. 8. Signal degradation factors versus clock frequency for the minimum geometry device operated with a two-phase push clock.

transfer due to trapping in interface states because the effective parallel edge area is reduced and the charges under the storage and transfer gates, and the time at which emptying of the interface states begins tend to be less dependent on the initial charge. For example, when the device is operated with a two-phase push clock, the incomplete charge transfer due to the interface state is reduced by over an order of magnitude over that when it is operated with a drop clock. If the device is operated in the complete charge transfer mode the other details of the clocking waveforms such as its rise time and waveshape affect mainly the time interval Δt the charge spends under the transfer gate and the time t_4 at which the interface states starts to empty. For example, if the rise time increases, Δt and t_4 increase and the signal degradation $\epsilon_{s,}$ due to the interface states under the storage gates increases slightly. The signal degradation due to interface states under the transfer gates and the perpendicular edges $\epsilon_{t,}$ and $\epsilon_{s\perp}$ also increase very slightly if $\Delta t/\tau_{e,t} \gg 1$, but decrease if the fill factor F_s and F_0 are less than unity.

Certain design features of CCD structures may reduce the incomplete charge transfer due to the interface states. A wide active channel increases the signal charge relative to the net charge trapped in the parallel edges and hence reduces the signal degradation factor at low frequencies.[6] Thinner oxide over the active channel increases the oxide capacity and the signal charge density. Thus, the net charge trapped under the storage gates, transfer gates,

[6] Increasing the active channel width increases also the SNR and dynamic range of the CCD. The noise introduced to the signal charge in the storage process through the leakage and thermal generation current is proportional to the square root of the gates' area. The noise introduced during the transfer process through the fluctuations of the carriers trapped in the interface states and through suppressed transfer loss fluctuations is also proportional to the square root of the gates' area [17], [18]. But the signal charge is directly proportional to the gate area. Hence the dynamic range and SNR can be increased by increasing the active channel width of the device without degrading its high-frequency performance.

and the perpendicular edges decreases, and the area of the edges is reduced. A higher substrate doping reduces the edges' area, but also reduces the fringing fields under the storage gates and hence decreases the rate of free charge transfer. A structure with a high substrate doping (or channel stop diffusion) and a low doping under the active channel reduces the parallel edge area and increases the fringing fields at the same time. The large fringing fields reduce the incomplete free charge transfer at high frequency. The net charge trapped under the transfer and storage gates is also reduced as the interface states start to empty earlier in the transfer process. The perpendicular edge area is increased in this structure, but since in the overlapping gate CCD the effect of the perpendicular edges is relatively small, the overall effect of interface states on incomplete transfer is reduced at low frequencies. Such a structure can be easily achieved with ion implantation or otherwise. Reduction of the signal degradation due to trapping in interface states also can be achieved by decreasing the interface state density N_{ss}, for example, by using the (100) instead of the (111) substrate. Moving the charge pockets in potential wells in the bulk rather than at the interface as in buried channel CCD [19] eliminates the incomplete charge transfer and fluctuation noise due to trapping of the signal charge in the interface states. Since trapping in the defect states of the buried channel is expected to be much smaller than interface state trapping, the signal degradation in buried channel charge-coupled devices is much smaller than in surface channel CCD.

The signal degradation due to trapping in interface states limits the performance of CCD devices at low frequency, but at high frequency the signal degradation due to incomplete free charge transfer is dominant. According to the simple model we have considered, the capture cross section σ_h and the interface state density N_{ss} were taken constant for simplicity. Actually the variation of N_{ss} and σ_h with energy will change the frequency dependence of the signal degradation due to trapping in interface states from that plotted in Figs. 7 and 8. However, the frequency dependence of the signal degradation factor due to the interface states will still be weaker than that due to incomplete free charge transfer. The latter changes very rapidly with frequency, for example, in Fig. 8 it changes by more than four orders of magnitude over only one decade of frequency.

So far, we have assumed that the background charge and the signal charge are sufficiently large so that the interface states under the transfer gates and the perpendicular edges can effectively equilibrate with the mobile carriers. However, if the background charge, or the capture cross section σ_h, or the time interval Δt the carriers spend under the transfer gates and the perpendicular edges is too small, then these interface states cannot equilibrate with the mobile carriers in transit. The fill factors F_s and F_0 are thus less than unity, and the first two terms in (26) dominate at sufficiently low frequency. In this case the contribution to the signal degradation from the interface states under the perpendicular edges and the transfer gates tends to a constant value at low frequency given by (27) and (30). This contribution is due to the difference in the filling probabilities of the interface states for the background charge and the signal charge. The contribution to the signal degradation from the interface states under the parallel edges and the storage gates increase also by decreasing the background charge. However, the trapping in the interface states under the parallel edges still remains the dominant effect especially from minimum geometry devices.

If the storage and transfer gate lengths are reduced, the time interval Δt that the charge spends under the transfer gate decreases and the relative area of the perpendicular edges increases. Also the time t_s at which the emptying of the interface states starts decreases. Thus $\epsilon_{s\parallel}$ slightly decreases but $\epsilon_{s\perp}$ increases, $\epsilon_{s\perp}$ decreases very slightly in the case $\Delta t/\tau_{s\perp} \gg 1$, but increases considerably if the filling probabilities F_s and F_0 are less than unity. The signal degradation due to the parallel edges $\epsilon_{s\parallel}$, which is the dominant effect, also decreases very slightly.

The interface states under the storage gates, the transfer gates, and the perpendicular edges can capture carriers every cycle from the signal charge and the fat zero charge. Hence the interface states with energy levels above E_1 [given by (18), (22), (29), and (34)] do not get a chance to reemit the captured carriers and are filled all the time. The interface states with energy between the valence band edge and the energy E_1 will be emptying and filling every cycle.[7] For example, for digital signals, the net trapped charge from the first "one bit" in the interface states under the storage and transfer gates and the perpendicular edges is almost independent of the number of preceding "zero bits." But the net trapped charge from the first one bit in the interface states under the parallel edges increases logarithmically with the number of preceding zero bits. If a two-phase device is operated with no fat zeros, then the net trapped charge per transfer from the first one bit preceded by n_{zero} zero bits can be easily obtained from (12).

$$\Delta q = eA_{s\parallel}KTN_{ss}\ln\left(\frac{n_{zero}+1/2}{f_0}-t_{s\parallel}\right)\Big/\left(\frac{1}{2f_0}t_{s\parallel}\right)$$
$$+eA_{s\perp}KTN_{ss}P_s\ln\left(\frac{n_{zero}+1/2}{f_0}-t_{s\perp}\right)\Big/\left(\frac{1}{2f_0}-t_{s\perp}\right)$$
$$+eA_sKTN_{ss}\ln\left(\frac{n_{zero}+1/2}{f_0}-t_{s\perp}\right)\Big/\left(\frac{1}{2f_0}-t_s\right)$$

and for $t_{s\parallel} < 1/2f_0$ and $t_{s\perp} \ll 1/2f_0$

$$\Delta q = eKTN_{ss}(A_{s\perp}+A_{s\parallel}F_s+A_s)\ln(2n_{zero}+1). \quad (37)$$

[7] Thus the incomplete charge transfer due to trapping in interface states under the storage and transfer gates and the perpendicular edges is due to the variable mean occupation of the state with energy close to E_1. Therefore the values of N_{ss} and σ_h at the energy E_1 should be used to estimate the trapping effects in these states.

where $E_c(x)$ is the exponential integral of order c defined by

$$E_c = \int_1^\infty \frac{\exp(-xv)}{} \, dv \qquad \text{(A4)}$$

and

$$p_{tr} = N_{ss}KT[E_1(K_2(t-t_4)\exp(-E_s/KT)) - E_1[K_2(t-t_4)] - E_1(K_2(t-t_4)\exp(-E_s/KT) + K_1(t-t_4)p(t_4)) + E_1(K_2(t-t_4) + K_1(t-t_4)p(t_4))].$$

$$c = \tau K_2 \exp(-E/KT). \qquad \text{(A5)}$$

If $K_1\tau p(t) > 1$, then the asymptotic expansion of $E_c(x)$ can be used:

$$E_c(x) = \frac{e^{-x}}{x+c}. \qquad \text{(A6)}$$

For $t > t_3 + [1/K_1p(t_3)]$, (A3) reduces to

$$n_{ss}(t) = \frac{N_{ss}}{1 + \frac{K_2\exp(-E/KT)}{K_1p(t)}} + \frac{N_{ss}}{1 + \frac{K_2\exp(-E/KT)}{K_1p(t_3)}} \cdot \exp[-K_1p(t_3)\tau(1 - \exp(-(t-t_3)/\tau)) - K_2\cdot(t-t_3)\exp(-E/KT)]. \qquad \text{(A7)}$$

Two special cases are of interest. First, if $K_1p(t_3)\tau > 1$, then the second term is negligible for $t > t_3 + \tau$, and (A7) reduces to

$$n_{ss}(t) = \frac{N_{ss}}{1 + \frac{K_2\exp(-E/KT)}{K_1p(t)}}. \qquad \text{(A8)}$$

Thus the interface states have a small effective time constant τ_{eff} and can equilibrate very rapidly with the mobile carrier. Assuming a constant interface state density N_{ss} states/cm^2·eV and a constant capture cross section σ_h cm^2, the total density of trapped carriers p_{tr} is given by

$$p_{tr} = \int_0^{E_s} n_{ss}(t)\,dE = N_{ss}KT \ln \frac{\left[\exp(E_s/KT) + \frac{K_2}{K_1p(t)}\right]}{\left[1 + \frac{K_2}{K_1p(t)}\right]}.$$

If $1/K_2 < [1/K_1p(t)] < 1/K_2\exp(E_s/KT)$, then

$$p_{tr} = N_{ss}\left(E_s - KT\ln\frac{K_2}{K_1p(t)}\right). \qquad \text{(A9)}$$

Second, if $K_1p(t)\tau \leq 1$, (A7) reduces to

$$n_{ss} = \frac{N_{ss}}{1 + \frac{K_2\exp(-E/KT)}{K_1p(t_4)}} \cdot \exp[-K_2(t-t_4)]\exp(-E/KT) \qquad t > t_4, \qquad \text{(A10)}$$

where t_4 is the time the emission of carriers becomes dominant and the refilling of the traps becomes negligible. It is given by

$$K_1p(t_4)\tau = 1. \qquad \text{(A11)}$$

Similarly integrating (A10), we get

If $1/K_2 < t - t_4 < 1/K_2\exp(E_s/KT)$ and $t - t_4 > [1/K_1p(t_4)]$, then we may use the asymptotic expansion of the exponential integral for small and large arguments to get

$$p_{tr} = N_{ss}\left[E_s - KT\ln K_2(t-t_4) - \frac{KT}{(t-t_4)K_1p(t_4)}\right]. \qquad \text{(A12)}$$

References

[1] A. M. Mohsen, T. C. McGill, and C. A. Mead, "Charge transfer in charge-coupled devices," in *ISSCC Dig. Tech. Papers*, Feb. 1972, pp. 248–249.

[2] ——, "Charge transfer in overlapping gates charge-coupled devices," *IEEE J. Solid-State Circuits*, vol. SC-8, June 1973, to be published.

[3] J. E. Carnes, W. F. Kosonocky, and E. G. Ramberg, "Free charge transfer in charge-coupled devices," *IEEE Trans. Electron Devices*, vol. ED-19, pp. 798–808, June 1972.

[4] C. N. Berglund and R. J. Strain, "Fabrication and performance consideration on charge-transfer dynamic shift registers," *Bell Syst. Tech. J.*, vol. 51, pp. 655–703, 1972.

[5] A. M. Mohsen, T. C. McGill, and C. A. Mead, "The influence of clocking waveform on CCD operation," presented at the IEEE Electron Devices Meeting, Edmonton, Alta., Canada, June 1972, to be published.

[6] J. R. Strain, "Power and surface state loss analysis of charge-coupled devices," presented at the IEEE Electron Devices Meeting, Washington, D. C., Oct. 1970.

[7] J. E. Carnes and W. F. Kosonocky, "Fast interface state losses in charge-coupled devices," *Appl. Phys. Lett.*, vol. 20, p. 261, 1972.

[8] M. F. Tompsett, "Effect of charge trapping on transfer efficiency and signal-to-noise ratio in surface charge-coupled devices," presented at the IEEE Electron Devices Meeting, Edmonton, Alta., Canada, June 1972.

[9] W. F. Kosonocky and J. E. Carnes, "Charge-coupled digital circuits," *IEEE J. Solid-State Circuits*, vol. SC-6, pp. 314–326, Oct. 1971.

[10] W. Shockley and W. T. Read, "Statistics of recombination of holes and electrons," *Phys. Rev.*, vol. 87, p. 835, 1952.

[11] E. H. Nicollian and A. Goetzberger, "MOS conductance technique for measuring surface state parameters," *Appl. Phys. Lett.*, vol. 7, p. 216, 1965.

[12] ——, *Bell Syst., Tech. J.*, vol. 46, p. 1055, 1967.

[13] E. Denling, E. Klausmann, and A. Goetzberger, *Solid-State Electron.*, vol. 15, p. 559, 1972.

[14] Y. Daimon, A. M. Mohsen, T. C. McGill, and C. A. Mead, to be published.

[15] A. M. Mohsen, T. C. McGill, M. Anthony, and C. A. Mead, "Push clock: A new approach to charge-coupled device clocking," *Appl. Phys. Lett.*, vol. 22, Feb. 15, 1973.

[16] C. N. Berglund, "Analog performance limitations of charge-transfer dynamic shift registers," *IEEE J. Solid-State Circuits*, vol. SC-6, pp. 391–394, Dec. 1971.
[17] K. K. Thornber, "Noise suppression in charge transfer devices," *Proc. IEEE* (Lett.), vol. 60, pp. 1113–1114, Sept. 1972.
[18] J. E. Carnes and W. F. Kosonocky, "Noise sources in charge-coupled devices," *RCA Rev.*, vol. 33, pp. 327–343, June 1972.

[19] R. H. Walden *et al.*, "The buried channel charge-coupled device," *Bell Syst. Tech. J.*, pp. 1635–1640, Sept. 1972.
[20] W. F. Kosonocky and J. E. Carnes, "Two-phase charge-coupled shift registers," in *ISSCC Dig. Tech. Papers*, 1972, p. 132.
[21] P. A. Levine, "Measurements of CCD transfer efficiency by use of feedback to increase the effective number of transfers," this issue, pp. 104–108.