

2026年9月15日(火) 開催 DAFSユニバーシティ委員会主催

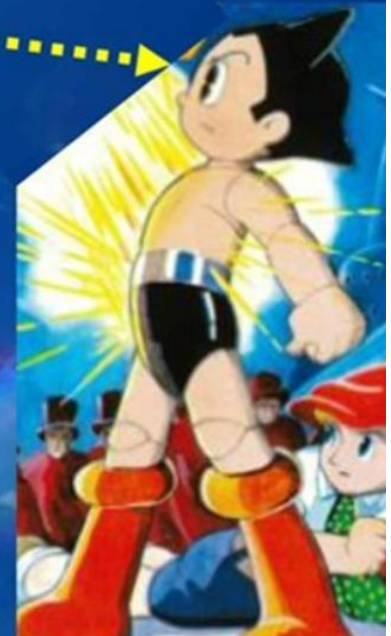
『AIロボティクスセミナー』

人工知能搭載AIロボットに不可欠な半導体部品の紹介

半導体産業人協会（SSIS）教育委員会委員 萩原良昭 講師

鉄腕アトムは半導体部品で構成され創られています。
鉄腕アトムの賢い電子の目は太陽の光を吸収して
光エネルギーを電気エネルギーに変換します。
鉄腕アトムの賢い電子の目は太陽電池でもあります。
賢い電子の目は半導体で造られます。

半導体とは？



[2026_09_15_DAFSユニバーシティ_Slides_講師_SSIS_教育委員会_萩原良昭.pdf](#)

[2026_09_15_DAFSユニバーシティ_Slides_講師_SSIS_教育委員会_萩原良昭.mp4](#)

宮本 武蔵



宮本武蔵肖像

(島田美術館蔵。熊本県指定文化財)

宮本武蔵といえば二刀流と考えられがちだが、必ずしも二刀にこだわることを主張しているわけではなく、『五輪書』では多数の敵や立てこもる敵と戦う時に二刀が良いことや、実戦では両手で太刀を扱えない場面が多いので片手で太刀を振るのに慣れておくべきこと、さらに命を賭けた戦いでは持っている道具を余すことなく役立てるべきことが述べられている

- ソフトとハードの両刀使いのできる技術者
- 経営学と生産工学の両方を基礎に持つ経営者
- あらゆる可能性を見逃さず探求する経営者と技術者の熱意と連携が事業の成功の鍵となる。

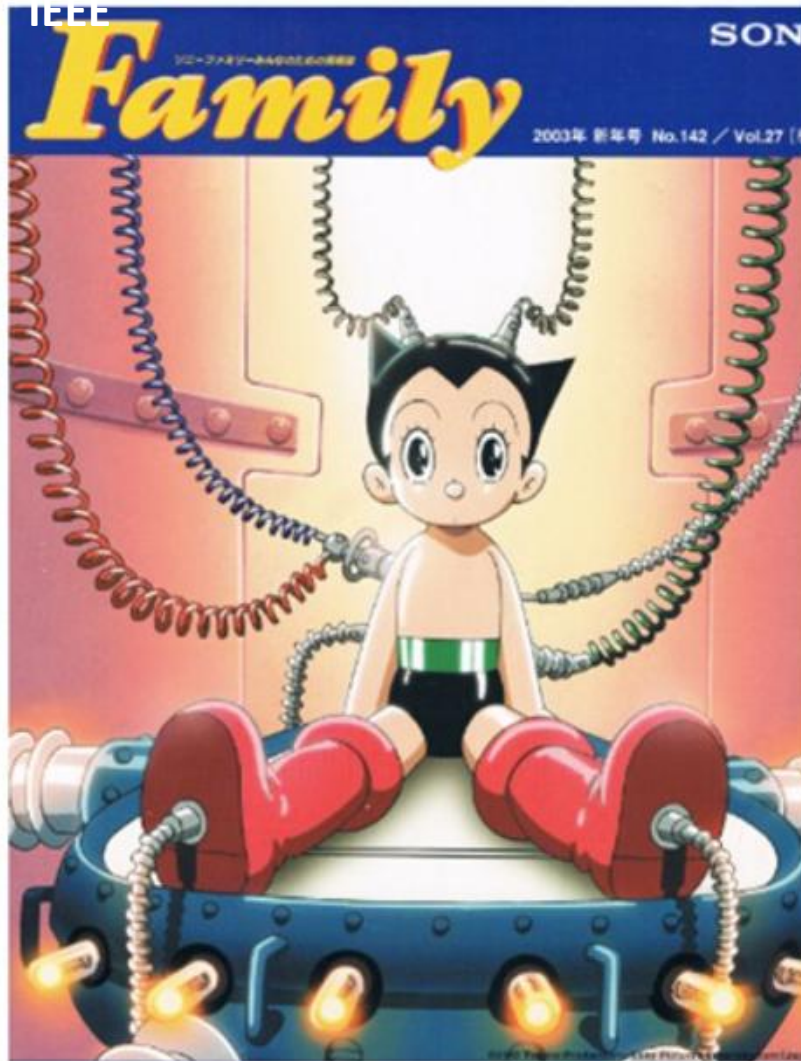
半導体産業人協会 教育委員会 もと委員長
合同会社 LOCOMTEC 萩原AIPS研究所 所長

萩原良昭 (旧姓大門)

Yoshiaki Daimon Hagiwara
PhD, IEEE Life Fellow, AAIS Fellow,
Armermia State High Technology Award Laureate 2024

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<http://www.aiplab.com/> hagiwara@aiplab.com
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<https://www.sojo-u.ac.jp/> hagiwara@ofc.sojo-u.ac.jp
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Introduction to AIPS



Sony Family Journal 2003 January Issue, No.142/Vol.27

Yoshiaki Hagiwara was born on July 4, 1948 in Kyoto Japan. Graduated from Murasaki-no Elementary School in 1958. Lady Murasaki Shikibu is very famous as the writer of the story of Genji. Graduated from Rakusei Middle High School in 1961. Moved to Riverside-city in California USA in 1965 and graduated from Riverside City Polytechnique High School in 1967. Lived in Pasadena California since 1967 and received BS1971, MS1972 and PhD1975 in Electrical Engineering and Physics from California Institute of Technology (Caltech) . Joined Sony on February 1975 till July 2008. Taught at Sojo University as a professor till 2017. He is now serving for the ssis.or.jp.

Semiconductor Company President Award 1999



Newspaper describing Sony Victory on Sony-Fairchild Patent War

SONY- Fairchild Patent War (1991-2000) on Pinned Photo Diode with Vertical OFD





1980年7月1日

東京でビデオムービーを発表する岩間(左)

SONY 半導体の黎明期の人々



塚本哲男
(つかもと てつお)

- 1922年(大正11年) 生 (台湾)
- 1944年(昭和19年) 大阪帝国大学理学部物理学科卒業
- 1946年(昭和21年) 東京通信工業に入社。
- 1954年(昭和29年) トランジスタラジオ用グローントランジスタの結晶製造を担当。
- 1964年(昭和39年) ソニー厚木工場副長。
- 1971年(昭和46年) ソニー中央研究所副所長
- 1976年(昭和51年) ソニー学園湘北短期大学学長
- 2000年(昭和55年) ソニーを定年退職

塚本哲男 <https://www.shmj.or.jp/museum2010/exhibi612.htm>

「ゲルマニウムグローン型トランジスタのリン導入の経過説明」

東京通信工業は昭和29年4月岩間和男が米国から帰ってトランジスタラジオに向けての高周波用トランジスタをグローン型でやることを決定。塚本哲夫はその担当となった。結晶引き上げ装置が設計製作され、直ちにトランジスタの生産が始まった。そして昭和30年8月にはトランジスタラジオTR55が発売された。

しかし、局部発振用のトランジスタの収率は悪く、ラジオは順調に生産販売が伸びても半導体は収率改善のために苦しんだ。塚本哲夫はエミッタ材料として5属で一番原子番号の小さいリンを使ってみようとして実験を試みた。出来上がったトランジスタは素晴らしい出来栄で高周波特性もその歩留まりも良かった。これはゲルマニウム中のリンの拡散係数がアンチモンよりずっと低いことによっていた。

これで行こうと生産を切り替えたが、今度は歩留まり悪が続き、会社は苦境に立たされた。塚本哲夫は江崎玲於奈にトランジスタの調査を依頼し、江崎玲於奈はPN接合の順方向トンネル現象を発見した。同時にこの問題の解決法はリンの濃度の適正化であることが分かった。塚本哲夫はそのためにインジウムリンという化合物半導体を溶融ゲルマニウムに投入することを思い立ち実験が成功した。インジウムは偏析によってトランジスタ部分には入らないのであった。投入するインジウムリンの正確な評量が鍵であった。これは昭和32年春のことで、ソニーはトランジスタラジオで優位に立つことが出来た。



井深 大



岩間 和夫



江崎 玲於奈



Carver Mead

2022 Kyoto Prize Laureates
Carver Mead

Gordon and Betty Moore Professor of Engineering and Applied Science, Emeritus, (

**Computers That
Put the Power
Where It Belongs**

by Carver Mead



Prof. C.A. Mead with his student, Yoshiaki Daimon Hagiwara in September 1971.

【京都賞記念講演】カーヴァー・ミード「情報革命の時代を生きて」

<https://ieeexplore.ieee.org/document/1050799>

128-bit multicomparator

[C.A. Mead](#) ; [R.D. Pashley](#) ; [L.D. Britton](#) ; [Y.T. Daimon](#) ; [S.F. Sando](#)

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976

Abstract:

A 128-bit multicomparator was designed to perform the search-sort function on arbitrary length data strings. Devices can be cascaded for longer block lengths or paralleled for bit-parallel, word-serial applications. The circuit utilizes a 3-phase static-dynamic shift register cell for data handling and a unique gated EXCLUSIVE-NOR circuit to accomplish the compare function. The compare operation is performed bit parallel between a 'data' register and a 'key' register with a third 'mask' register containing DON'T CARE bits that disable the comparator. The multicomparator was fabricated using p-channel silicon-gate metal-oxide-semiconductor (MOS) technology on a 107/spl times/150 mil chip containing 3350 devices. With transistor-transistor logic (TTL) input, data rates in excess of 2 MHz have been attained. The average power dissipation was 250 mW in the dynamic mode and 300 mW in the static mode.

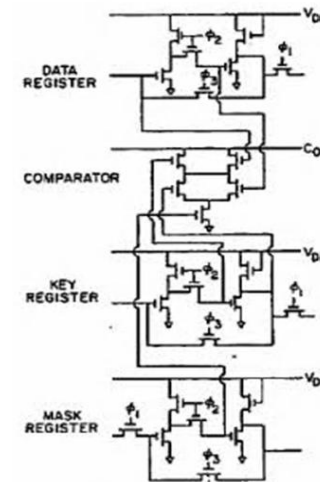


Fig. 5. Full schematic of one bit slice of the multicomparator.

<https://ieeexplore.ieee.org/document/1050799>

128-bit multicomparator

C.A. Mead ; R.D. Pashley ; L.D. Britton ; Y.T. Daimon ; S.F. Sando

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976

Designed by Caltech Student (Hagiwara) with Intel E-D MOS Technology, 1972.

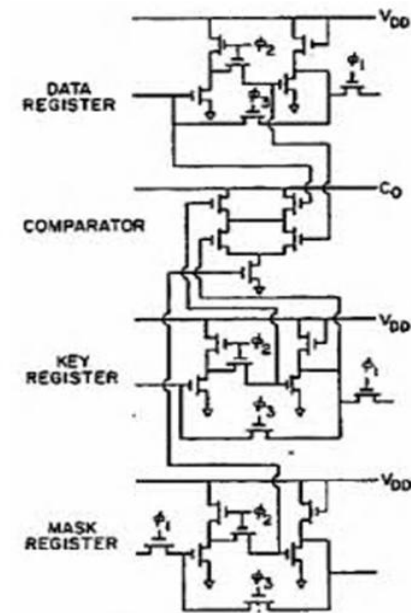
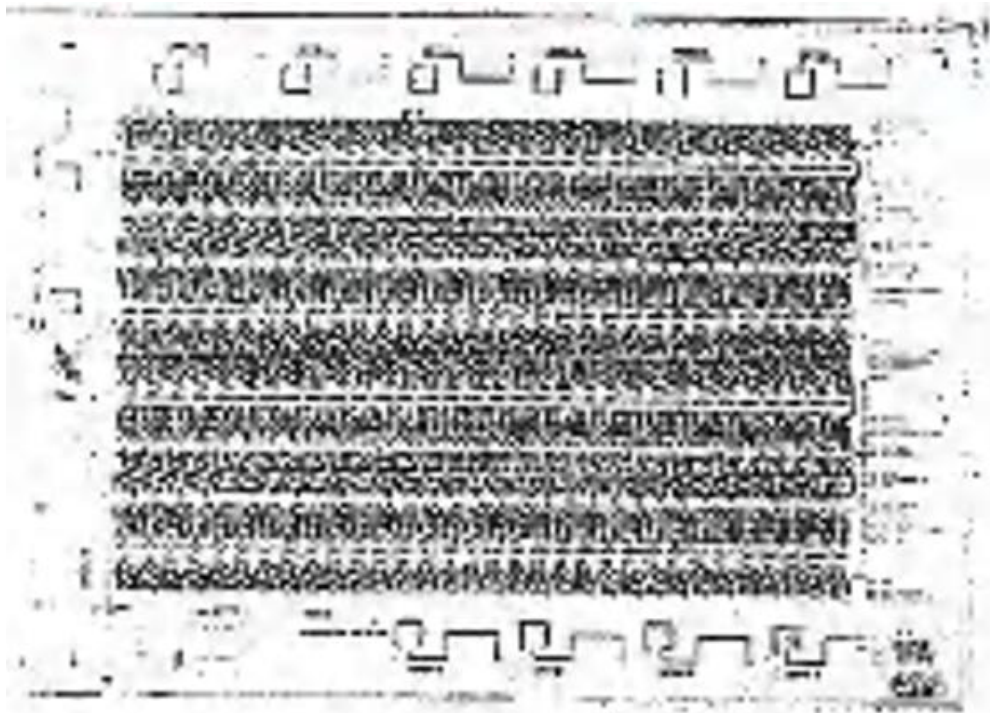


Fig. 5. Full schematic of one bit slice of the multicomparator.

<https://www.elspub.com/pdf/doi/10.55092/20250003>

Past, Presence and Future Applications of Buried-channel Double-junction Sony Hole Accumulation Diode (HAD) type Image Sensors and Solar Cells with Pinned Surface and Empty Potential Well.

May 23-25, 2025

Yoshiaki Daimon Hagiwara

2. Multi-chip 3DIC back-light illuminated CMOS image sensor for real-time AI robot vision

128-bit Comparator Block

one-bit Comparator Element Block

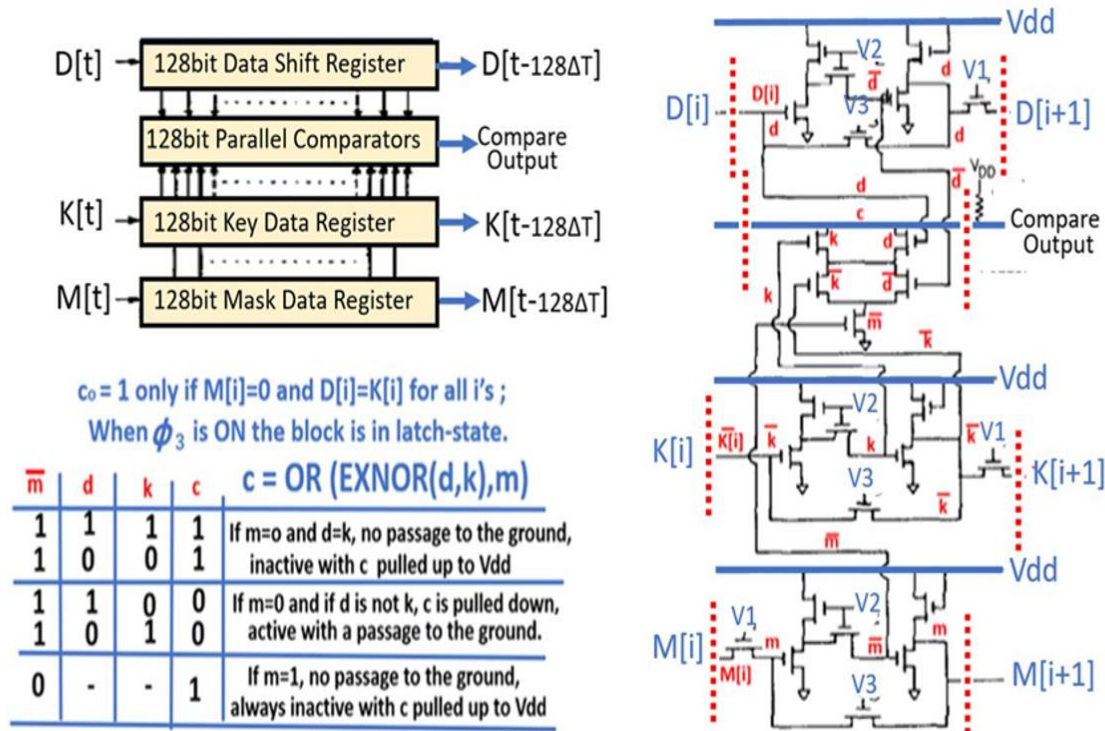


Figure 3. Full schematics of one bit slice of a new 128-bit multi-comparator for AI robot vision.

Introduction to Semiconductor Device

IEEE

[Caltech 1975 PhD Thesis by Yoshiaki Daimon Hagihara.pdf](#)

P.96

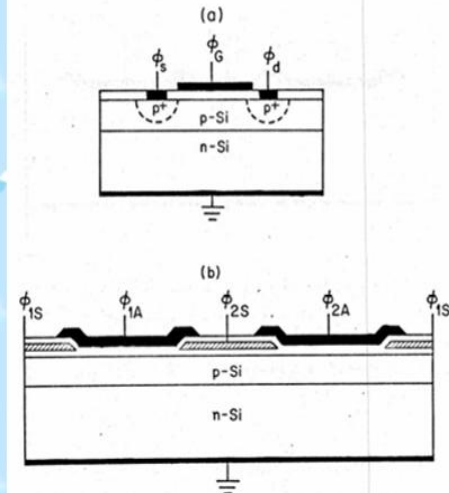


Fig. 4.1a The structure of a surface field effect transistor with a metallurgical channel. The channel is p-type, epitaxially grown.
Fig. 4.1b One unit cell of overlapping gate buried channel CCD.

P.106

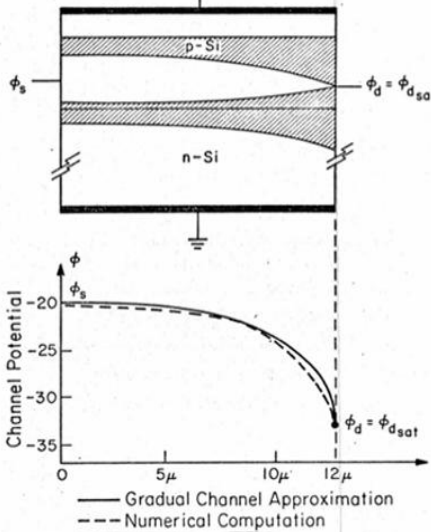


Fig. 4.2a The ideal condition at the onset of saturation is illustrated. $\phi_d = \phi_{d_{sat}} \approx -32.8$ volt and $\phi_s \approx -20$ volt.
Fig. 4.2b The channel potentials computed by the gradual channel approximation and the numerical computation are compared. The gate length L is 12 μ . $\phi_{SF} \approx -10$ volt.

P.108

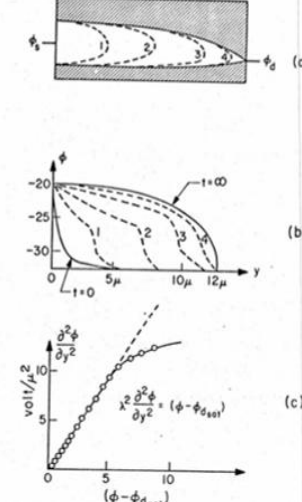


Fig. 4.3a The boundary of the channel at the transition period when the drain voltage changes suddenly from ϕ_s to $\phi_{d_{sat}}$.
Fig. 4.3b The channel potential at transit times. The profiles at $t=0$ and $t=\infty$ are calculated exactly.
Fig. 4.3c The curvature of the channel potential.

Surface-channel type Charge Coupled Device(SCCD) has only 99.9 % charge transfer Efficiency while Buried-channel type Charge Coupled Device(BCCD) has 99.999 % charge transfer efficiency and was as useful for 800H x 500V TV format. But CCD is not applicable because 99.999% efficiency is good enough for 6000H x 4000V HDTV.

Introduction to Semiconductor Device

IEEE

[Caltech 1975 PhD Thesis by Yoshiaki Daimon Hagihara.pdf](#)

Gaussian Impurity doping profile by the newly developed ion implantation technology used actually in the (t, x, y) numerical device analysis.

The (t, x, y) numerical device analysis of Buried Channel CCD Dynamic Charge Packet and two-dimensional Potential Profile.

Charge Transfer in Charge Coupled Devices
Thesis by Yoshiaki Daimon-Hagihara
California Institute of Technology
February 16, 1975

**IBM360 Main Frame Computer
programmed by FORTRAN Coding
using PUNCH-CARD,
in 1970-1974 in Caltech.**

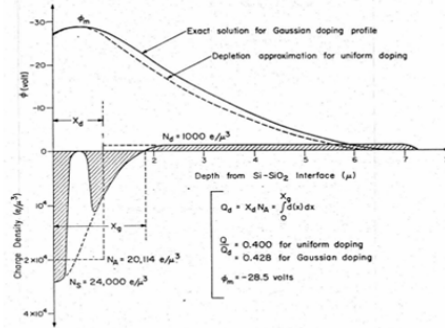


Fig. 1.17 The potential profiles ϕ by the depletion approximation and the exact numerical solution of the Gaussian doping profile are compared. $X_d = 1.0 \mu$ and the p-layer doping N_A of $20,000 \text{ e}/\mu^3$.

Chapter One

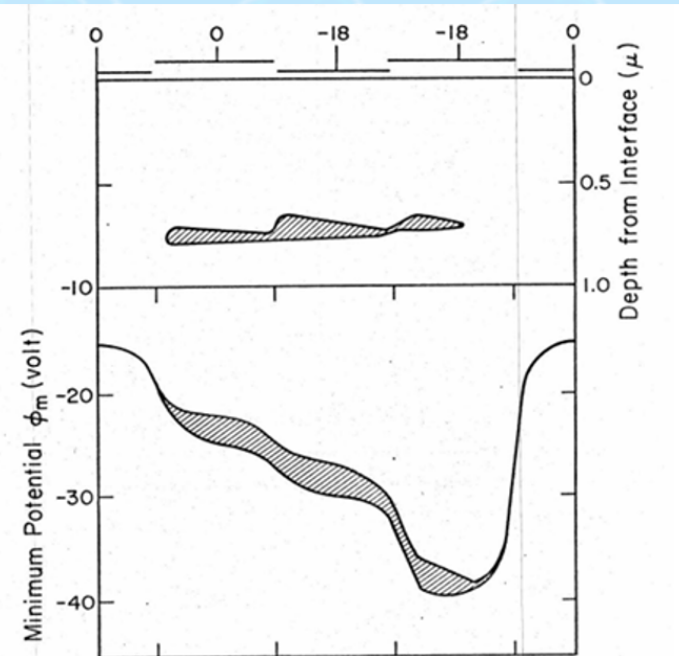


Fig. 4.14 The physical location of the charge packet in the p-layer is shown in the upper figure. The lower figure is the minimum potential with signal charge present.

Reported at ISSCC1974, February 1974 in Philadelphia, USA as a PhD student paper.

Introduction to Semiconductor Device

IEEE

[Caltech 1975 PhD Thesis by Yoshiaki Daimon Hagihara.pdf](#)

The (t, x, y) numerical device analysis of Buried Channel CCD Dynamic Charge Packet and two-dimensional Potential Profile for the overlapping Polysilicon Gate 2-phase CCD.

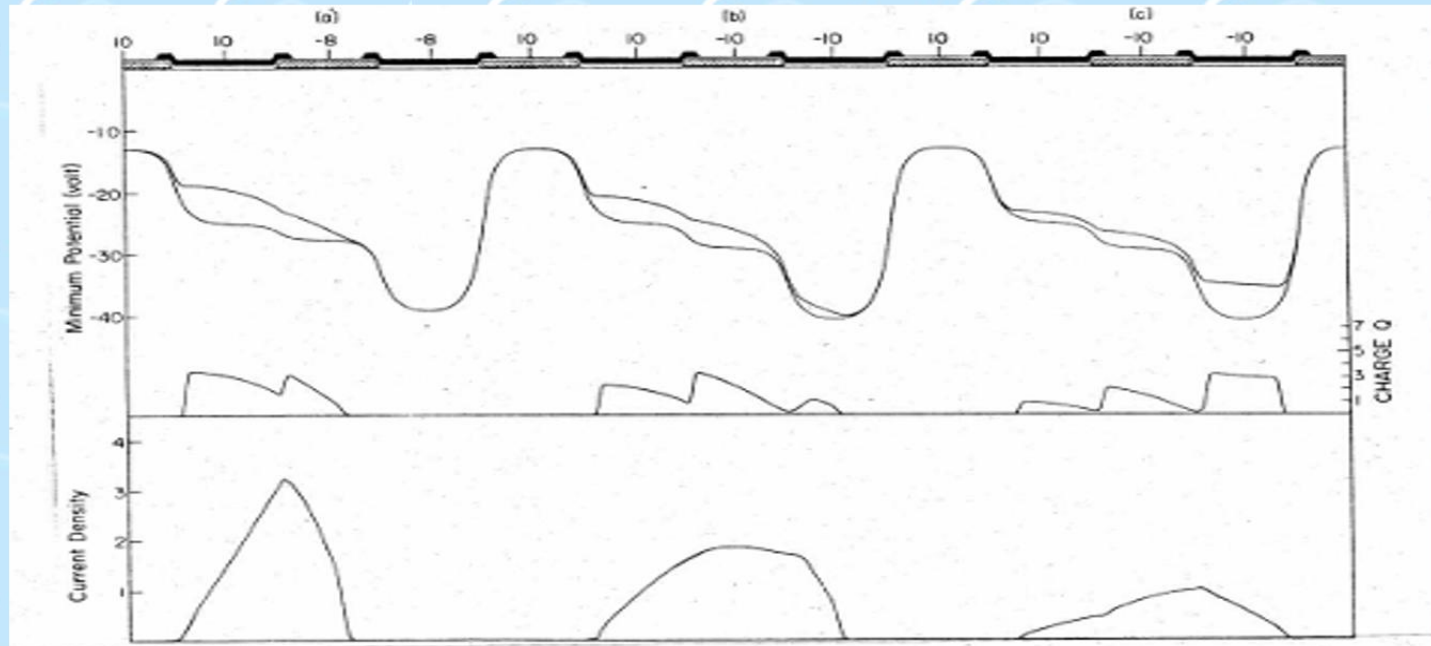
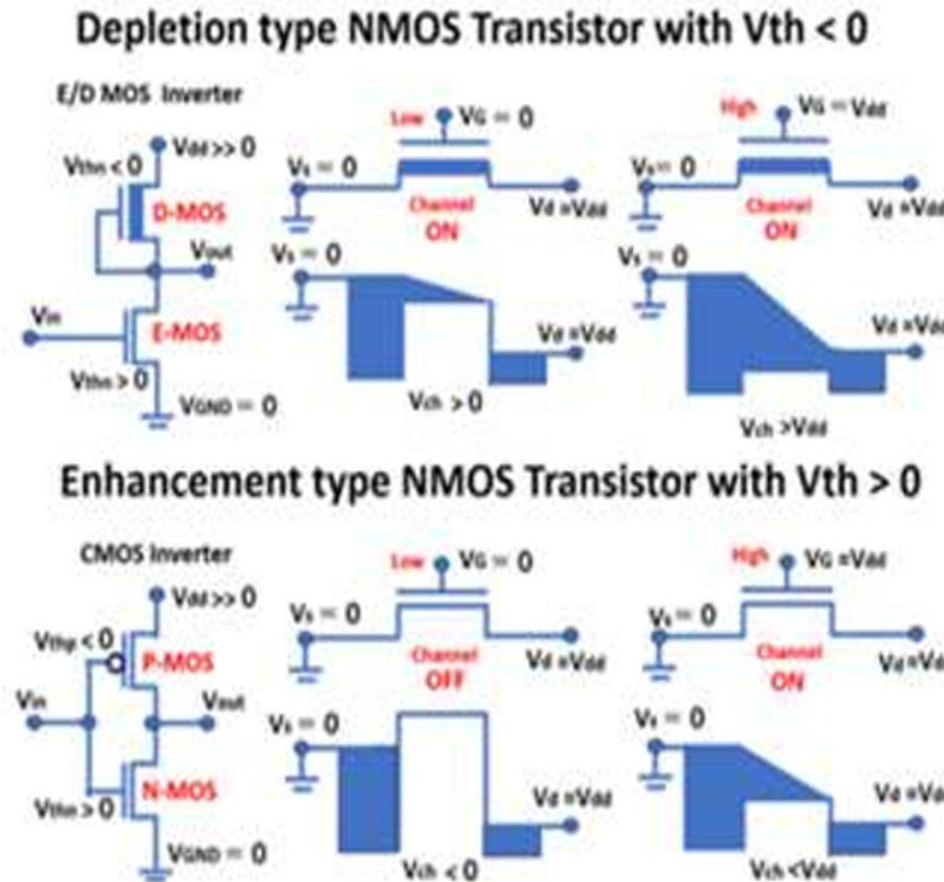


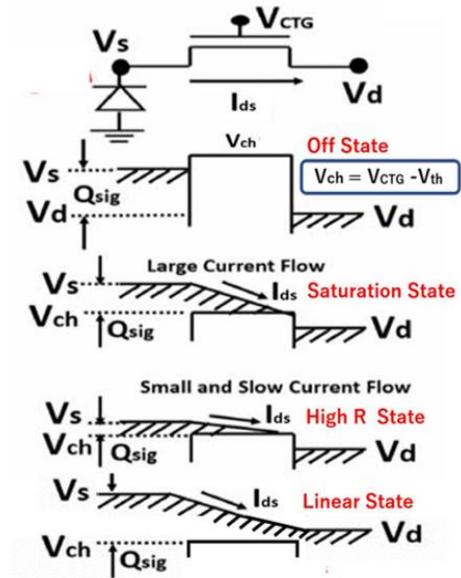
Fig. 5.1 The three stages (a), (b), and (c) of the charge transfer in buried channel CCDs are illustrated by the minimum potential, charge and current density plots. Charge and current density are normalized.

Introduction to Semiconductor Device

Serious Image Lag Problem in Floating-Surface N+P single junction photodiode

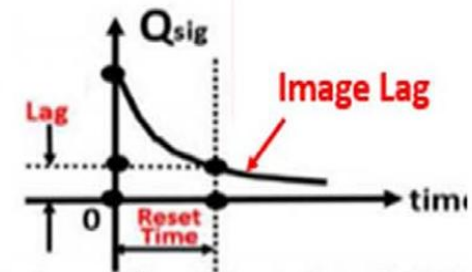


Water Gate Models of E/D MOS Transistors and CMOS Inverter

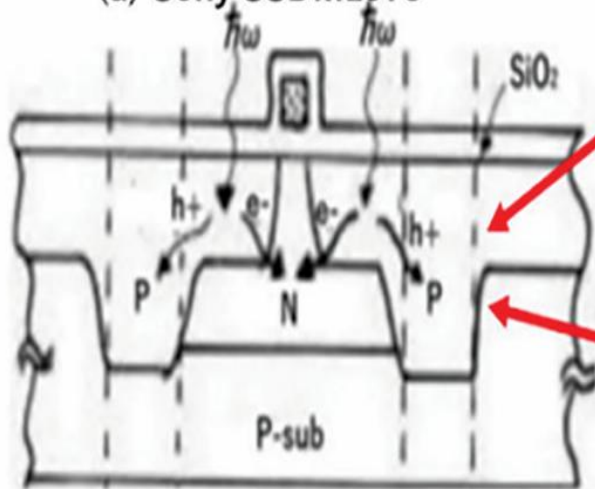


$$I_{ds}(t) = I_0 (V_s - V_{ch})^2$$

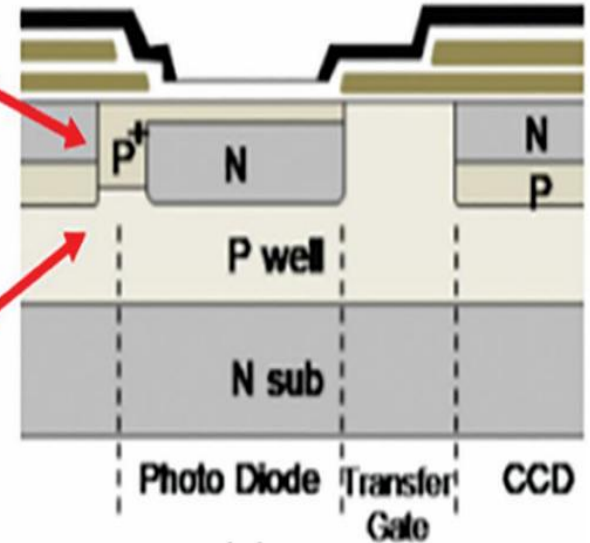
$$Q_{sig}(t) = Q_0 \exp(-t/\tau)$$



(a) Sony SSDM1978



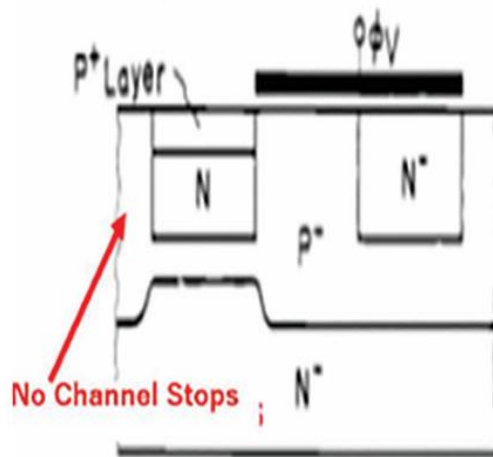
(b) Japan Semiconductor History Museum



heavily doped P⁺ channel stops formed by deep High Energy Ion Implantation

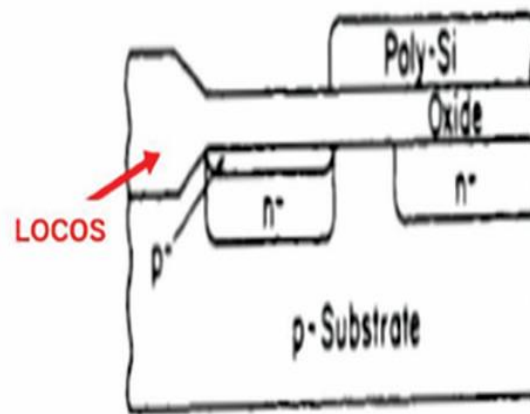
No LOCOS Isolation nor Shallow Trench Isolation were used.

(c) NEC IEDM1982



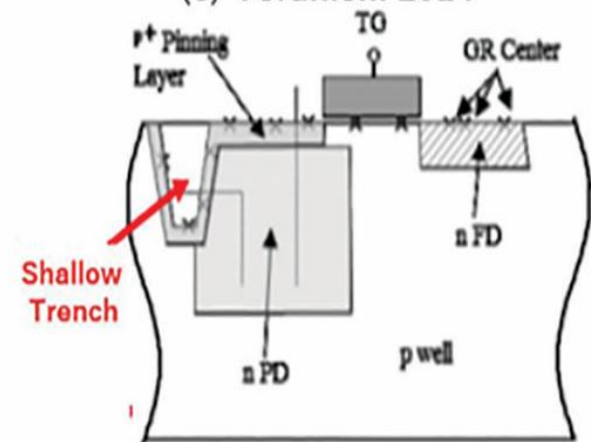
No Channel Stops ;

(d) KODAK IEDM1984



LOCOS

(e) Teranishi 2014



Shallow Trench

萩原良昭の大切な思い出写真宝物





Sony Kumamoto Technology Center



an invited ESSCIRC2001 Plenary Talk, Villach, Austria, September, 2001.

Yoshiaki Hagiwara

Sony Corpoartion, Tokyo Japan

yoshiaki.hagiwara@jp.sony.com

Abstract

A brief historical overview of a first home entertainment consumer electronic gadget, called a portable transistor radio is given, and then some introductory comments on the basic semiconductor device concepts are explained. They are strongly related to the microelectronics of the present home entertainment LSI chips with regard to the product specifications and performance aspects of the home entertainment LSI chip sets, such as for digital cameras, home robotics and games.

AIBO 2nd Generation, ERS-210



Sony Dream Robot, SDR-3



Fig. 10 New AIBO Models, ERS-210 and SDR-3

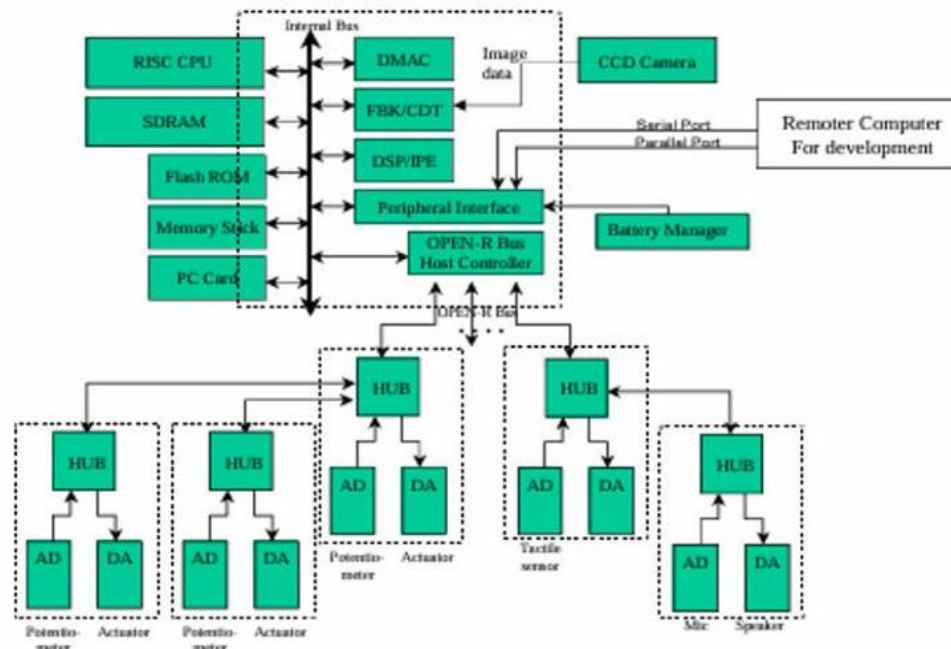


Fig. 11 Logical Hardware Block Diagram

- (3) M. Fujita and H. Kitano: "{D}evelopment of and {A}utonomous {Q}uadruped {R}obot for {R}obot {E}ntertainment", Autonomous Robots vol.5, pp.7-8, Kluwer Academic Publishers, 1998.

- (4) Kohtaro Sabe, "Architecture of Entertainment Robot - Development of AIBO -", IEEE Computer Element MESA Workshop 2001, Mesa Arizona, Jan 14-17, 2001

an invited ESSCIRC2001 Plenary Talk, Villach, Austria, September, 2001.

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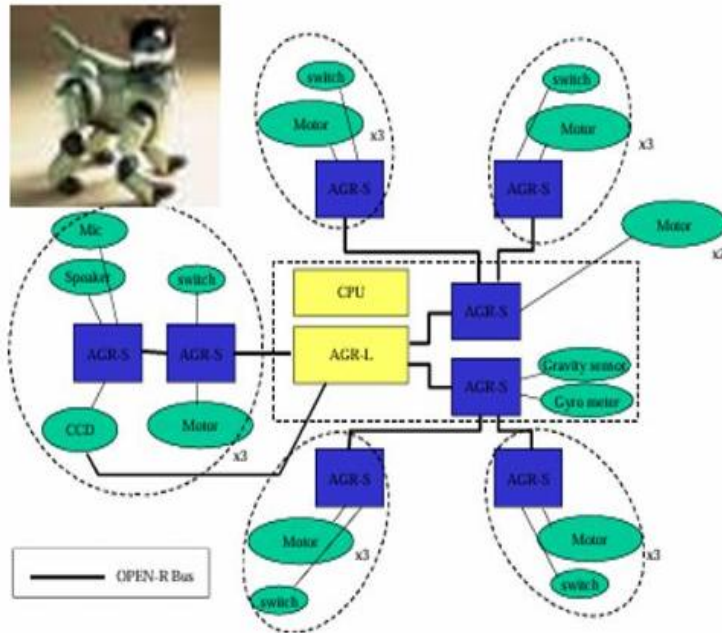


Fig. 12 Topology of ERS-110

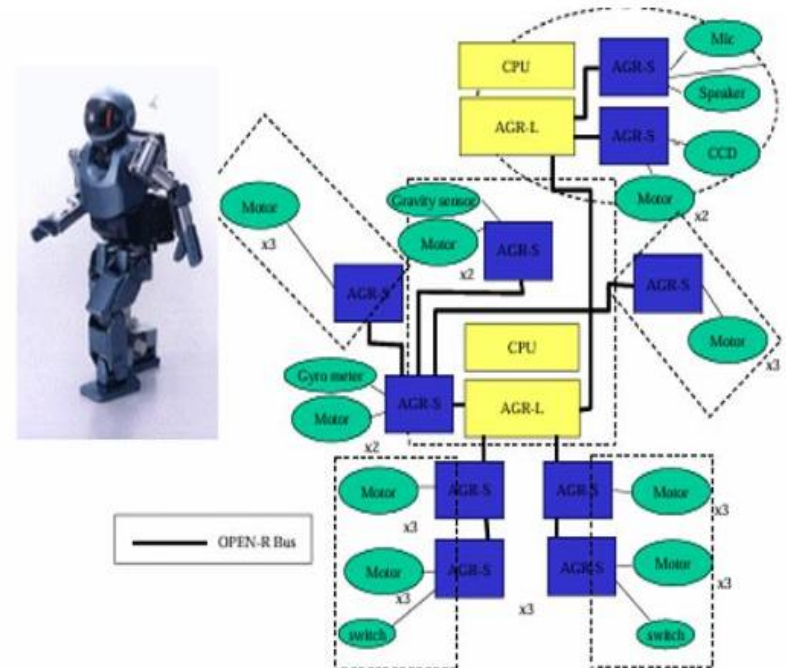


Fig. 13 Topology of SDR-3x

- (3) M. Fujita and H. Kitano: "{Development of and Autonomous Quadruped Robot for Entertainment}", Autonomous Robots vol.5, pp.7-8, Kluwer Academic Publishers, 1998.

- (4) Kohtaro Sabe, "Architecture of Entertainment Robot - Development of AIBO -", IEEE Computer Element MESA Workshop 2001, Mesa Arizona, Jan 14-17, 2001

an invited ESSCIRC2008 Plenary Talk, Technical Digest of IEEE
ESSCIRC2008 Conference,
Edinburgh, Scotland UK, September 2008.

SOI Design in Cell Processor and Beyond

Yoshiaki Daimon Hagihara

Chairman and CEO , AIPS/AINS Consortium

(Ex-Sony Fellow, Semiconductor Strategic Planning)

Hagihara-Yoshiaki@aiplab.com



Figure 1a Regency TR-1 Radio

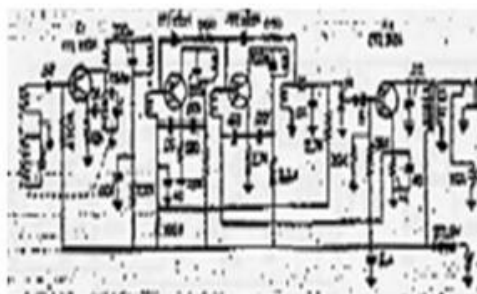
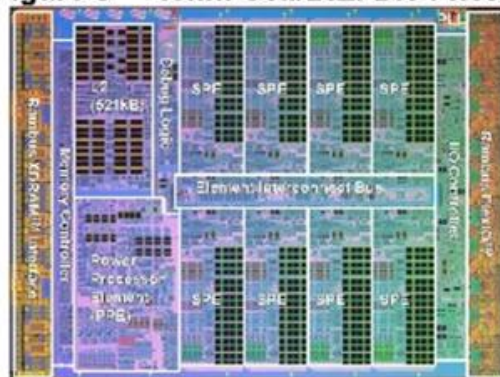


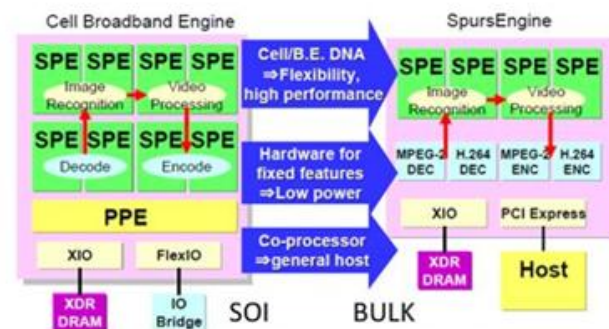
Figure 1b Circuits Diagram of Regency TR-1 Radio

Figure 8 45nm Cell/B.E. Die Photo



Osamu Takahashi ISSCC2006

By 1994, the games were just starting to move to 0.5-micron processes, while the leading process was 0.35 micron. Eventually over time, the game chips migrated to smaller processes to increase integration and reduce costs. Now games



Mitsuo Saito at ICD-ARC Panel May 13, 2008

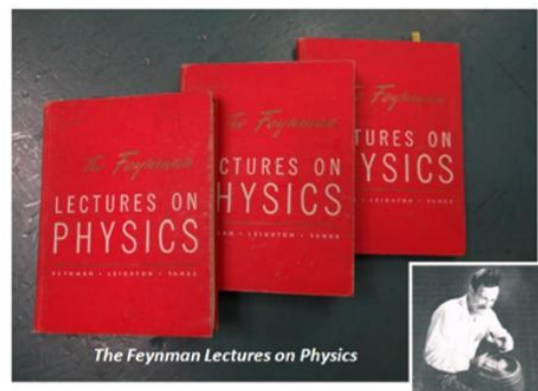
Figure 10 Cell/B.E. and Toshiba SpursEngine



Nicky Lu, flanked by intently listening Tom Lee and Rinaldo Castello.



Yoshi Hagihara, Eric Vittoz and Bob Brodersen.



Memory of Pro. Richard Feynman



Prof. T. C. McGill

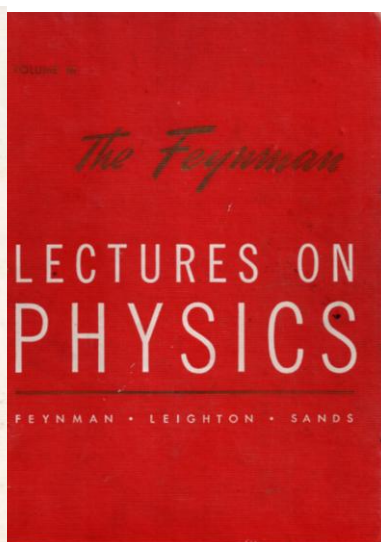
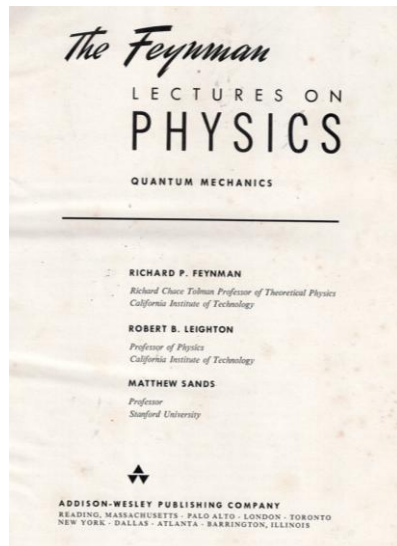
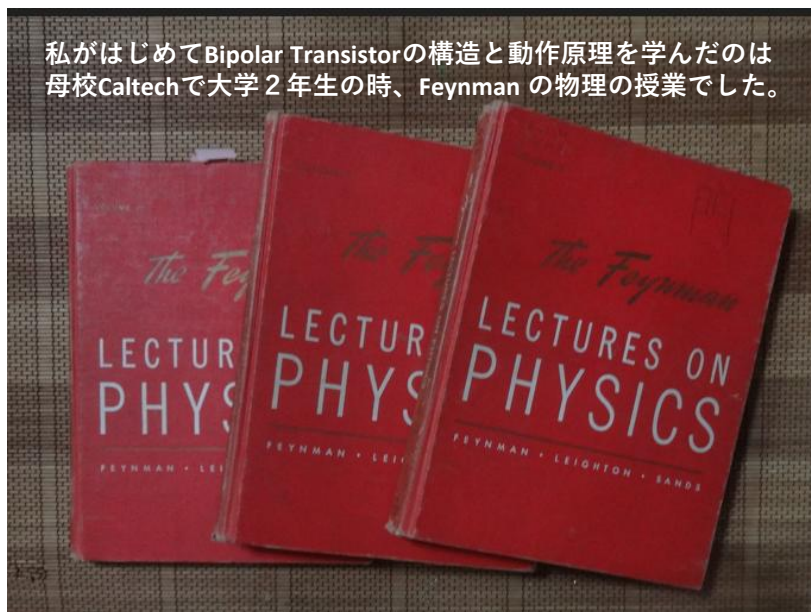


Prof. James McGaldin

As an undergraduate student at Caltech
from Sept 1967 till June 1969, at age 19 to 20,
I learned Feynman Physics from Prof. Feynman
and Prof. Leighton at Pasadena, California USA.

Yoshiaki Daimon Hagiwara

私をはじめBipolar Transistorの構造と動作原理を学んだのは
母校Caltechで大学2年生の時、Feynmanの物理の授業でした。



constant so long as ΔV is not too large. When they approach the barrier, these carriers will still find a downhill potential and will all fall down to the p -side. (If ΔV is larger than the natural potential difference V_i , the situation would change, but we will not consider what happens at such high voltages.) The net current I of positive carriers which flows across the junction is then the difference between the currents from the two sides:

$$I = I_0(e^{+q\Delta V/kT} - 1). \quad (14.14)$$

The net current I of holes flows into the n -type region. There the holes diffuse into the body of the n -region, where they are eventually annihilated by the majority n -type carriers—the electrons. The electrons which are lost in this annihilation will be made up by a current of electrons from the external terminal of the n -type material.

When ΔV is zero, the net current in Eq. (14.14) is zero. For positive ΔV the current increases rapidly with the applied voltage. For negative ΔV the current reverses in sign, but the exponential term soon becomes negligible and the negative current never exceeds I_0 —which under our assumptions is rather small. This back current I_0 is limited by the small density of the minority carriers on the n -side of the junction.

If you go through exactly the same analysis for the current of negative carriers which flows across the junction, first with no potential difference and then with a small externally applied potential difference ΔV , you get again an equation just like (14.14) for the net electron current. Since the total current is the sum of the currents contributed by the two carriers, Eq. (14.14) still applies for the total current provided we identify I_0 as the maximum current which can flow for a reversed voltage.

The voltage-current characteristic of Eq. (14.14) is shown in Fig. 14-10. It shows the typical behavior of solid-state diodes—such as those used in modern computers. We should remark that Eq. (14.14) is true only for small voltages. For voltages comparable to or larger than the natural internal voltage difference V_i , other effects come into play and the current no longer obeys the simple equation.

You may remember, incidentally, that we got exactly the same equation we have found here in Eq. (14.14) when we discussed the “mechanical rectifier”—the ratchet and pawl—in Chapter 46 of Volume I. We get the same equations in the two situations because the basic physical processes are quite similar.

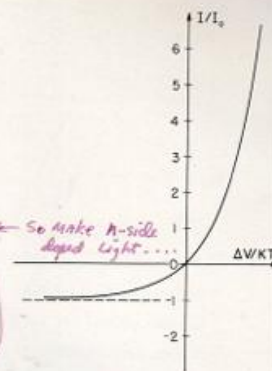


Fig. 14-10. The current through a junction as a function of the voltage across it.

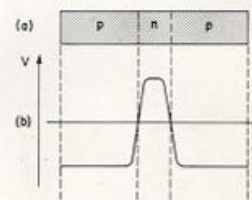


Fig. 14-11. The potential distribution in a transistor with no applied voltages.

14-6 The transistor

Perhaps the most important application of semiconductors is in the transistor. The transistor consists of two semiconductor junctions very close together. Its operation is based in part on the same principles that we just described for the semiconductor diode—the rectifying junction. Suppose we make a little bar of germanium with three distinct regions, a p -type region, an n -type region, and another p -type region, as shown in Fig. 14-11(a). This combination is called a p - n - p transistor. Each of the two junctions in the transistor will behave much in the way we have described in the last section. In particular, there will be a potential gradient at each junction having a certain potential drop from the n -type region to each p -type region. If the two p -type regions have the same internal properties, the variation in potential as we go across the crystal will be as shown in the graph of Fig. 14-11(b).

Now let's imagine that we connect each of the three regions to external voltage sources as shown in part (a) of Fig. 14-12. We will refer all voltages to the terminal connected to the left-hand p -region so it will be, by definition, at zero potential. We will call this terminal the *emitter*. The n -type region is called the *base* and it is connected to a slightly negative potential. The right-hand p -type region is called the *collector*, and is connected to a somewhat larger negative potential. Under these circumstances the variation of potential across the crystal will be as shown in the graph of Fig. 14-12(b).

Let's first see what happens to the positive carriers, since it is primarily their behavior which controls the operation of the p - n - p transistor. Since the emitter is

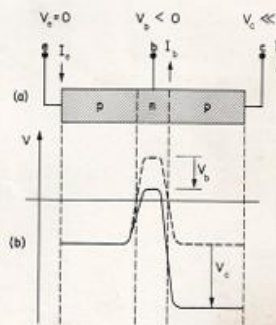
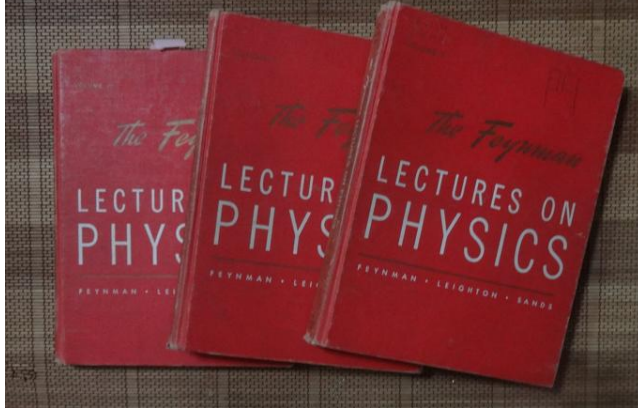


Fig. 14-12. The potential distribution in an operating transistor.

14-11

私がはじめてBipolar Transistorの構造と動作原理を大学2年生の時、Feynmanの物理の授業で学んだ。



人工知能パートナーシステム(AIPS)を支える
デジタル回路の世界

IEEE Life Fellow, Ph.D.

萩原 良昭 著

ISBN978-4-88359-339-2 B5判 上製 475頁

定価(本体3,000円+税)

未来の人間社会には人工知能パートナーシステム(AIPS)とも言える人間にやさしい支援システムが出現すると期待している。AIPS搭載の自動走行車や老人介護システム、人間型歩行ロボットやロボット・ハウスなどである。そこで本書では、そのAIPSを支える「デジタル回路の世界」と題し、ハードとソフトの両面で、人とコンピュータをつなぐデジタル技術について紹介している。図や絵をたくさん用意して、基礎からやさしく解説している。

真空管とBipolar Transistorの構造と動作原理の違いの比較

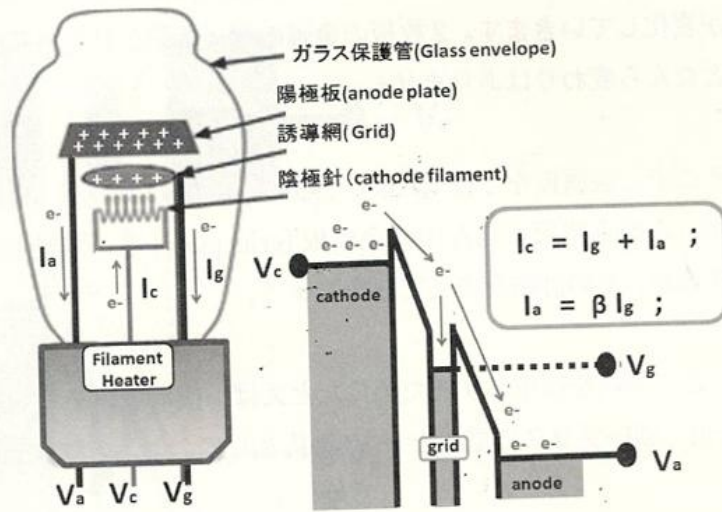


図 3-7-4 三極真空管の電流増幅動作

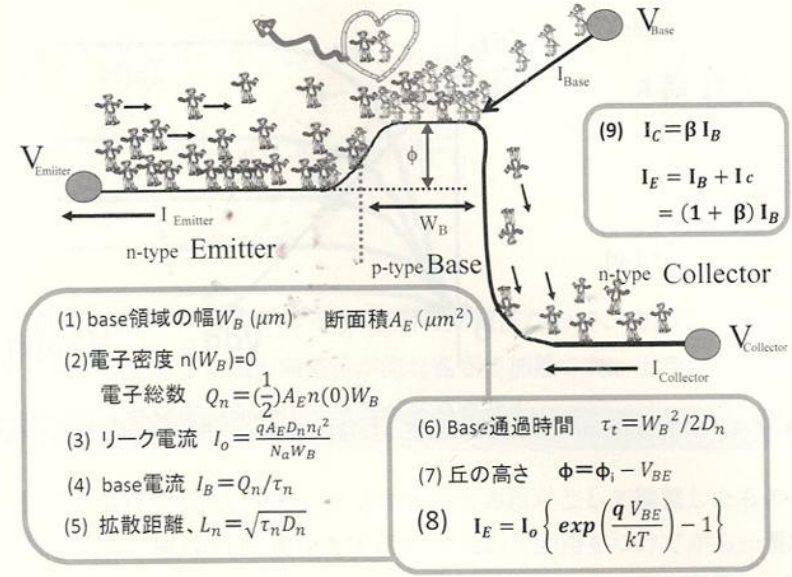
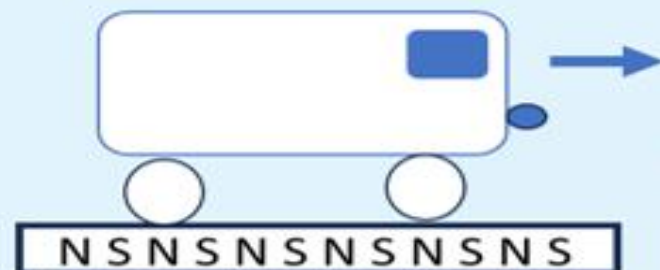
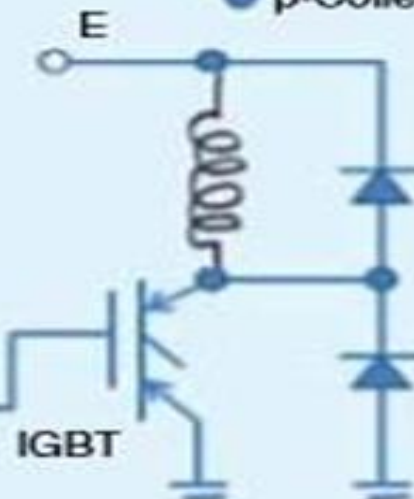
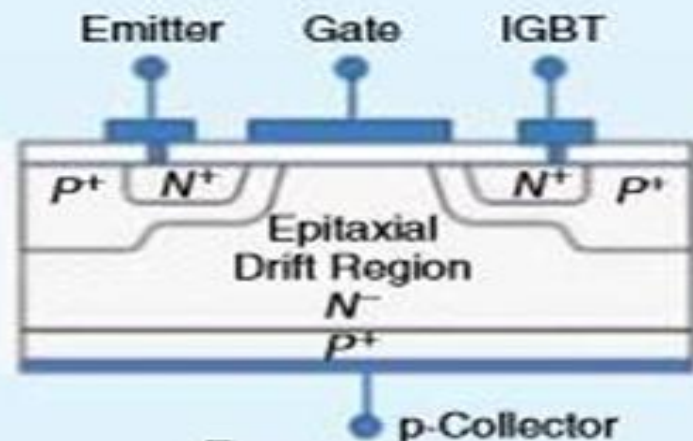


図 4-3-3 NPN bipolar transistor の関係するいろいろな物理定数

ISSSCC2023 Plenary Panel Talk, February 2013



Rails coated with Magnetic films
or magnetized and powered
by fast IGBT electrical switches.



ISSSCC2023 Plenary Panel Talk, February 2013

Magnescale

Magnescale Products



Achieves high resolution with the interpolation processing technology developed by Magnescale

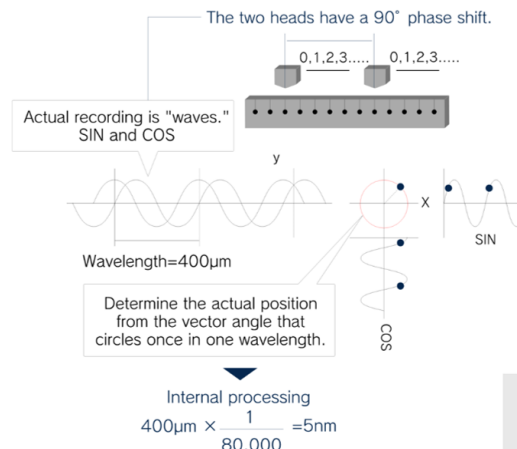
5nm Resolution in Positioning

Interpolation processing technology is a technology that accurately divides the signal waveform detected from a magnetic scale to the required pitch (fineness). For example, in the case of a SmartSCALE, two sine waves with a phase shift of 90 degrees are detected from a magnetic scale engraved with a pitch of 400μm. If the signal contains distortion, accurate position information (true value) cannot be obtained. The DC component is removed from the signal detected from the scale, and level and phase adjustments are made in real time, and **the position information with a resolution of 5nm is obtained by dividing the signal into 80,000 segments through advanced signal processing.**

<https://www.magnescale.com/en/magnescale/>

When looking for environmental resistance and high precision, we ended up with magnetism. The history of Magnescale, which even became this company name, begins with the invention of the magnetic flux responsive magnetic head by Sony's Mitsuyoshi Uemura and others in 1965. Over 50 years have passed since then, and now we use magnetic resistance change (MR) heads, and even the magnetic materials have changed, but the essence remains the same—a position detection system that is resistant to harsh environments because it uses magnetic detection.

In the pursuit of environmental resistance and high precision, magnetism was the answer.



Linear Motor Car



N S N S N S N S N S

Rails coated with Magnetic films or magnetized and powered by fast IGBT electrical switches.

**5nm Resolution
in Positioning
and Angle-Rotation
Control of
Rotary Engine for
Robot Arms**

ISSSCC2023 Plenary Panel Talk, February 2013

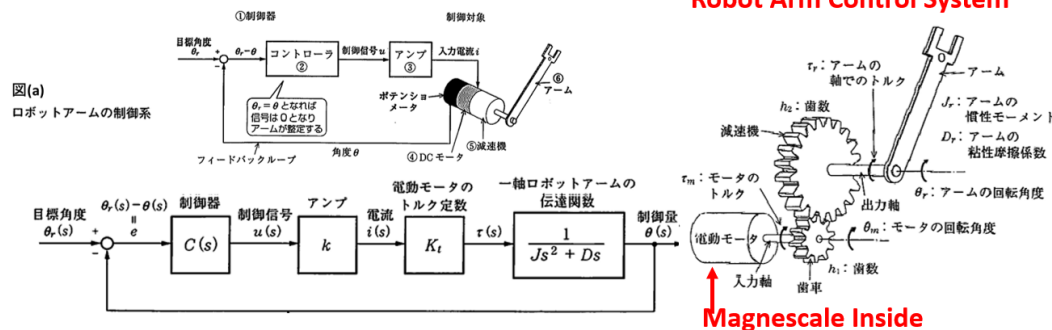
Magnescale

Magnescale Products



<https://www.magnescale.com/en/magnescale/>

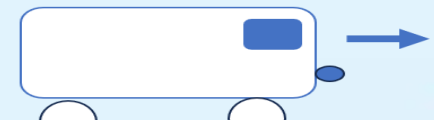
In the pursuit of environmental resistance and high precision, magnetism was the answer.



One-Axis Manipulator Control Feedback System Block

It's hardly affected by condensation or oil, common in machine tools, and continues to have high vibration and shock resistance. It also tracks the thermal expansion and contraction of machine tool tables. The evolved form of Magnescale is the Smart Scale, released in 2015. By adopting tunnel magnetoresistance (TMR) elements as magnetic sensors and developing new magnetic materials, signal processing circuits, and interpolation algorithms, it has created a system where the scale and head are completely separated. This complete separation allows both the head and scale to be fully protected, and even worn parts like bearings are eliminated. For NC machine tools, it was the industry's first to combine IP67 environmental resistance with 5nm high resolution.

Linear Motor Car



N S N S N S N S N S N S

Rails coated with Magnetic films or magnetized and powered by fast IGBT electrical switches.

**5nm Resolution
in Positioning
and Angle-Rotation
Control of
Rotary Engine for
Robot Arms**

Robot Arm を動かすのは半導体部品の仕事です。

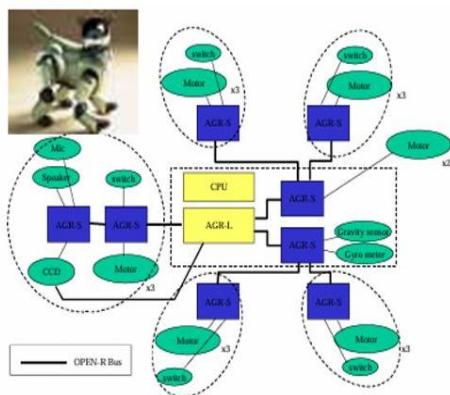


Fig. 12 Topology of ERS-110

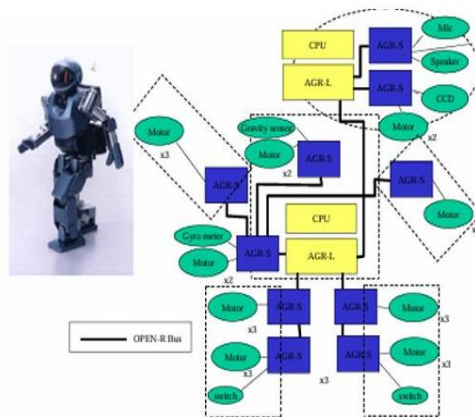


Fig. 13 Topology of SDR-3x

人間に置き換えた場合

- 第1軸：腰の回転
- 第2軸：肩の関節の動き
- 第3軸：肘の関節の動き
- 第4軸：手首の回転
- 第5軸：手首の曲げ
- 第6軸：指先の回転

制御用半導体部品が
サーボアンプ回路に指示を出し
PCM電気信号パルス出力で
サーボモーターをON/OFFし
常にロボットアームの軸の
回転角度をセンサー感知し
制御用半導体部品に
Feed-Backします。

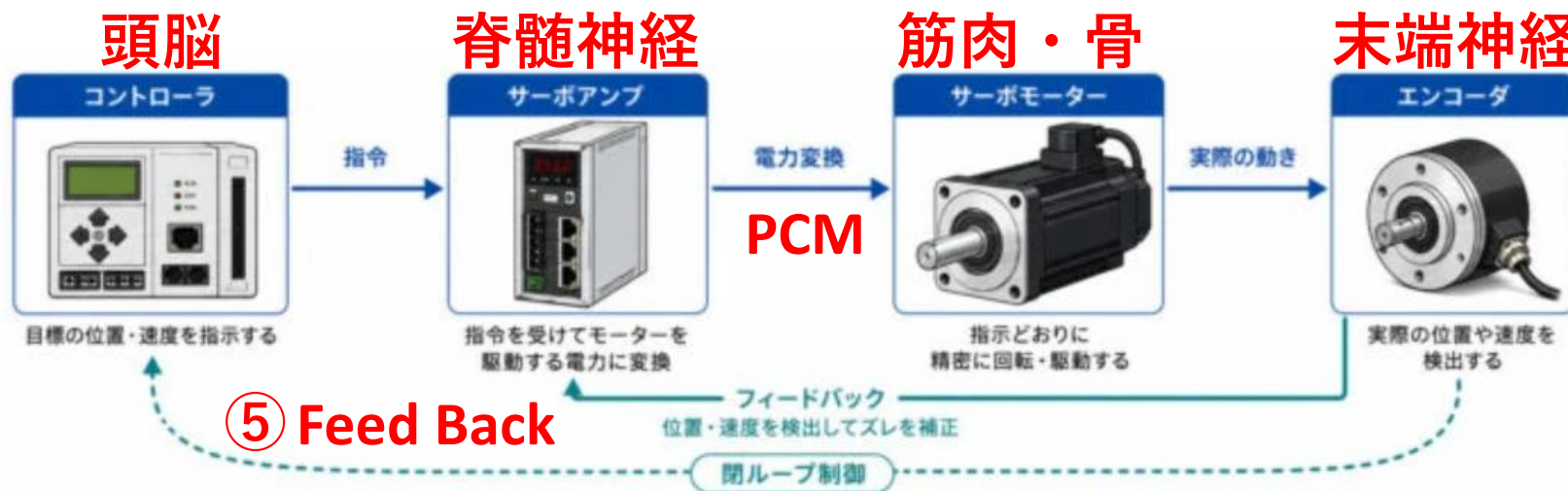


Rotary Servomotor controlled by Semiconductor Chips

Robot Arm を動かすのは半導体部品の仕事です。

Robot Armの各軸の各回転制御に広く 小型サーボモーター が利用されます。

- ① 制御用半導体部品 ② サーボアンプ回路 ③ サーボモーター ④ エンコーダー



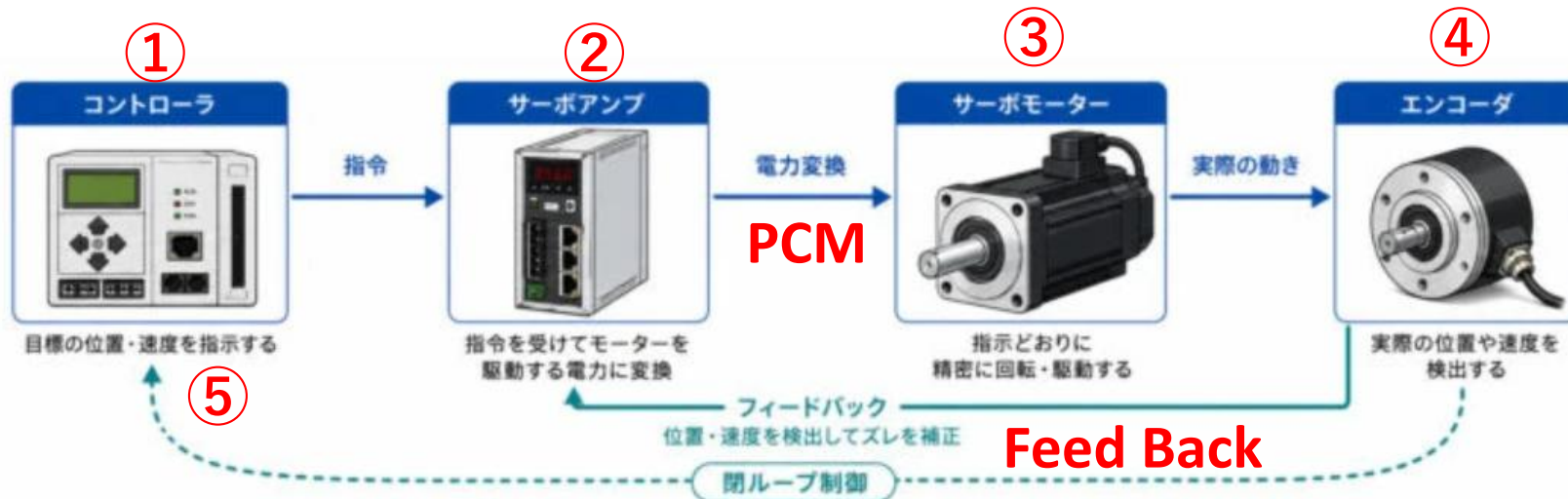
- ① 制御用半導体部品が
- ② サーボアンプ回路に指示を出し
PCM電気信号パルス出力で
- ③ サーボモーターをON/OFFし
常にロボットアームの軸の
- ④ 回転角度をセンサー感知し
制御用半導体部品に
- ⑤ Feed-Backします。



Robot Armの各軸にはサーボモーターとエンコーダーが内蔵されています。

<https://aiwaok.jp/articles/servo-motor>

- 長所： 高精度・高応答・負荷変動への制御設定能力（強さ）が
- 短所： そのまま、検出と調整の難しさがコストに跳ね返ります。



サーボモーターは最適ではなく、使わないほうが経済的なケースもあります。一定速度で回すだけの用途や、低速での位置決め・停止保持が中心の装置では、要求精度・負荷・速度条件により、ステッピングモーターやインバーター制御の誘導電動機など、より単純に低コストな方式で満たせる場合があります。インバーター制御は誘導電動機の回転速度を変える方式で、速度制御を得意とし、サーボモーターは速度制御だけでなく正確な位置決め制御を高精度に実現可能です。一般的な搬送設備の駆動主役は、インバーター制御の誘導電動機であることが多く、冷暖房設備はインバーター制御で十分で必ずしもサーボモーターが必要とは限りません。おもちゃのロボットでも値段と性能のバランスで製品が生まれます。

ロータリーモーターの特徴

回転運動を生成する一般的なモーターの一種

ロータリーモーターは、回転運動を生成する一般的なモーターの一種です。ステーター（固定子）とローター（回転子）から構成されています。電流がステーターの巻線を流れると、磁場が生成され、ローターが駆動されて回転運動を起こします。ロータリーモーターは、コストパフォーマンスが高く、汎用性が広く、技術の成熟が進んでいるため、多くの産業で使用されています。

サーボモーターは最適ではなく、使わないほうが経済的なケースもあります。一定速度で回すだけの用途や、低速での位置決め・停止保持が中心の装置では、要求精度・負荷・速度条件により、ステッピングモーターやインバーター制御の誘導電動機など、より単純に低コストな方式で満たせる場合があります。インバーター制御は誘導電動機の回転速度を変える方式で、速度制御を得意とし、サーボモーターは速度制御だけでなく正確な位置決め制御を高精度に実現可能です。一般的な搬送設備の駆動主役は、インバーター制御の誘導電動機であることが多く、冷暖房設備はインバーター制御で十分で必ずしもサーボモーターが必要とは限りません。おもちゃのロボットでも値段と性能のバランスで製品が生まれます。

ロータリーエンジンとは、三角形のローターが回転することで直接回転動力を生み出す独自構造の内燃機関です。

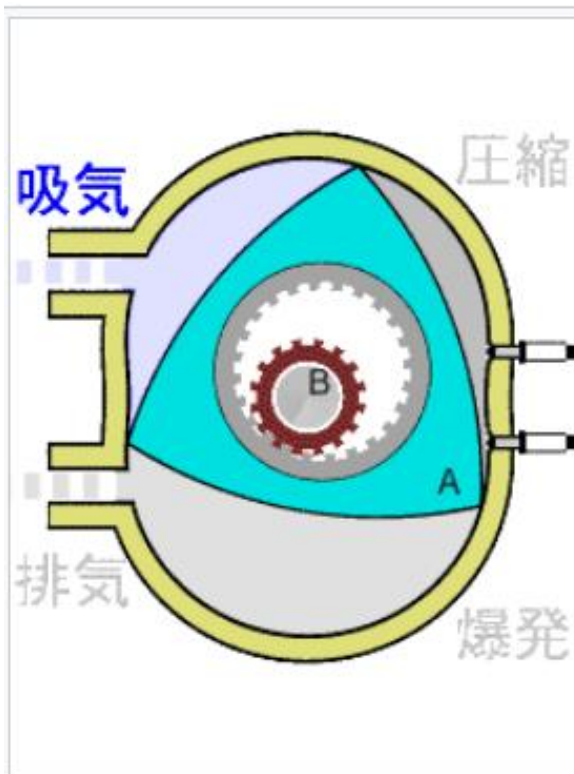
基本原理と構造

ロータリーエンジン（ヴァンケルエンジン）は、従来のピストンが往復運動するレシプロエンジンとは異なり、**三角形のローターが円形のハウジング内を回転することで吸気・圧縮・燃焼・排気の4工程を連続的にやり、直接回転動力を得る仕組み**です

ローターの回転により、吸排気ポートの開閉も自動的に行われるため、バルブやカムシャフトなどの複雑な動弁系は不要です

ロータリーエンジンの動作

吸気→圧縮→膨張→排気の
オットーサイクルが
3組同時進行している



ロータリーエンジンのローター
(マツダミュージアム、2005年2月撮影)



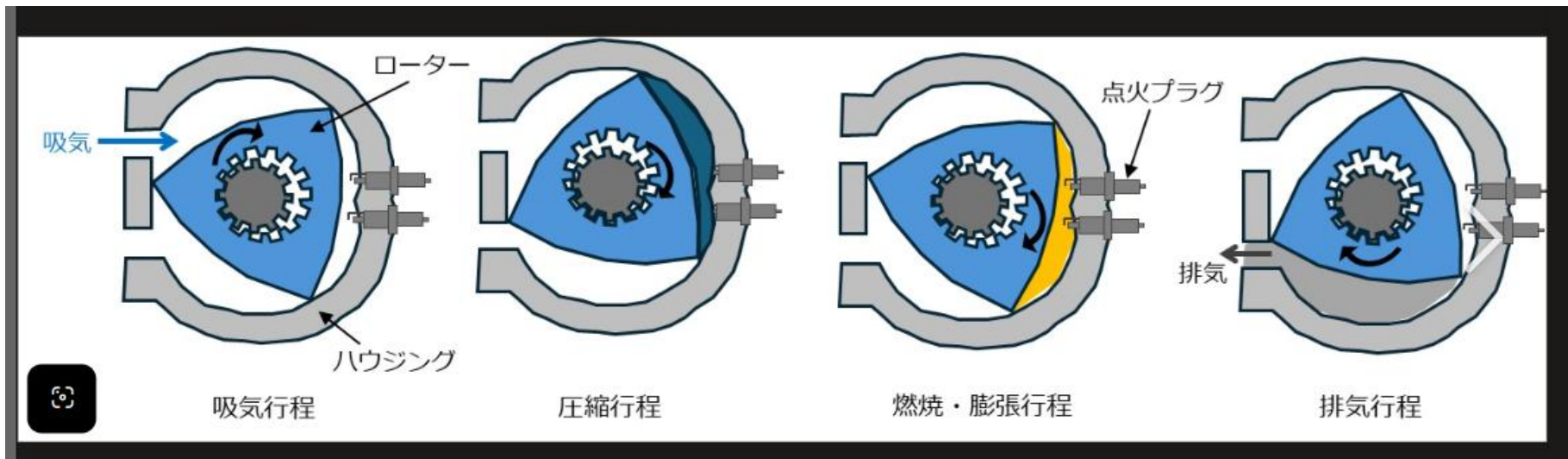
マツダスピード製レース用3ローターエンジン

ロータリーエンジンは、三角形のローターが回転することで動力を生み出す内燃機関です。従来のピストンエンジンとは異なる構造を持つエンジンです。

基本的な仕組み

ロータリーエンジンは、おむすび型のローターがまゆ型のハウジング内を回転することで、
・圧縮・燃焼・排気の四工程を連続的にを行い、回転運動として動力を発生させます。
ピストンエンジンのように往復運動を回転に変換する必要がなく、最初から回転運動で出力を得られる点が特徴

ローターの回転により、ハウジング内に3つの空間が形成され、それぞれの空間で工程が順に進行します。



When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of the threshold voltage is observed. This narrow channel effect has been applied successfully in creating an asymmetric potential well under an electrode for two-phase CCD operation. The feasibility of this structure has been confirmed in a 242-element analog delay line. The application is now extended to a 800 H/spl times/492 V frame transfer-type buried channel CCD imager with 14.31818 MHz frame shift, which results in a very low smear level of 0.01%, which is good enough for low-cost multimedia video camera applications.

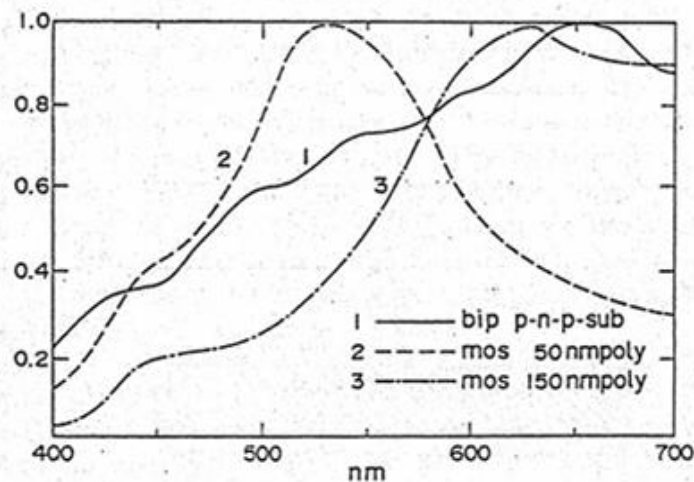
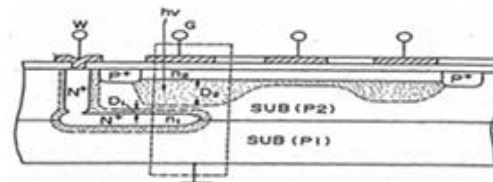


Fig. 7. Relative spectrum response. The relative response of the bipolar-type $\text{SiO}_2\text{-P2-N1-P1-SUB}$ structure is compared with poly- $\text{SiO}_2\text{-N2-P(SUB)}$ structures of the polysilicon thickness of 50 and 150 nm.

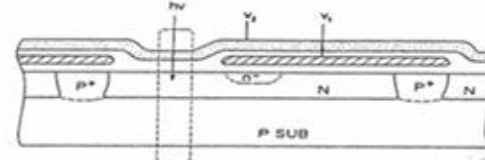
Early 1973

(3) mos 150 nmpoly



Sony 1974

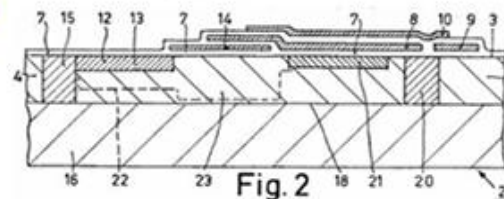
(2) mos 50 nmpoly



Philips 1975

(1) bip p-n-p-sub

June 9, 1975

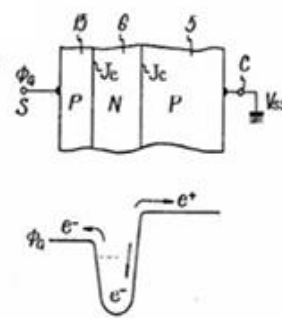
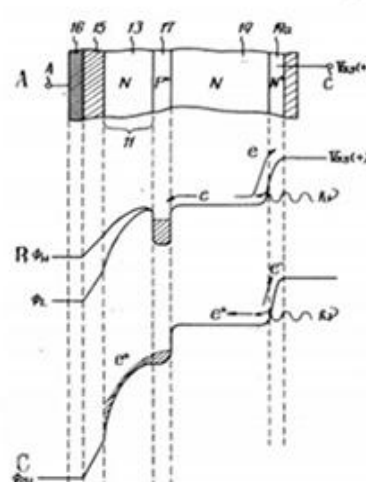
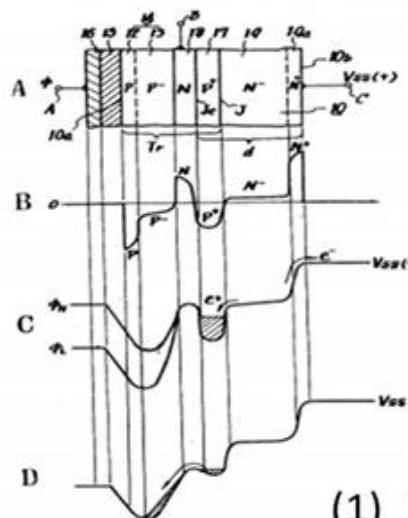


Sony (Hagiwara) March 5, 1975

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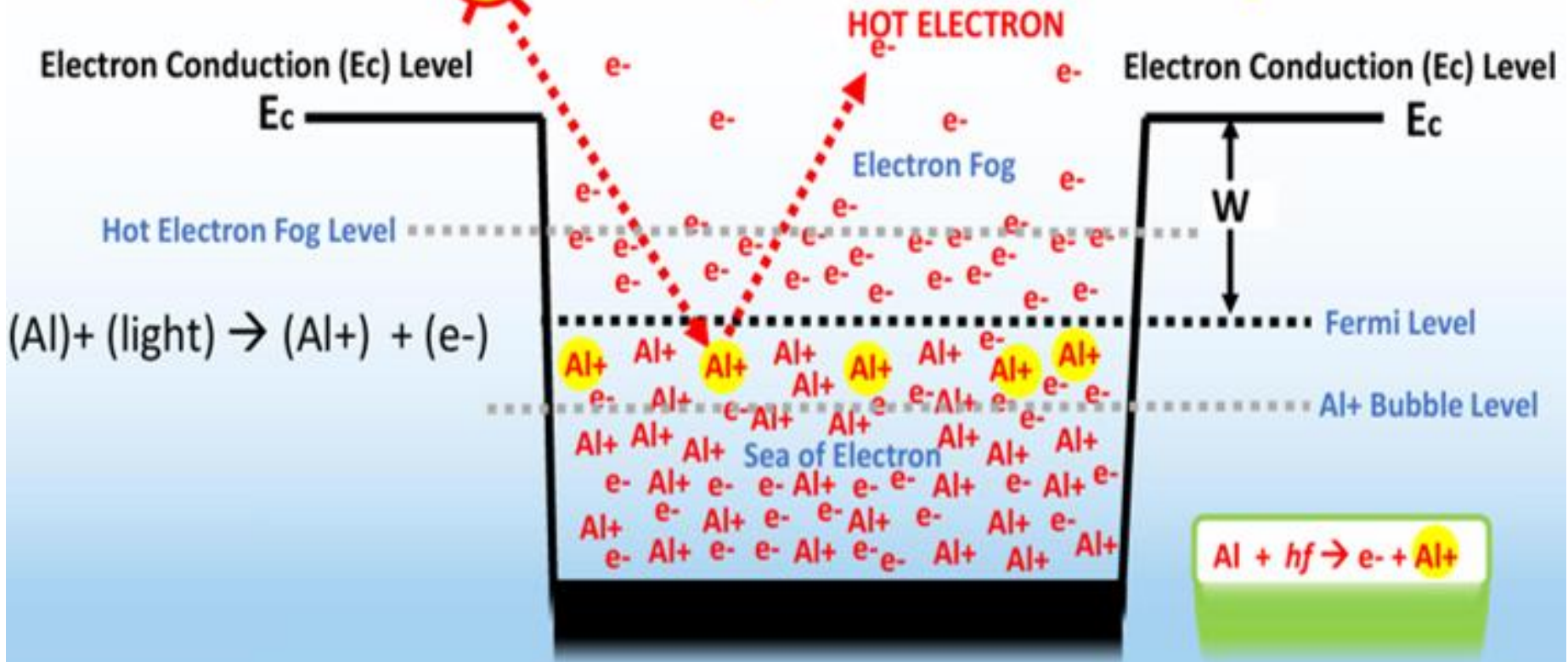


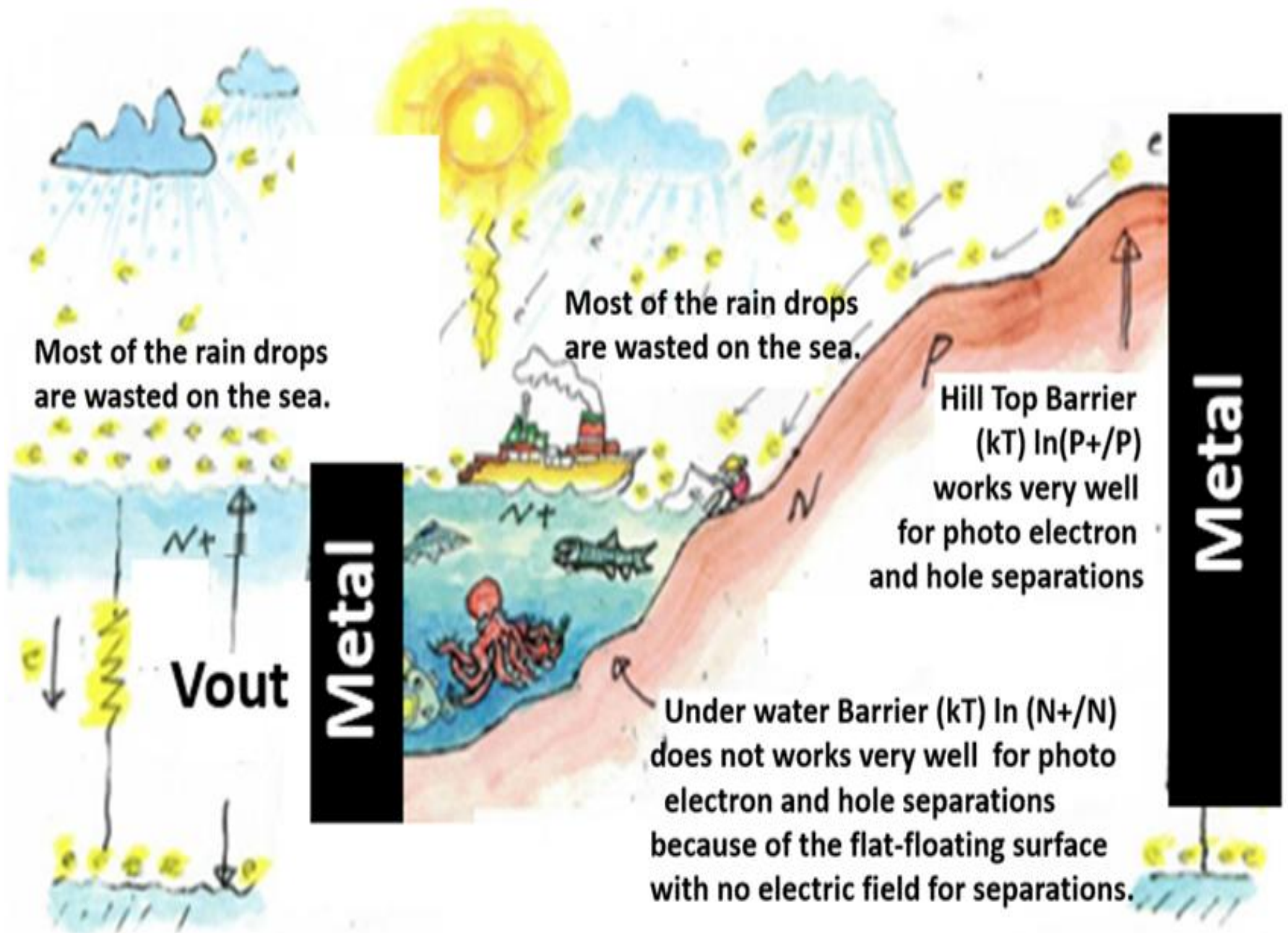
(1) bip p-n-p-sub March 5, 1975

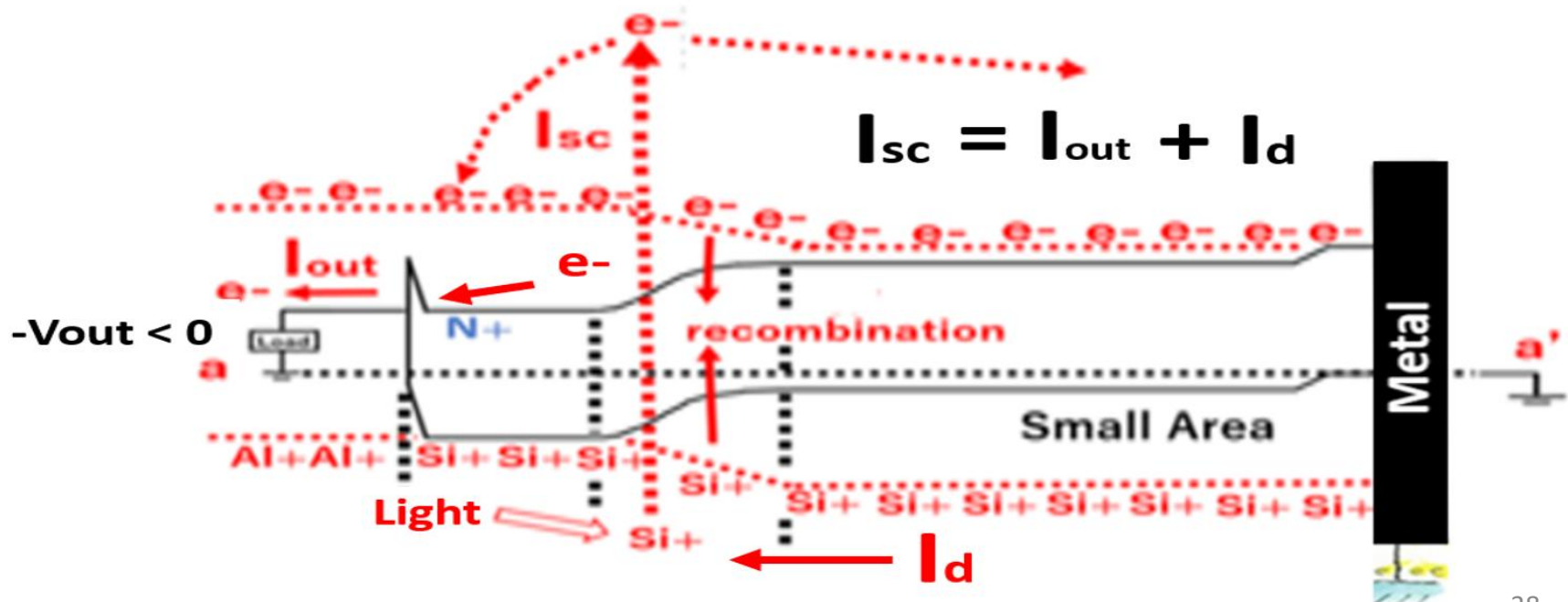
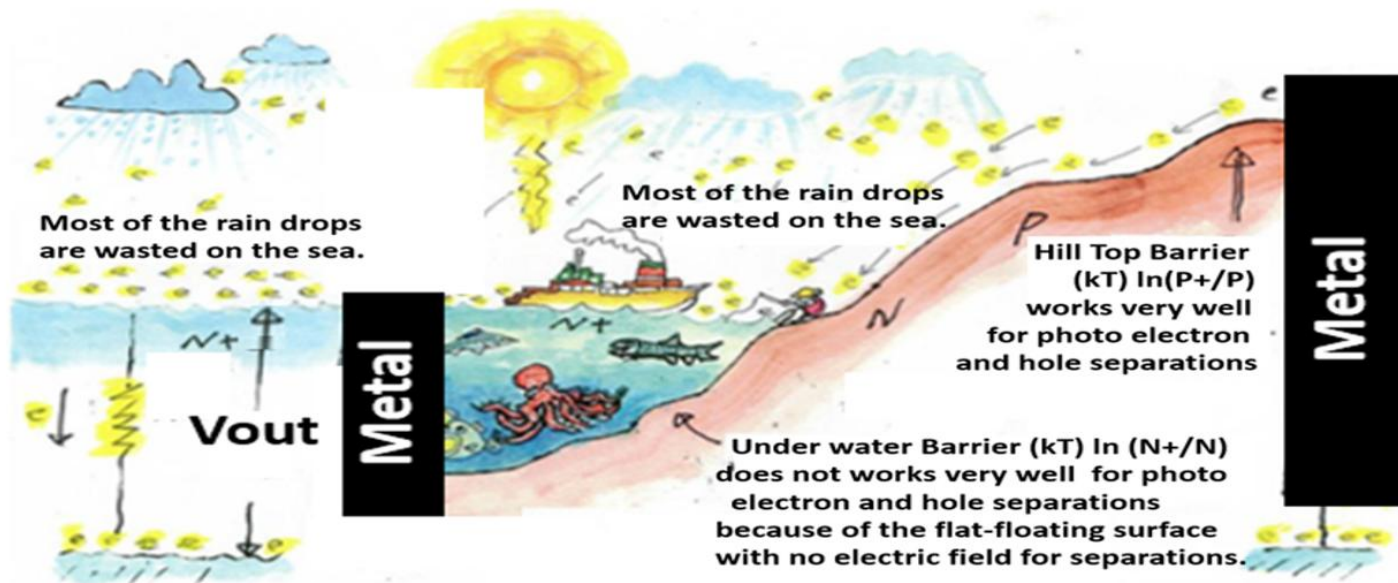
Physical Model of Metal

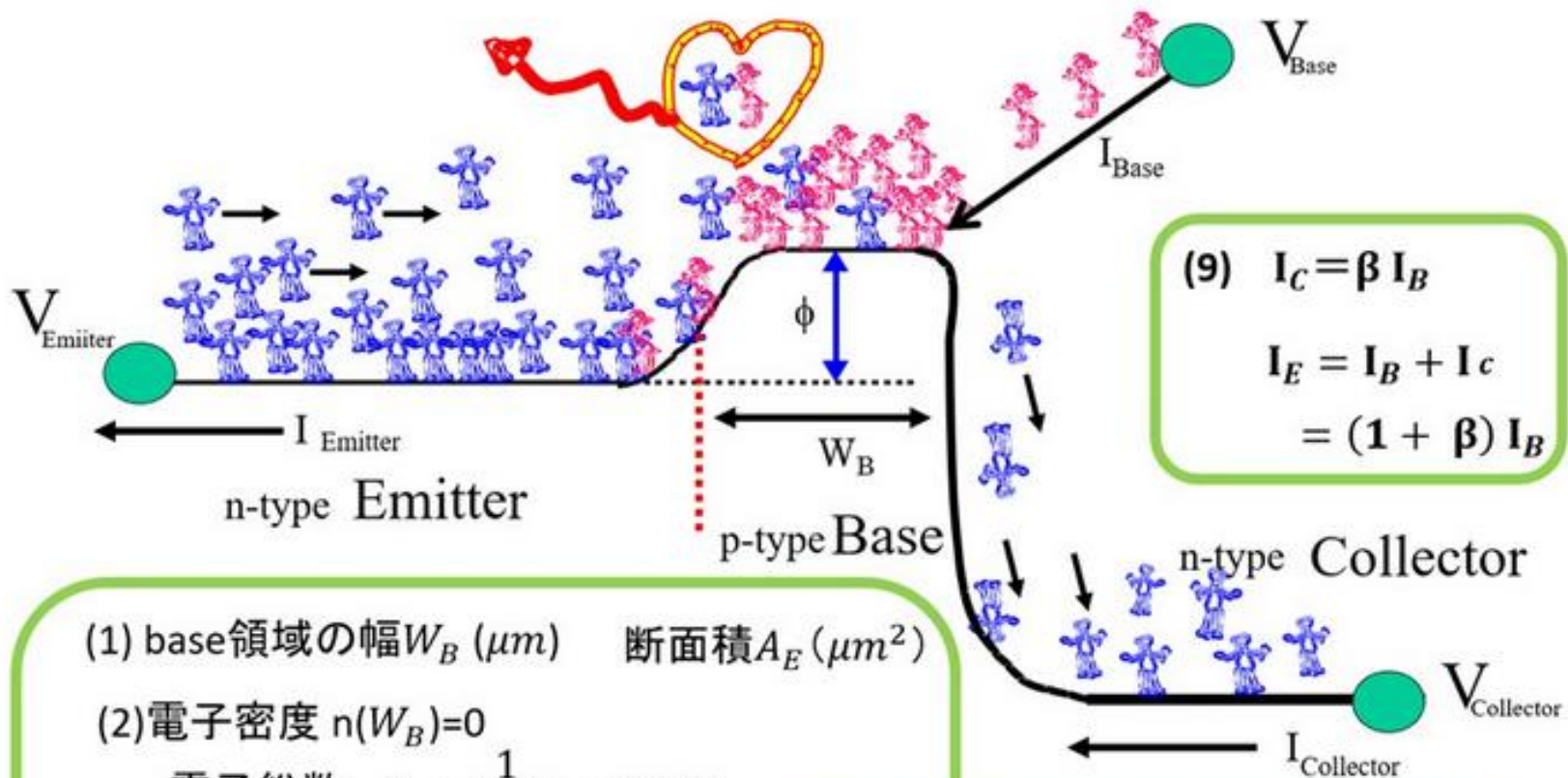


Concept of Electron Fog









$$(9) \quad I_C = \beta I_B$$

$$I_E = I_B + I_C \\ = (1 + \beta) I_B$$

(1) base領域の幅 W_B (μm) 断面積 A_E (μm^2)

(2) 電子密度 $n(W_B) = 0$

$$\text{電子総数 } Q_n = \left(\frac{1}{2}\right) A_E n(0) W_B$$

(3) リーク電流 $I_o = \frac{q A_E D_n n_i^2}{N_a W_B}$

(4) base電流 $I_B = Q_n / \tau_n$

(5) 拡散距離、 $L_n = \sqrt{\tau_n D_n}$

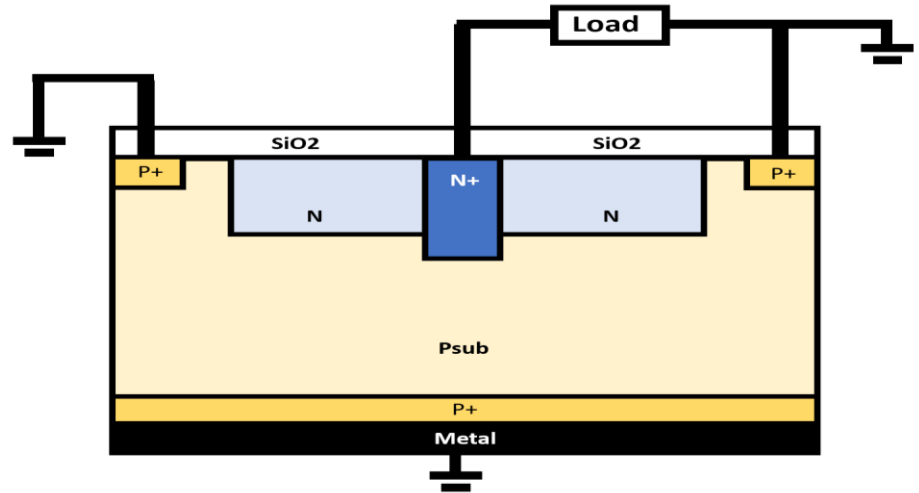
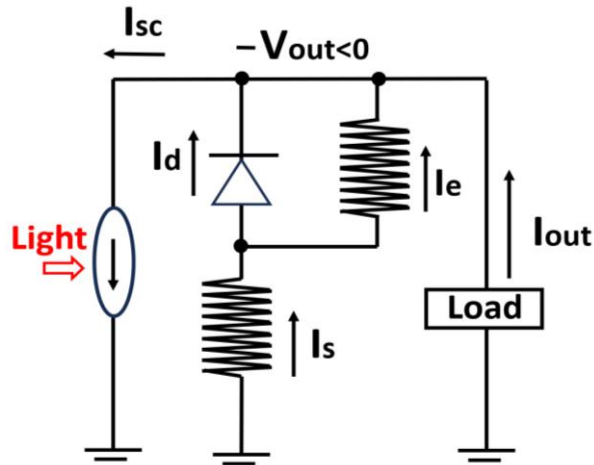
(6) Base通過時間 $\tau_t = W_B^2 / 2 D_n$

(7) 丘の高さ $\phi = \phi_i - V_{BE}$

$$(8) \quad I_E = I_o \left\{ \exp\left(\frac{q V_{BE}}{kT}\right) - 1 \right\}$$

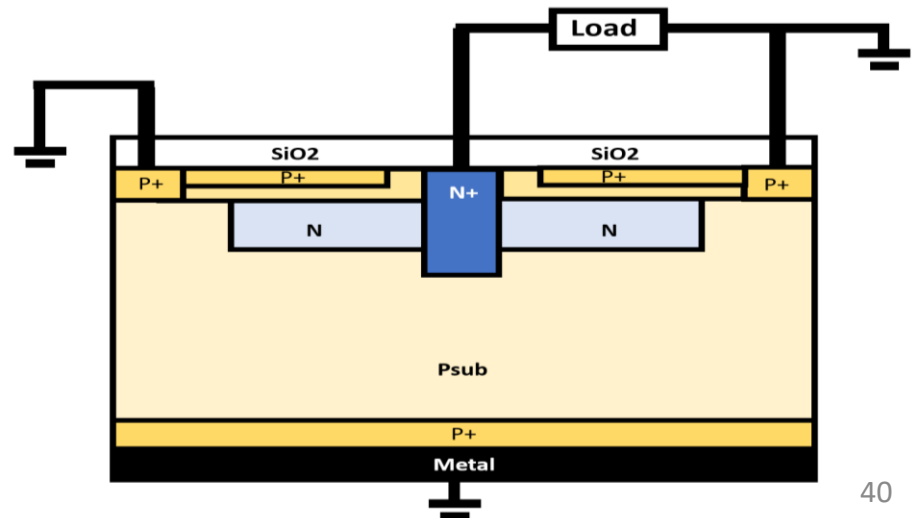
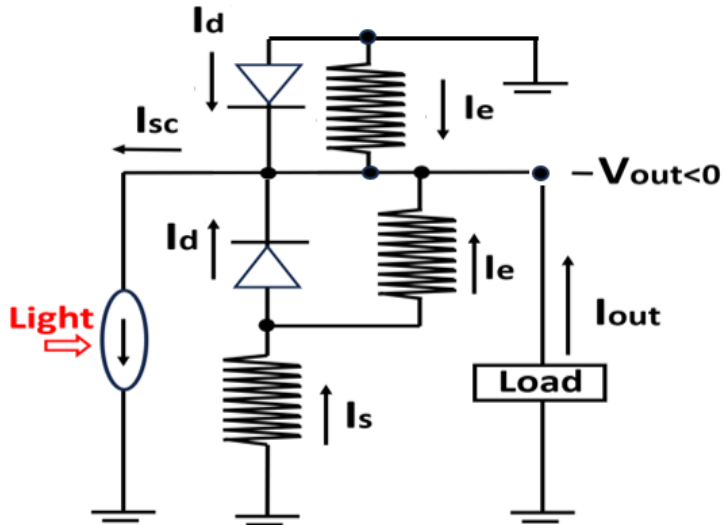
NPN bipolar transistorの関係するいろいろな物理定数

(1) Conventional N+N_{Psub}P+ Single Junction Solar Cell

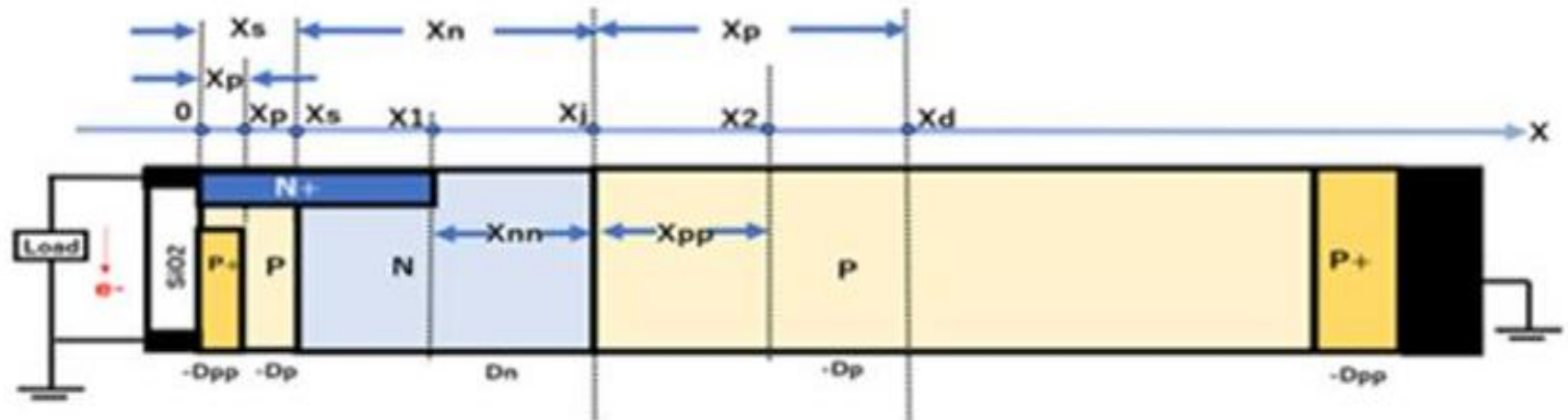


(2) Pinned-Surface P+PNP_{sub}P+ Double Junction Solar Cell with Buried-Channel Completely-Depleted Empty Potential Well

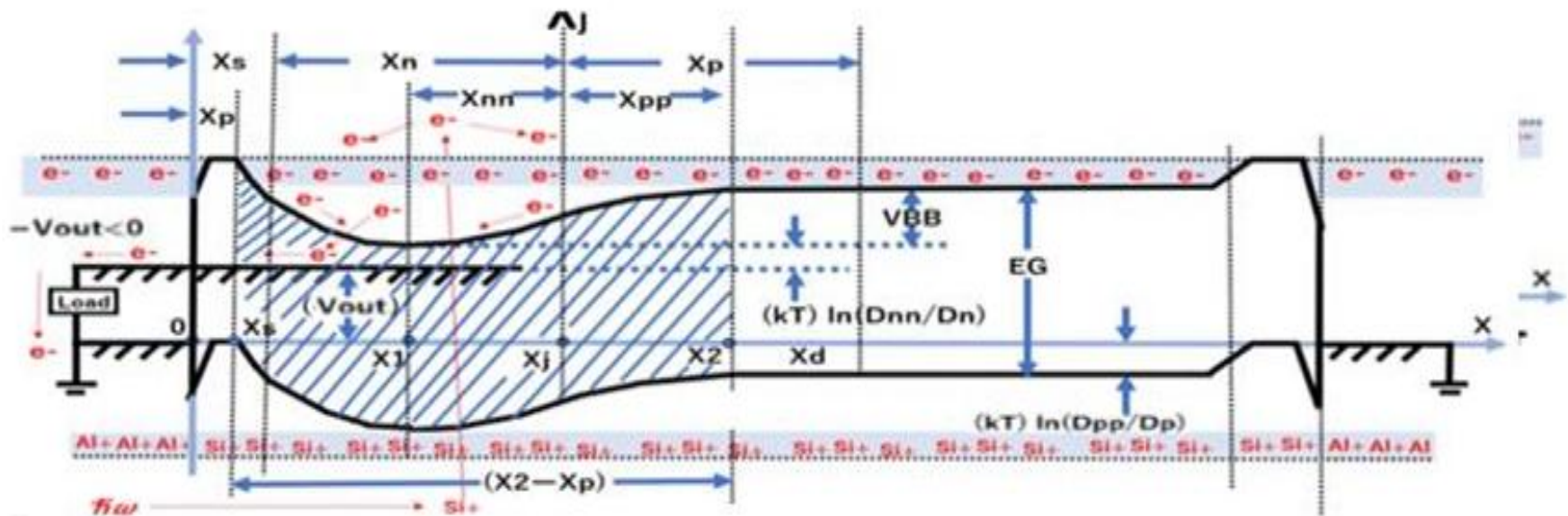
JPA2020-131313, Aug 1, 2020



Cross Sectional View of P+PNPP+ Double junction Solar Cell

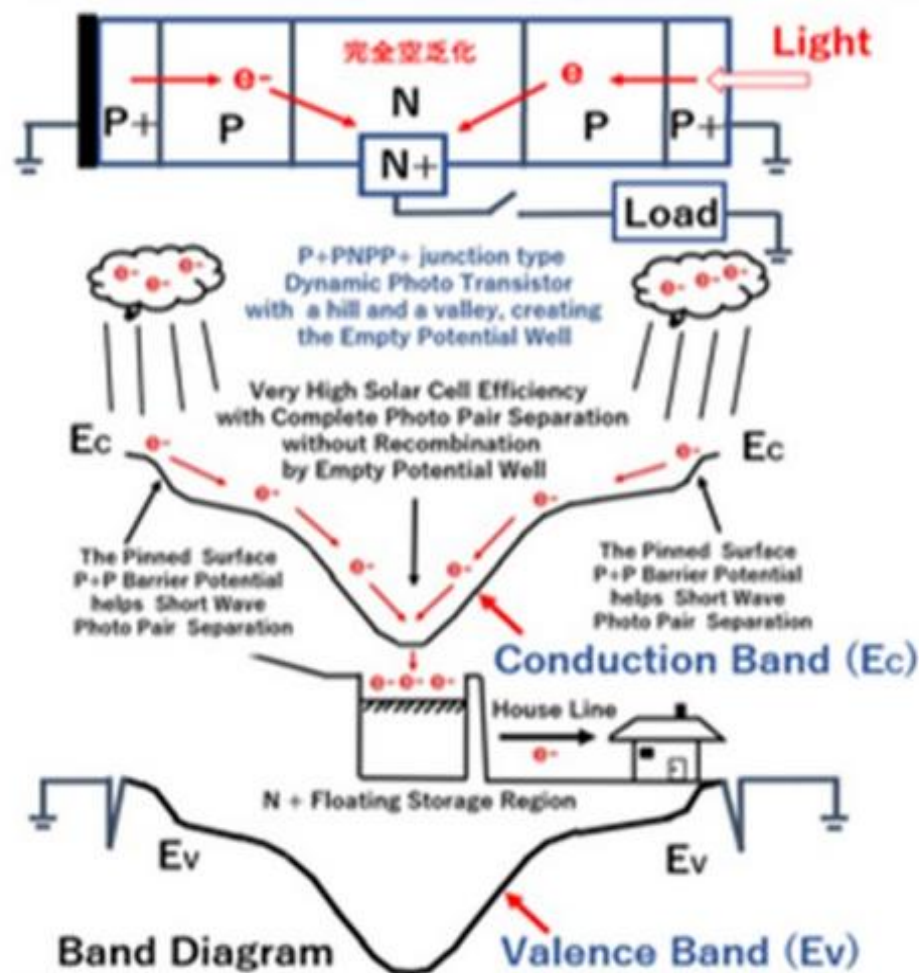


Band Diagram of P+PNPP+ Double junction Solar Cell

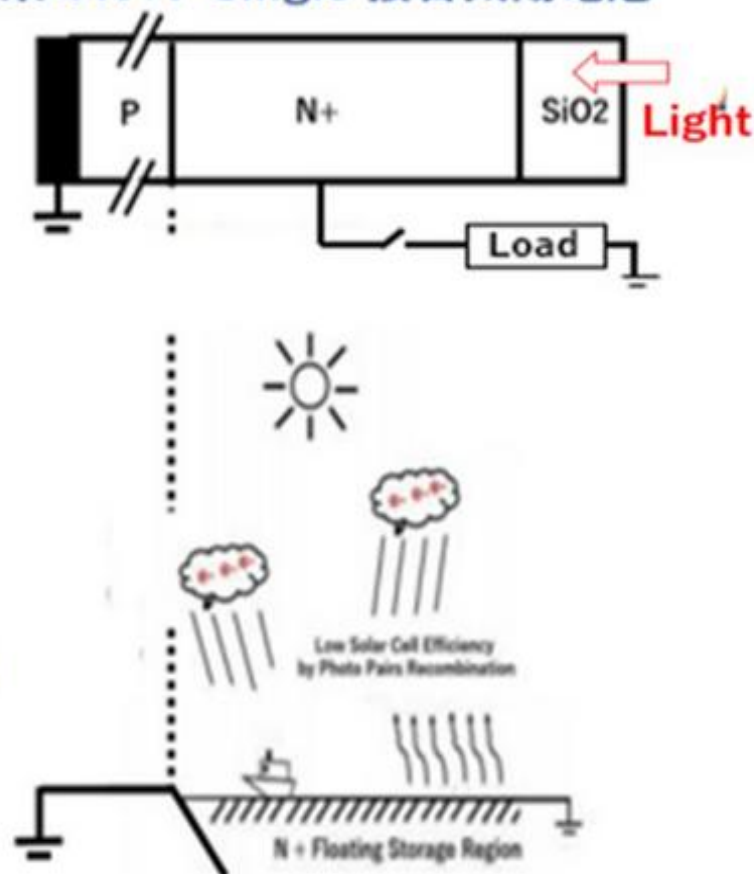


受光表面P+層と裏面のP+層の両面がピン留め接地された、P+PNPP+接合型新型太陽電池の提案

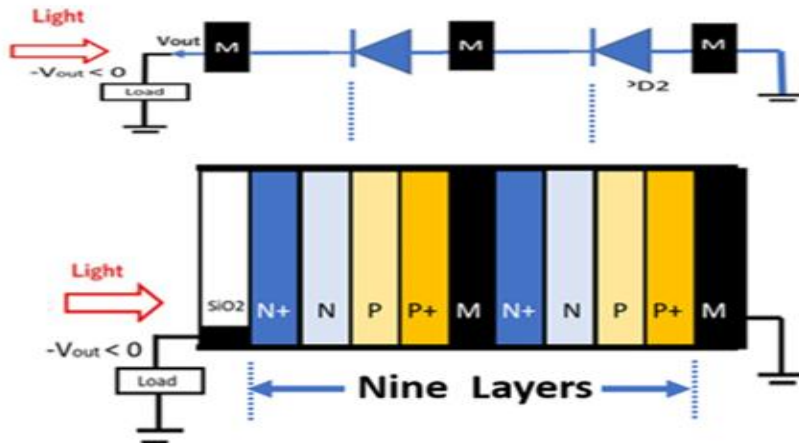
P+PN-PP+接合型太陽電池の提案



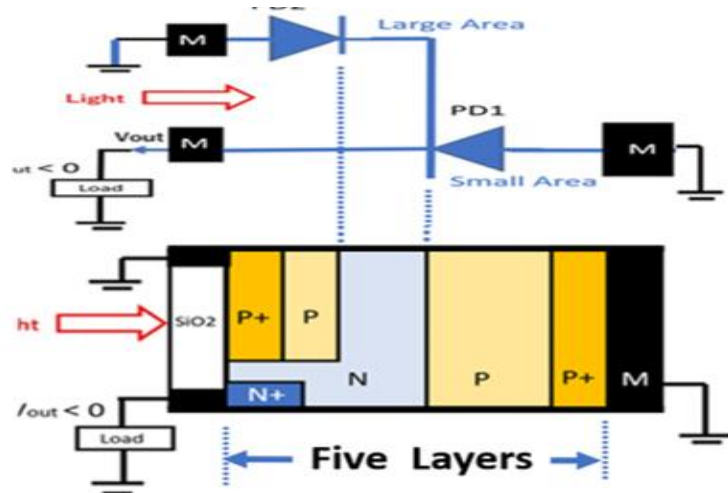
従来のN+P single 接合太陽電池



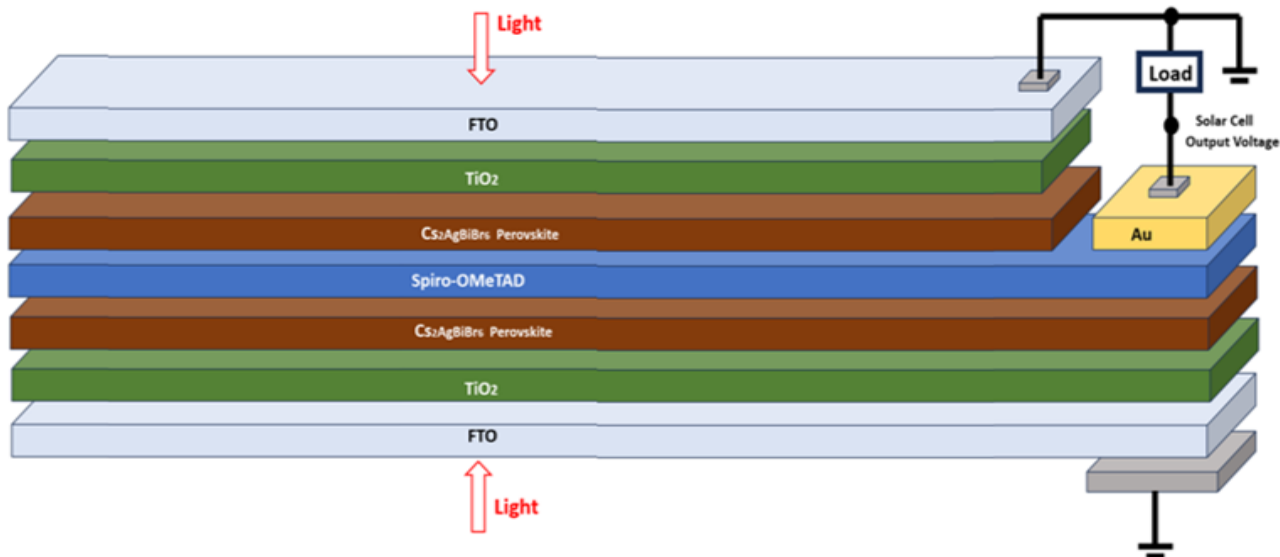
Tandem type Double Junction Nine Layers Process Solar Cell



Face-to-Face type Double Junction Five Layers Process Solar Cell



Double Junction type Perovskite Solar Cell



P+PNPP+ junction type Solar Cell

N+P junction type Solar Cell

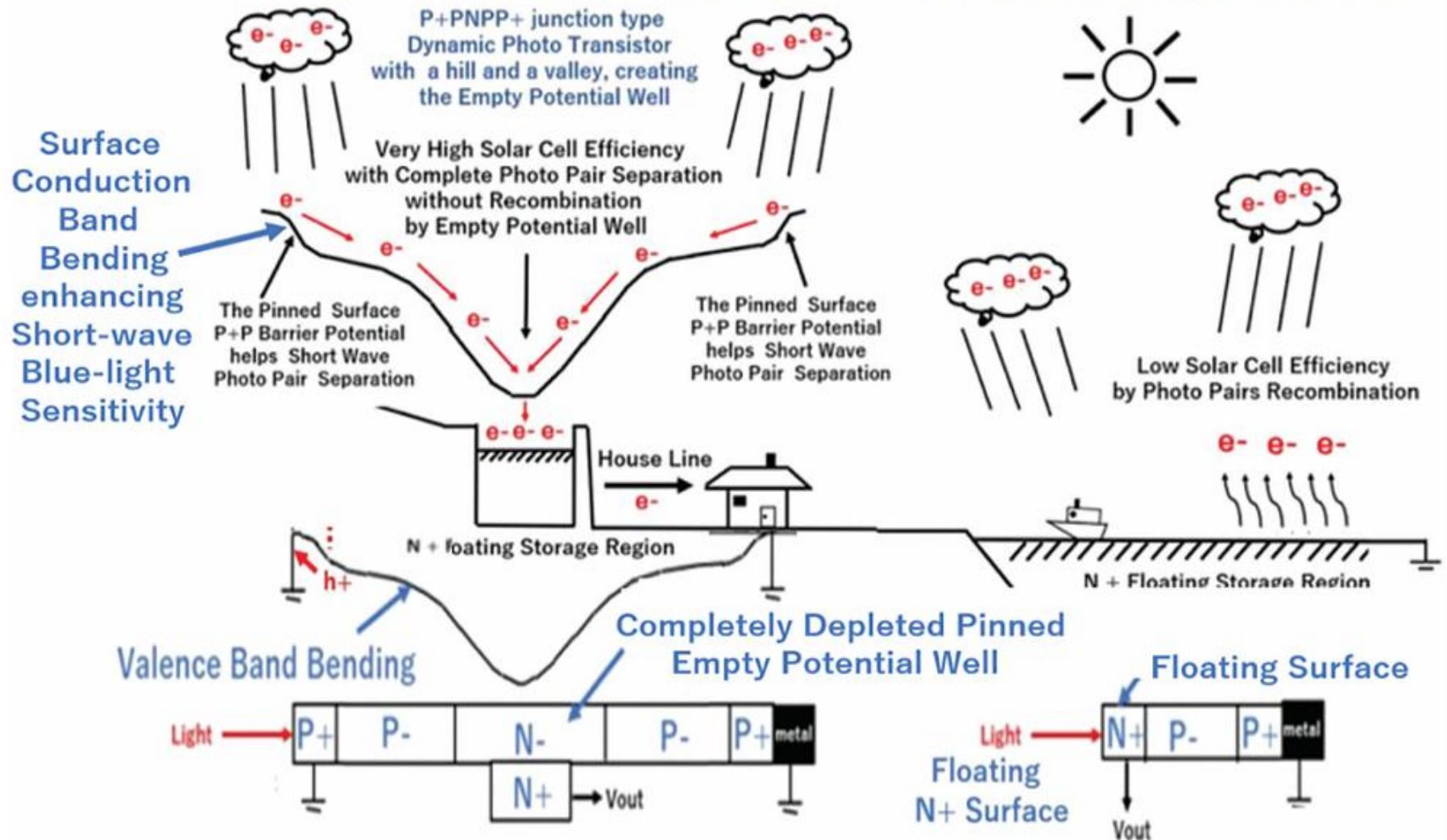
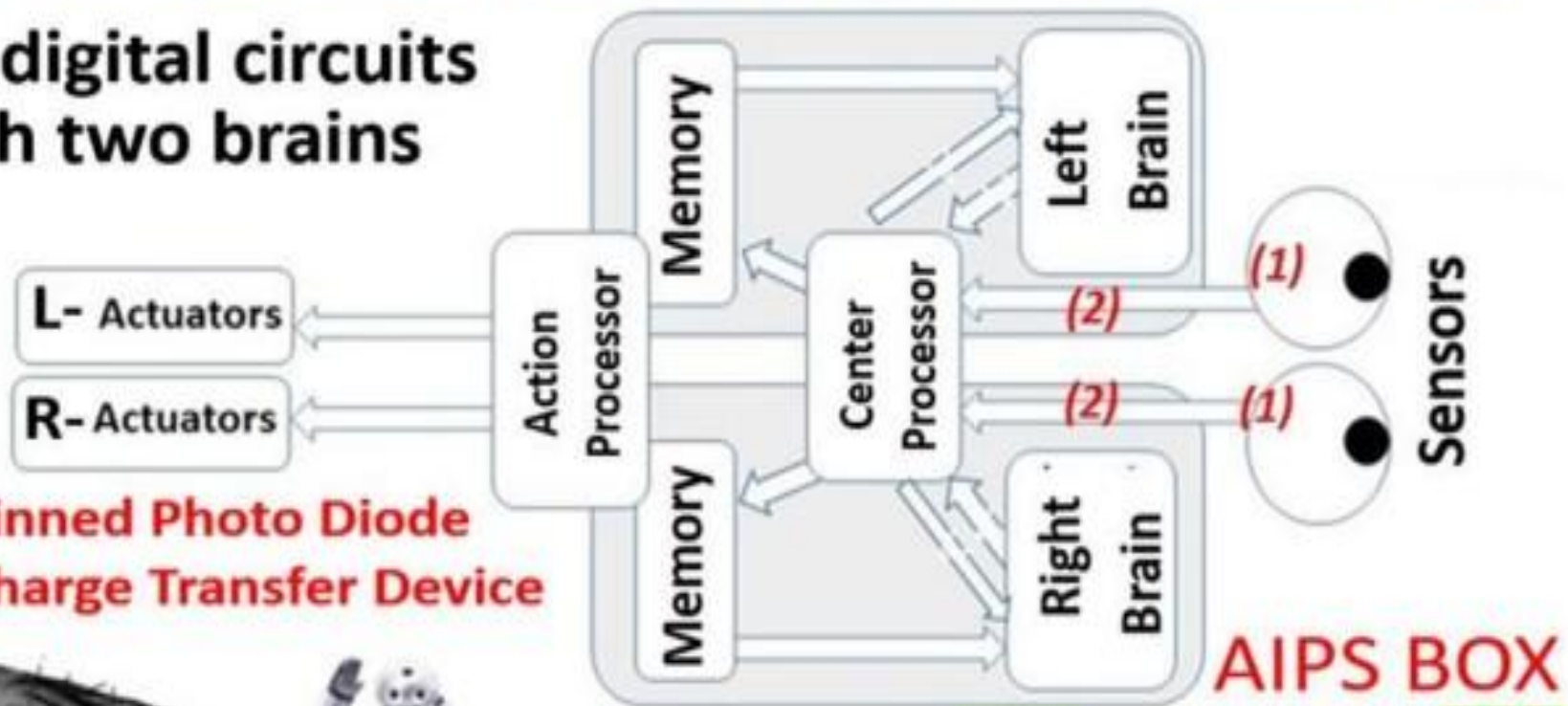


Fig. 11 The PNP double-junction PPD with the completely depleted N region and the floating N+ storage region has an excellent quantum efficiency (QE) for the blue-light. The floating-surface N+P single-junction-type photodiode has no surface electric field, where the photogenerated electron and hole pairs do not move and eventually they recombine with each other, resulting in a poor QE for the short-wave blue-light. 44

AIPS digital circuits with two brains



<https://ieeexplore.ieee.org/document/544383>

Yoshiaki Hagiwara.

Affiliation: SC Logic MCU Business Department, Sony Corporation, Atsugi, Japan

"High-density and high-quality frame transfer CCD imager with very low smear, low dark current, and very high blue sensitivity"

Published in: IEEE Transactions on Electron Devices.

Volume: 43, Issue: 12, December 1996, pp.2122-2130.

ABSTRACT:

When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of the threshold voltage is observed. This narrow channel effect has been applied successfully in creating an asymmetric potential well under an electrode for two-phase CCD operation. The feasibility of this structure has been confirmed in a 242-element analog delay line. The application is now extended to a 800 H/spl times/492 V frame transfer-type buried channel CCD imager with 14.31818 MHz frame shift, which results in a very low smear level of 0.01%, which is good enough for low-cost multimedia video camera applications.

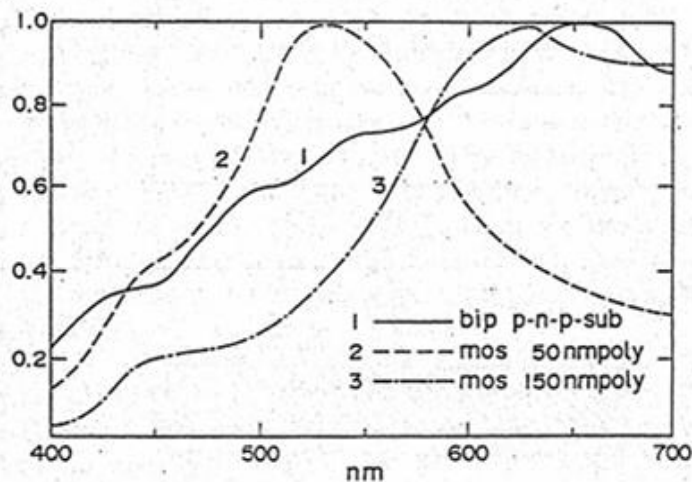
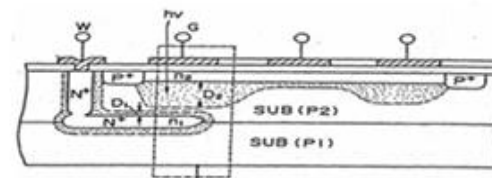


Fig. 7. Relative spectrum response. The relative response of the bipolar-type $\text{SiO}_2\text{-P2-N1-P1-SUB}$ structure is compared with $\text{poly-SiO}_2\text{-N2-P(SUB)}$ structures of the polysilicon thickness of 50 and 150 nm.

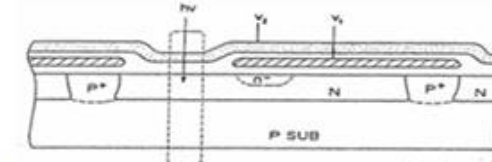
Early 1973

(3) mos 150nmpoly



Sony 1974

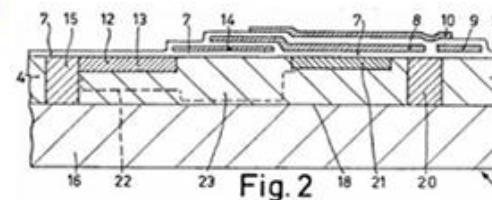
(2) mos 50nmpoly



Philips 1975

(1) bip p-n-p-sub

June 9, 1975

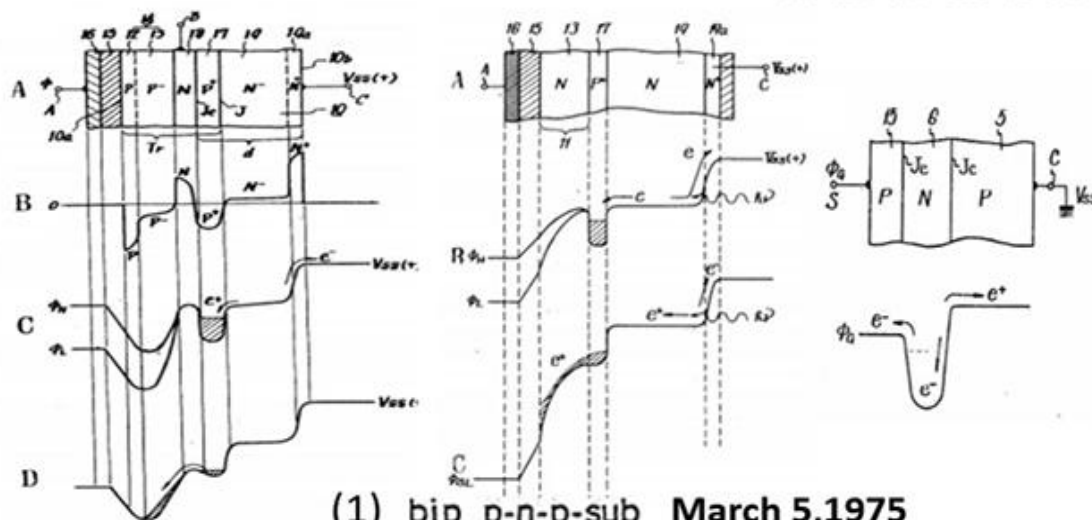


Sony (Hagiwara) March 5, 1975

JPA1975-127646

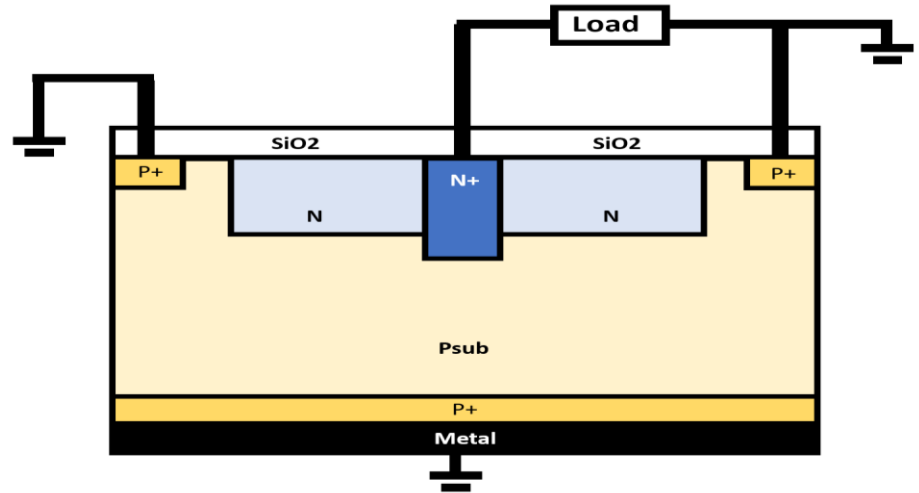
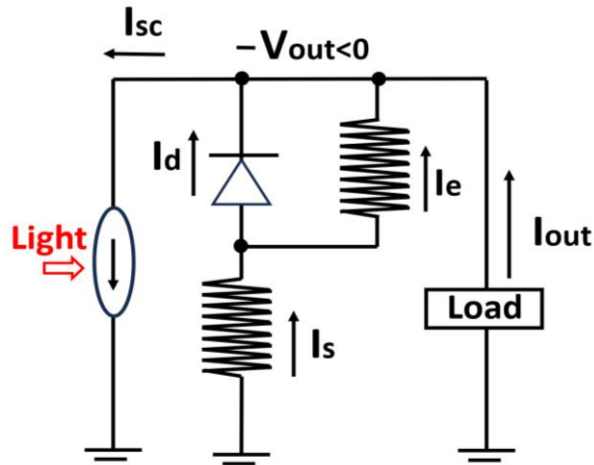
JPA1975-127647

JPA1975-134985



(1) bip p-n-p-sub March 5, 1975

(1) Conventional N+NPsubP+ Single Junction Solar Cell



(2) Pinned-Surface P+PNPsubP+ Double Junction Solar Cell with Buried-Channel Completely-Depleted Empty Potential Well

JPA2020-131313, Aug 1, 2020

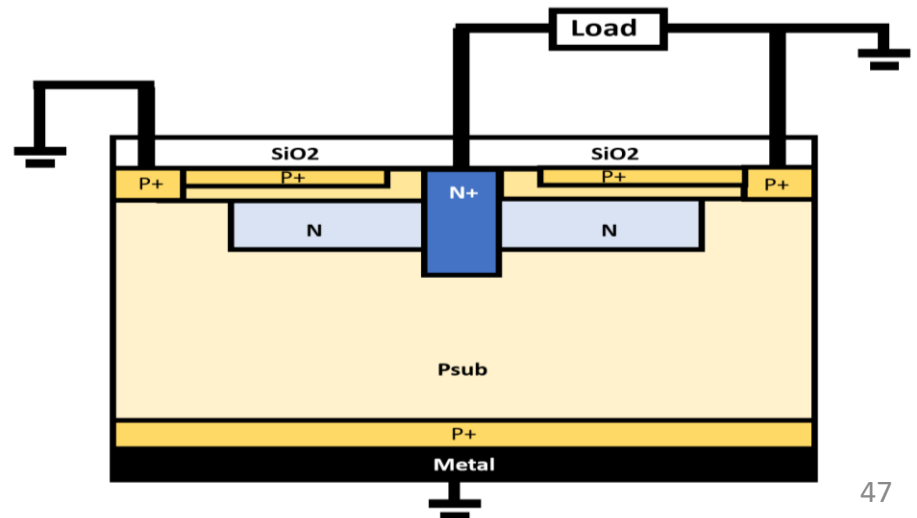
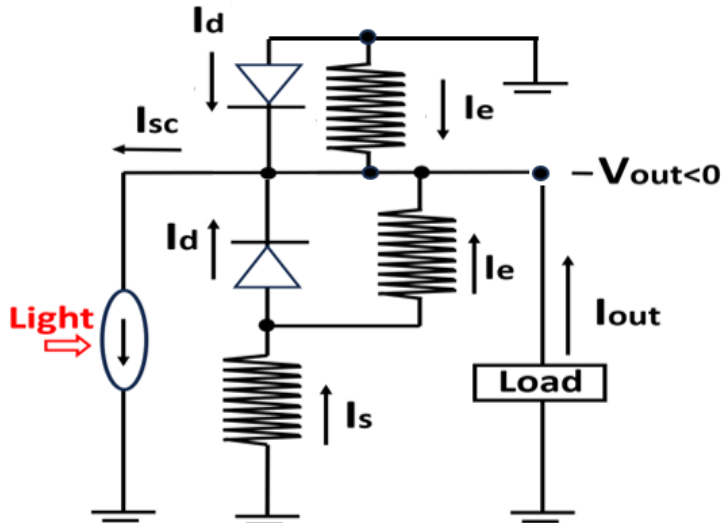


Image Sensor and Solar Cell in One Unit

- ### (1) P+PNPN+ Triple Junction Phototransistor

- ### (3) Memory and Processor

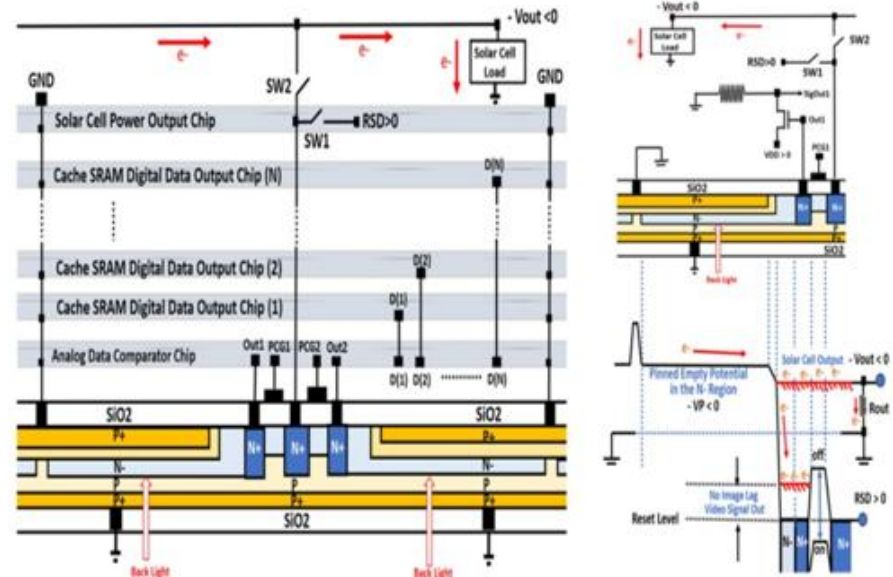


- ## (2) In-pixel ADC and Source-Follower Current AMP and Switching Gate Selector

- (1) P+PNPP+ Double Junction Phototransistor with Zero-resistance Pinned-Surface and Buried-Channel Empty Potential Well**

- ## (2) Switching Gate Selector

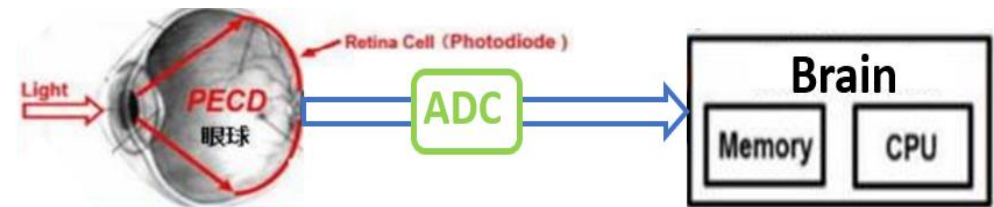
- ### (3) Output Loads (a) Solar Cell Unit and (b) Memory , Processor and Display Units



A cross-sectional view of our new AI Robot Vision chip in 3DIC multichip architecture

Introduction to AIPS

Fusion of Analog and Digital Semiconductor Device and Circuit Technology for Future AI Robot Applications



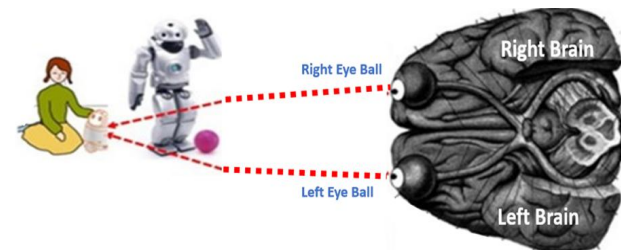
Introduction

Sensor and Analog Circuit Technology

Flash ADC and DFT Technology

Digital Circuit Technology

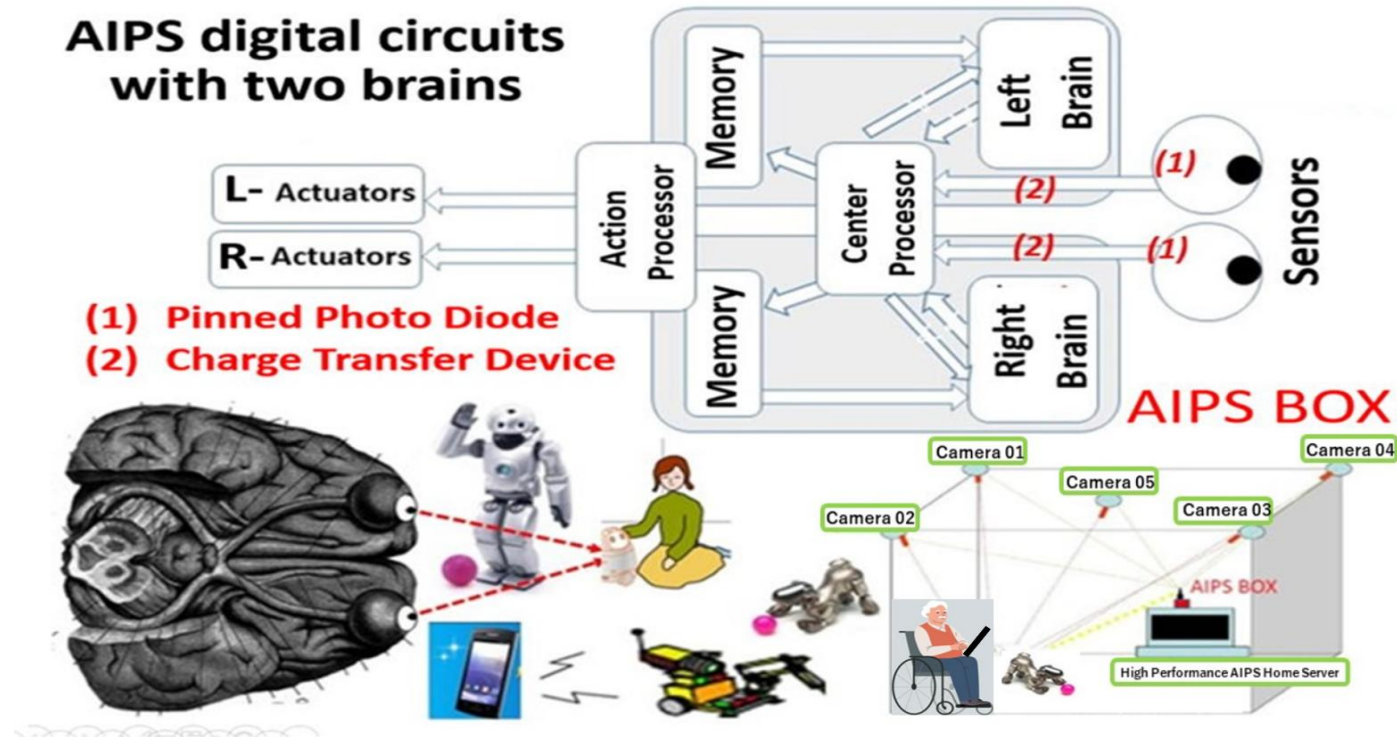
Conclusion



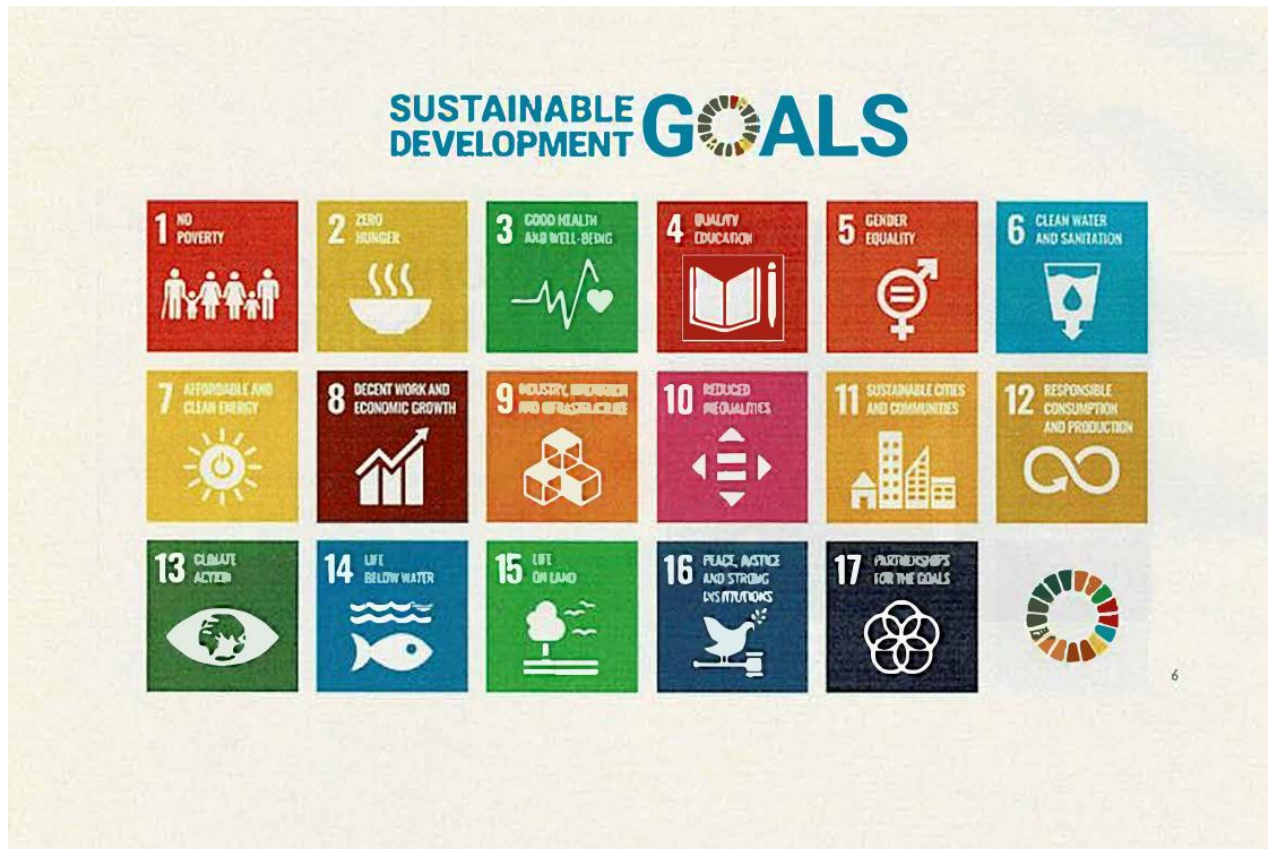
Introduction to AIPS

Concept of Artificial Intelligent Partner System (AIPS) proposed by Yoshiaki Hagiwara, May 2008

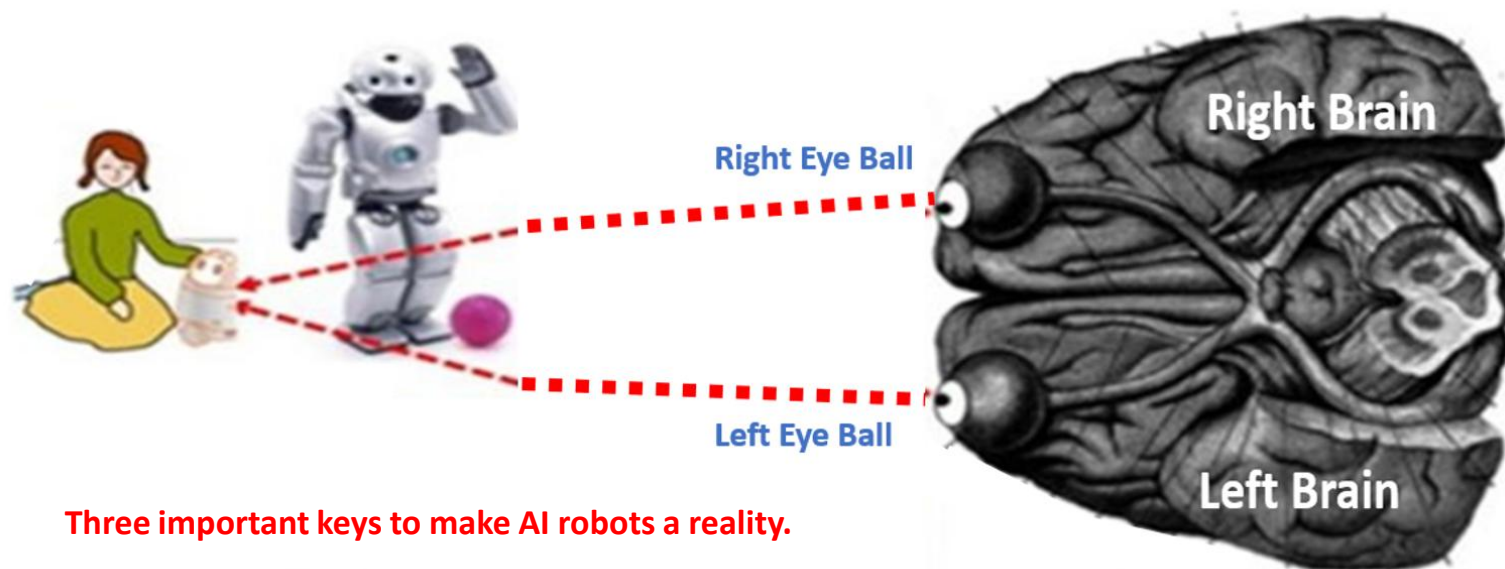
AIPS digital circuits with two brains



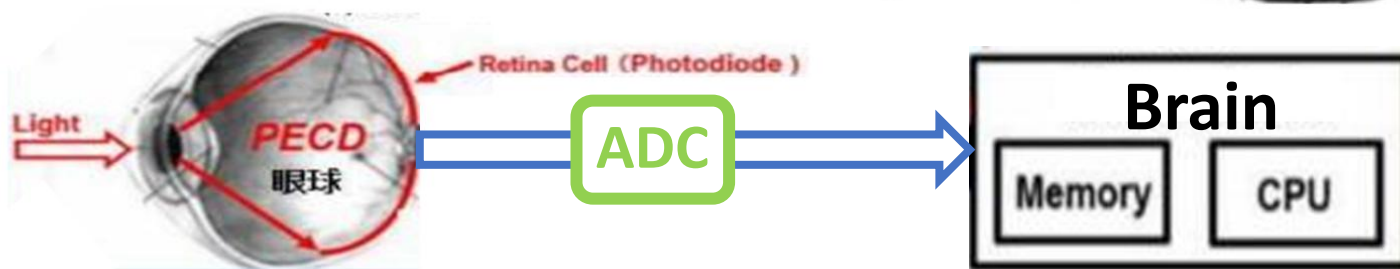
Introduction to AIPS



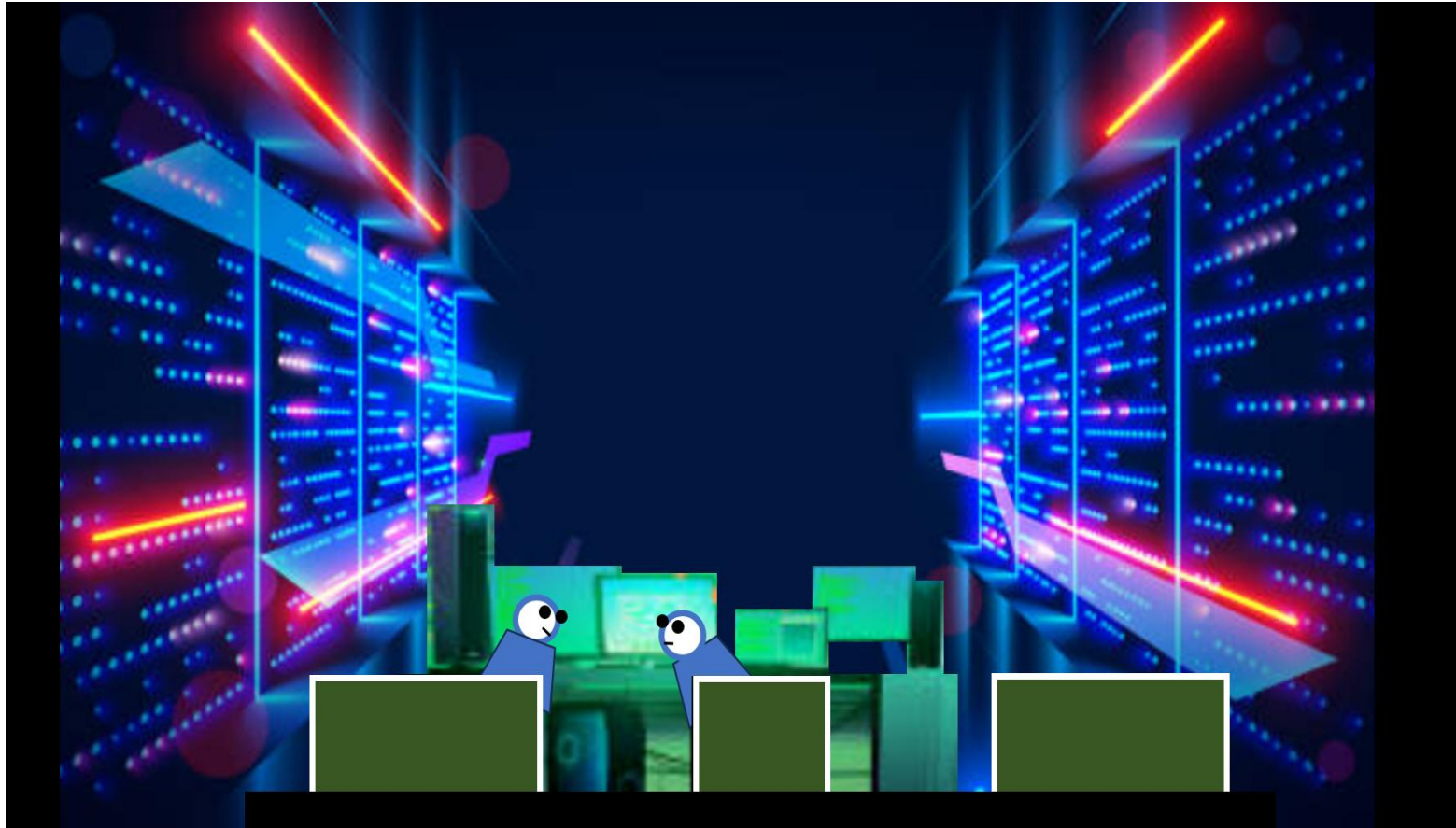
Introduction to AIPS



Three important keys to make AI robots a reality.



Introduction to AIPS

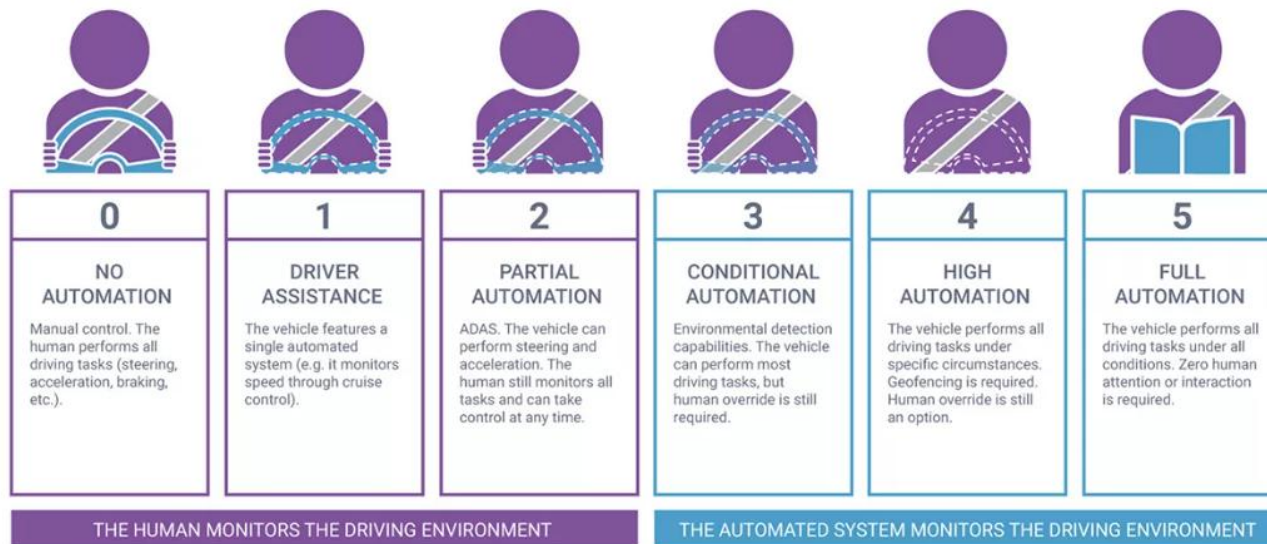


Introduction to AIPS

The 6 Levels of Vehicle Automation Explained | Synopsys Automotive

SYNOPSYS®

LEVELS OF DRIVING AUTOMATION



Introduction to AIPS

Nintendo First Generation Game Machine

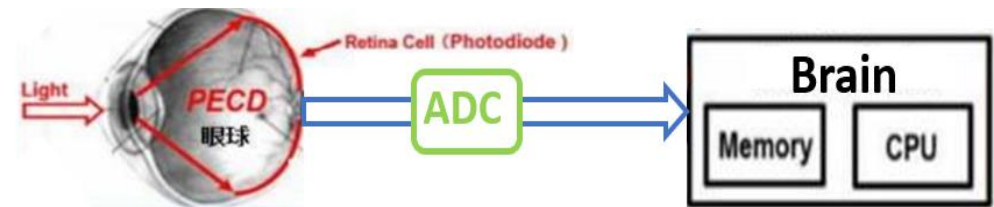


PlayStation 5 (CFI-2000A01)



Introduction to Semiconductor Device

Fusion of Analog and Digital Semiconductor Device and Circuit Technology for Future AI Robot Applications



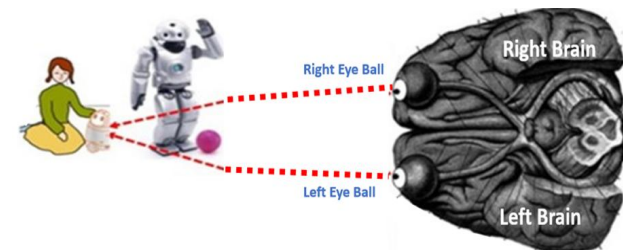
Introduction

Sensor and Analog Circuit Technology

Flash ADC and DFT Technology

Digital Circuit Technology

Conclusion

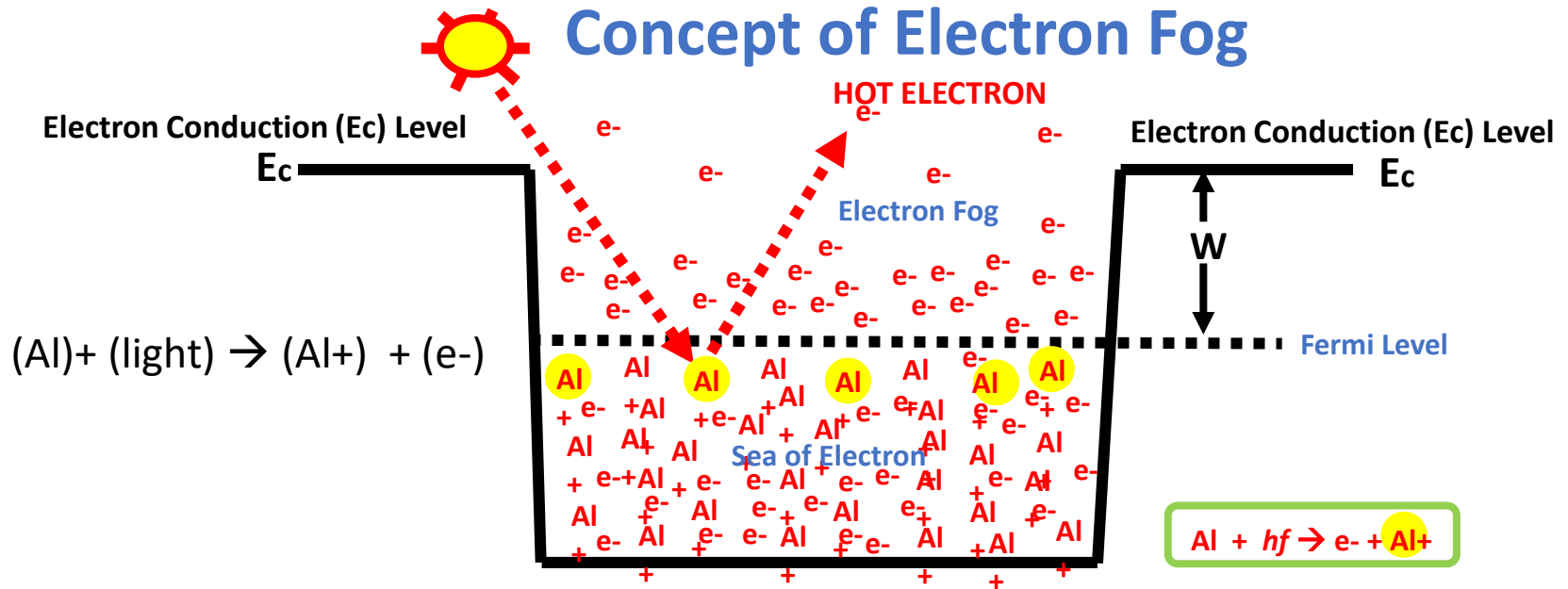


Introduction to Semiconductor Device

Physical Model of Metal



Concept of Electron Fog



Introduction to Semiconductor Device

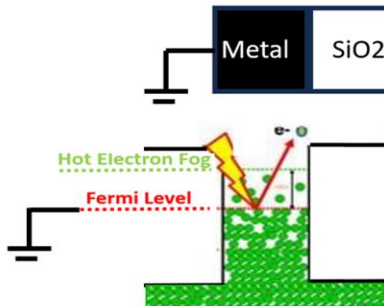
Concept of Four Vector in Einstein's Relativity was used to obtain the mass of electron (m_e)

Compton Effect, 1923

$$\Delta\lambda = \lambda_2 - \lambda_1 = \left(\frac{h}{m_e c} \right) (1 - \cos(\theta))$$

Beginning of Quantum Theory
and Physics of Semiconductor

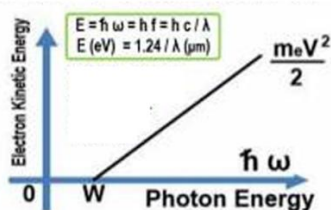
Metal/SiO₂



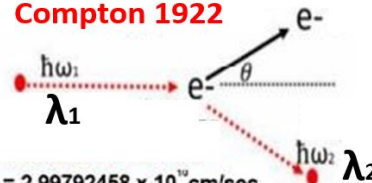
• = electron in Si atom or SiO₂ molecule



Einstein 1905



Compton 1922



$$\begin{aligned} c &= 2.99792458 \times 10^{10} \text{ cm/sec} \\ h &= 6.62606957 \times 10^{-34} \text{ Joule}\cdot\text{sec} \\ m_e &= 9.10938291 \times 10^{-31} \text{ kg} \end{aligned}$$

Compton Wave Length

$$\lambda_C = \left(\frac{h}{m_e c} \right)$$

$$\lambda_C = 2.426 \text{ pm}$$

$$1 \text{ pm} = 10^{-12} \text{ m}$$

Compton and Einstein received
Noble Prize by finding the
value of the Compton Wave length

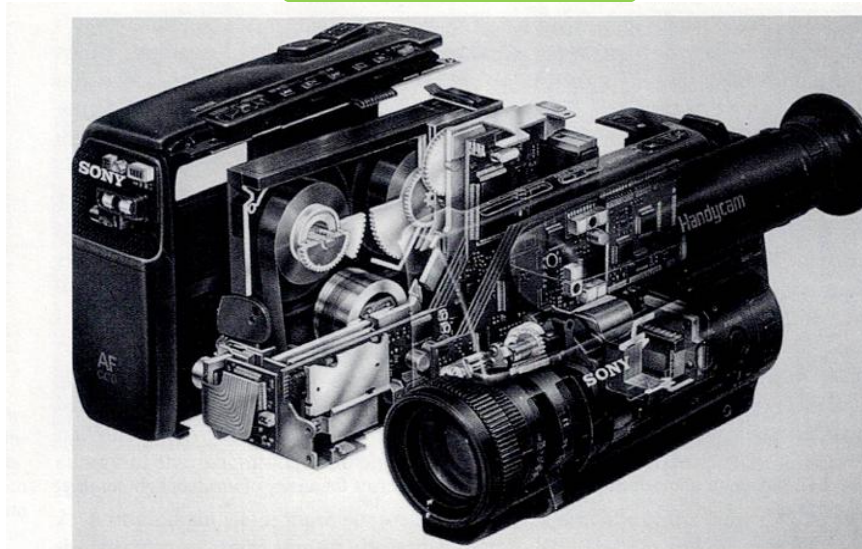
Introduction to Semiconductor Device

Concept of Four Vector in Einstein's Relativity is used to obtain the mass of electron (m_e)

Compton Effect, 1923

$$\Delta\lambda = \lambda_2 - \lambda_1 = \left(\frac{h}{m_e c} \right) (1 - \cos(\theta))$$

Beginning of Quantum Theory
and Physics of Semiconductor



Compton Wave Length

$$\lambda_C = \left(\frac{h}{m_e c} \right)$$

$$\lambda_C = 2.426 \text{ pm}$$

$$1 \text{ pm} = 10^{-10} \text{ m}$$

All light-sensitive detectors, including the eye and the one used in this video camera, are based on the absorption of energy from photons of light by electrons in the atoms the light falls on. (Courtesy Sony)

Ref: Author Beiser, Concepts of Modern Physics, McGraw-Hill, ISBN 0-07-004814-2, pp.62

Introduction to Semiconductor Device

Concept of Four Vector in Eistein's Relativity is used to obtain the mass of electron (me)

Concept of Four Vector in Eistein's Relativity

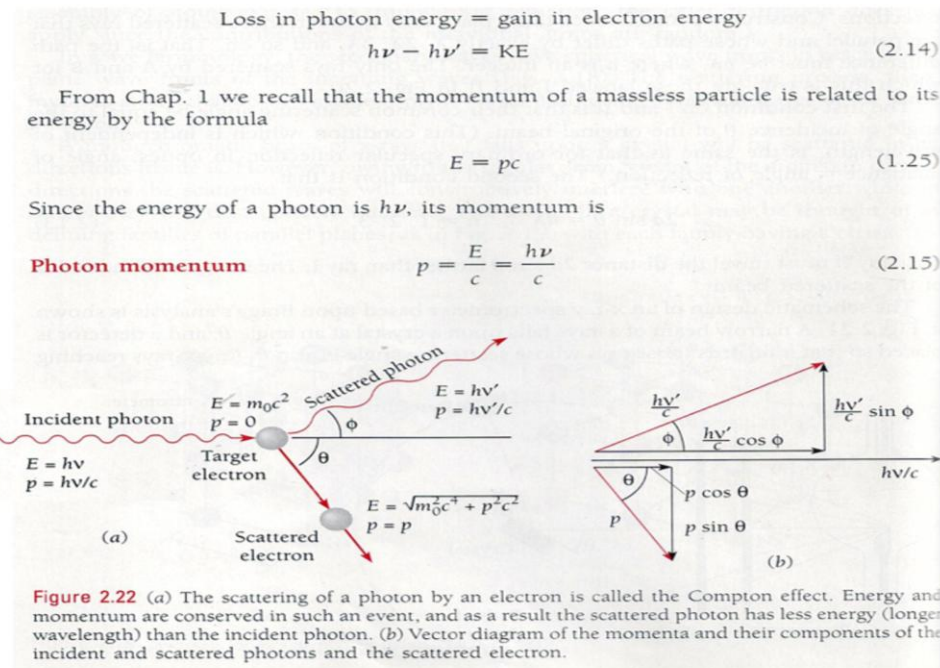
$$\begin{matrix} T' \\ X' \\ Y' \\ Z' \end{matrix} = \begin{matrix} \text{Lorentz} \\ 4 \times 4 \\ \text{Matrix} \end{matrix} \begin{matrix} T \\ X \\ Y \\ Z \end{matrix}$$

$$E = h\nu; P_x = hK_x;$$

$$P_y = hK_y; P_z = hK_z$$

$$w = 2\pi f = 2\pi c / \lambda = cK$$

$$\begin{matrix} E' \\ P_x' \\ P_y' \\ P_z' \end{matrix} = \begin{matrix} \text{Lorentz} \\ 4 \times 4 \\ \text{Matrix} \end{matrix} \begin{matrix} E \\ P_x \\ P_y \\ P_z \end{matrix}$$



Compton Wave Length

$$\lambda_C = \left(\frac{h}{m_e c} \right)$$

$$\lambda_C = 2.426 \text{ pm}$$

$$1 \text{ pm} = 10^{-12} \text{ m}$$

Ref: Author Beiser, Concepts of Modern Physics, McGraw-Hill, ISBN 0-07-004814-2, pp.62

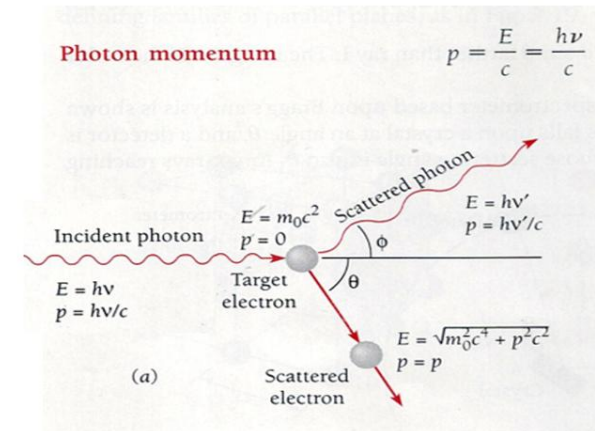
Introduction to Semiconductor Device



Argonne National Laboratory, AIP
Niels Bohr Library)

Arthur Holly Compton (1892–1962), a native of Ohio, was educated at College of Wooster and Princeton. While at Washington University in St. Louis he found that x-rays increase in wavelength when scattered, which he explained in 1923 on the basis of the quantum theory of light. This work convinced remaining doubters of the reality of photons; in fact, Compton himself coined the word “photon.”

length λ_C . Because $\lambda_C = 2.426$ pm for an electron, and even less for other particles owing to their larger rest masses, the maximum wavelength change in the Compton effect is 4.852 pm. Changes of this magnitude or less are readily observable only in x-rays: the shift in wavelength for visible light is less than 0.01 percent of the initial wavelength, whereas for x-rays of $\lambda = 0.1$ nm it is several percent. The Compton effect is the chief means by which x-rays lose energy when they pass through matter.



Compton Wave Length

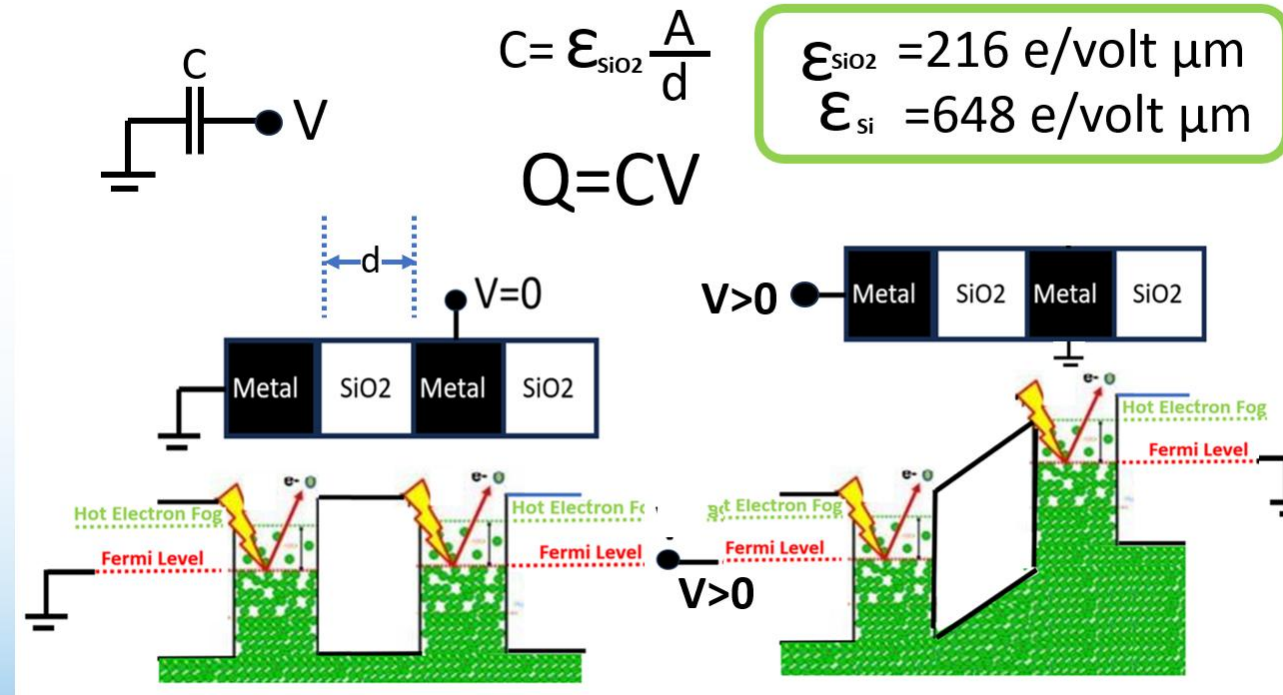
$$\lambda_C = \left(\frac{h}{m_e c} \right)$$

$$\lambda_C = 2.426 \text{ pm}$$

$$1 \text{ pm} = 10^{-12} \text{ m}$$

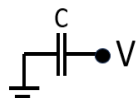
Introduction to Semiconductor Device

Physical Model of Capacitor



Introduction to Semiconductor Device

Physical Model of Capacitor

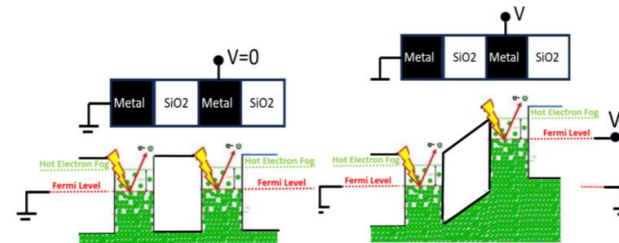


$$C = \epsilon_{\text{SiO}_2} \frac{A}{d}$$

$$Q = CV$$

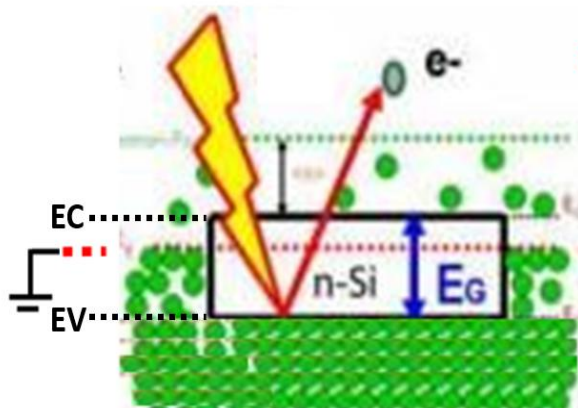
$$\epsilon_{\text{SiO}_2} = 216 \text{ e/volt } \mu\text{m}$$

$$\epsilon_{\text{Si}} = 648 \text{ e/volt } \mu\text{m}$$



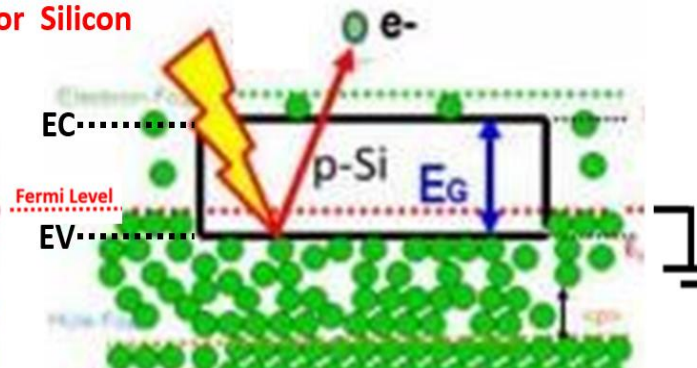
Physical Model of Semiconductor

n-type silicon



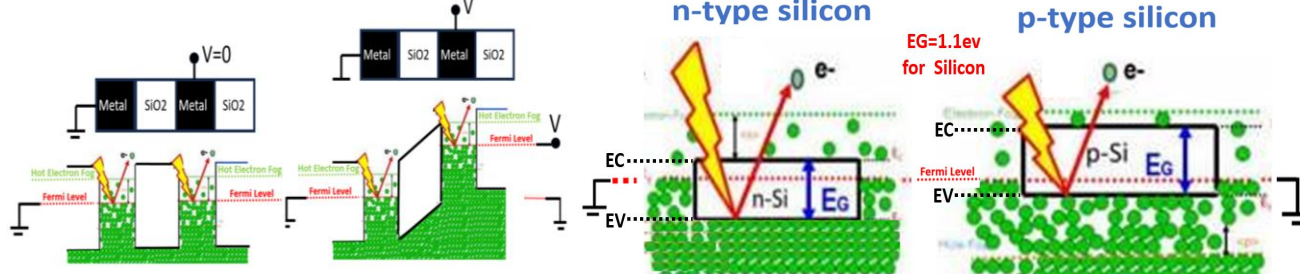
$E_g = 1.1 \text{ eV}$
for Silicon

p-type silicon

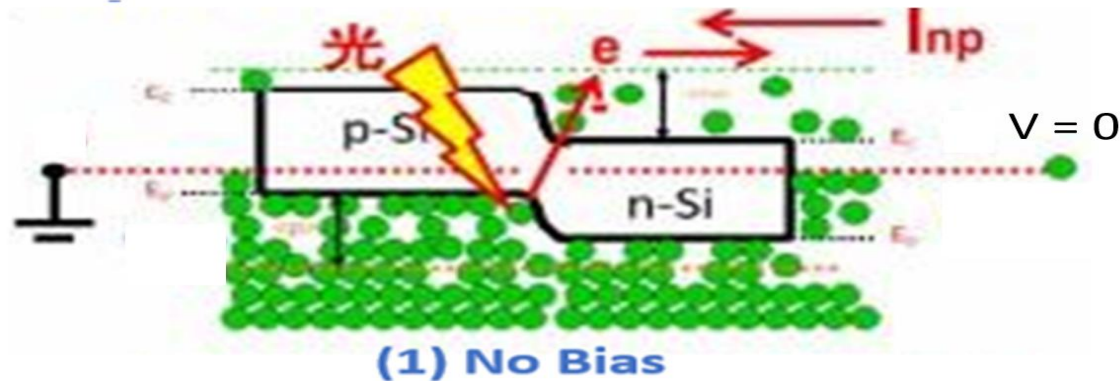


Introduction to Semiconductor Device

Physical Model of Capacitor

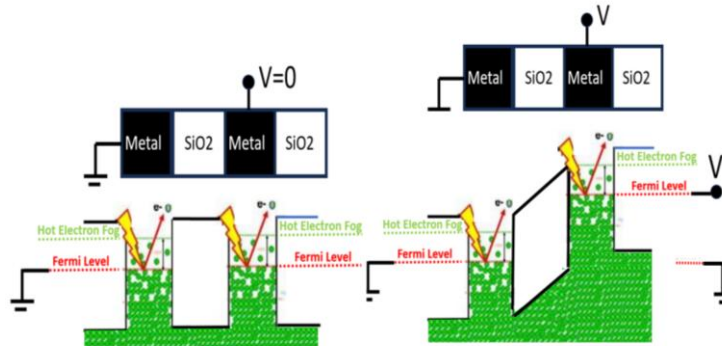


Physical Model of Silicon PN Single Junction

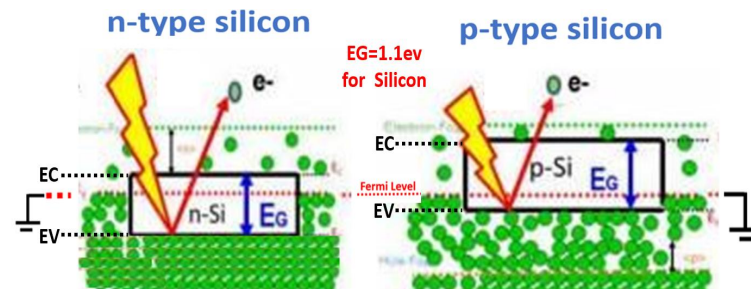
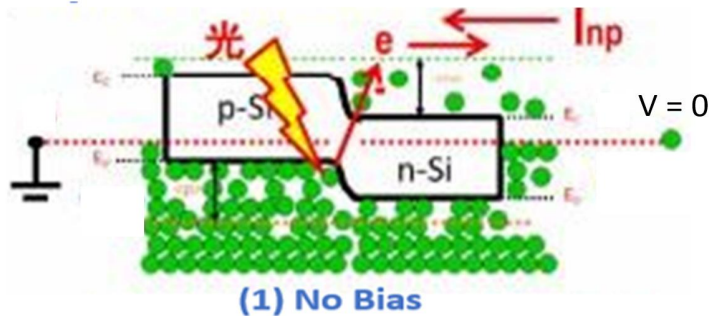


Introduction to Semiconductor Device

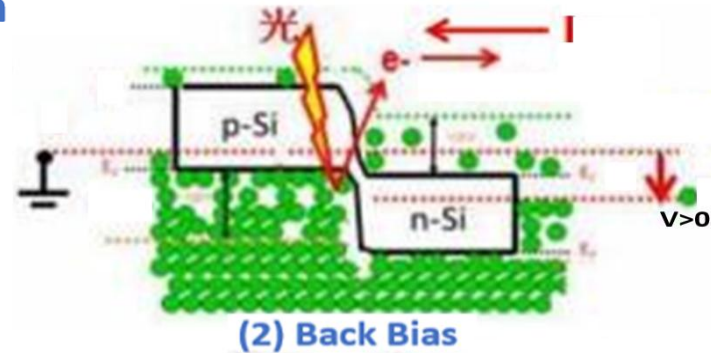
Physical Model of Capacitor



Physical Model of Silicon PN Single Junction

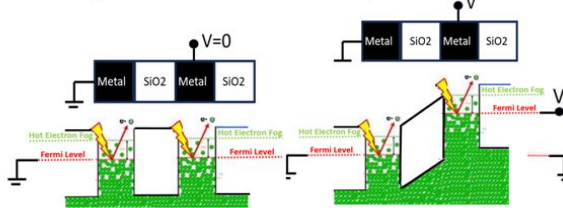


Back Bias Current is Small

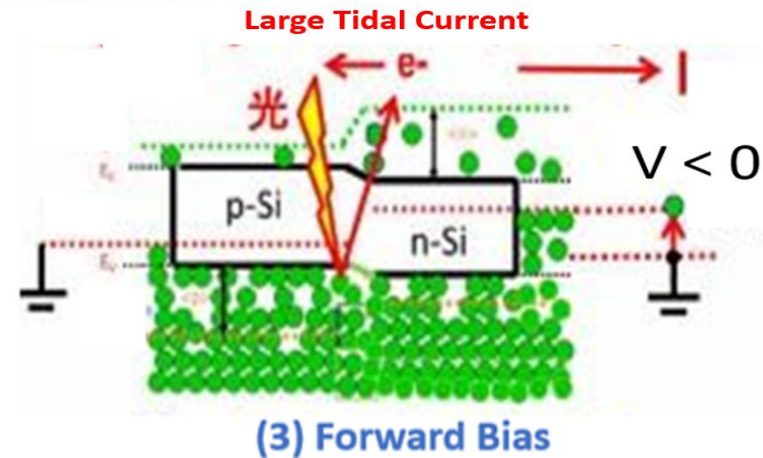
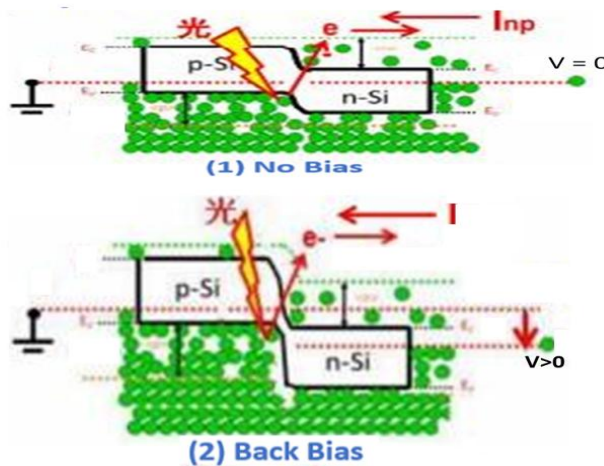


Introduction to Semiconductor Device

Physical Model of Capacitor

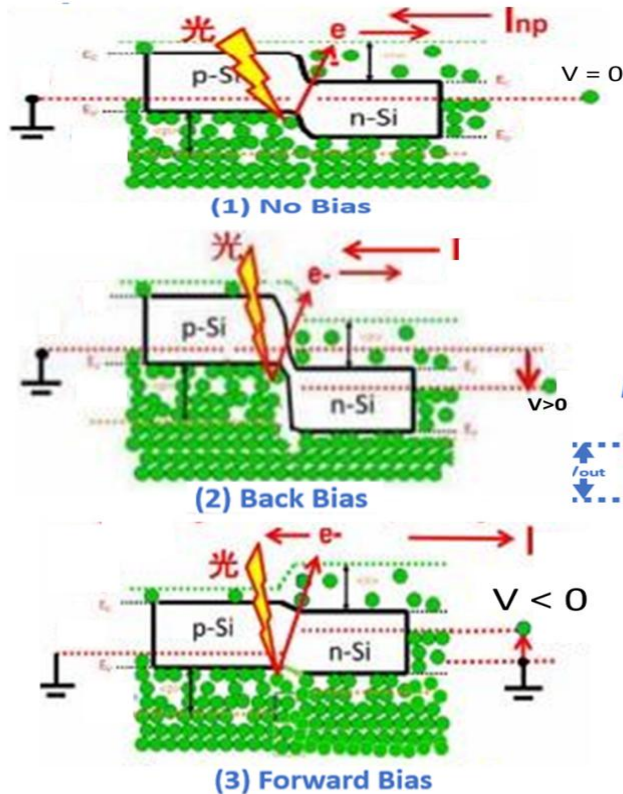


Physical Model of Silicon PN Single Junction

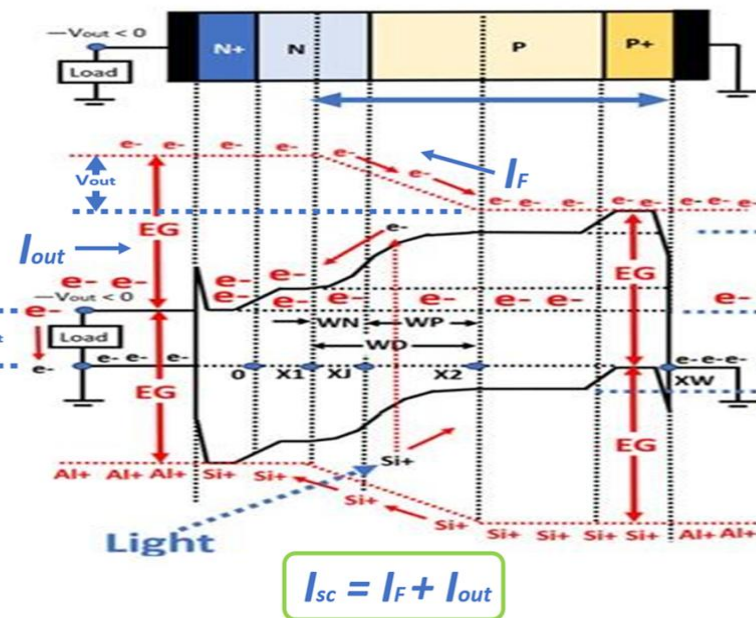


Introduction to Semiconductor Device

Physical Model of Silicon PN Single Junction

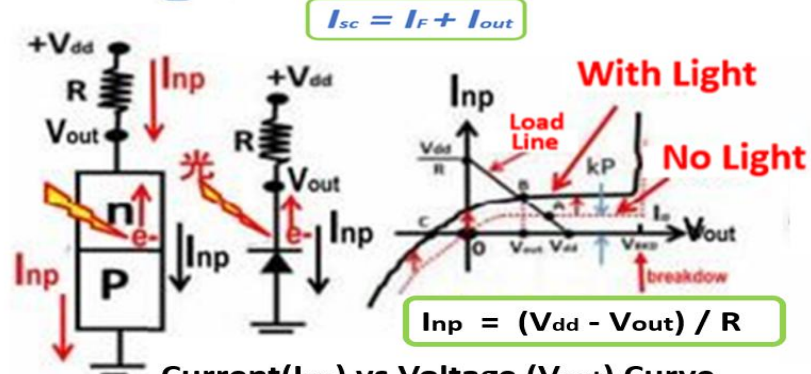
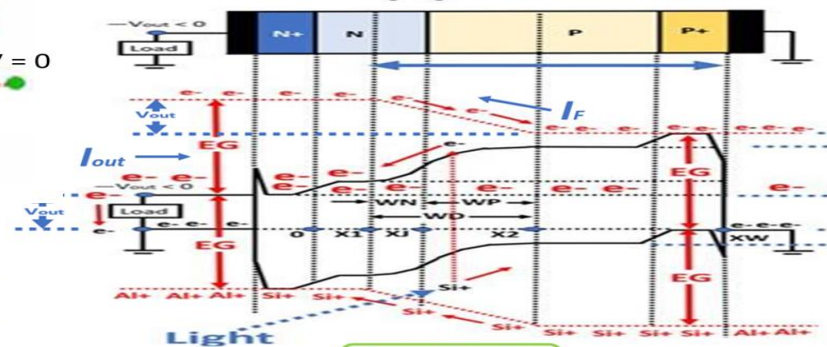
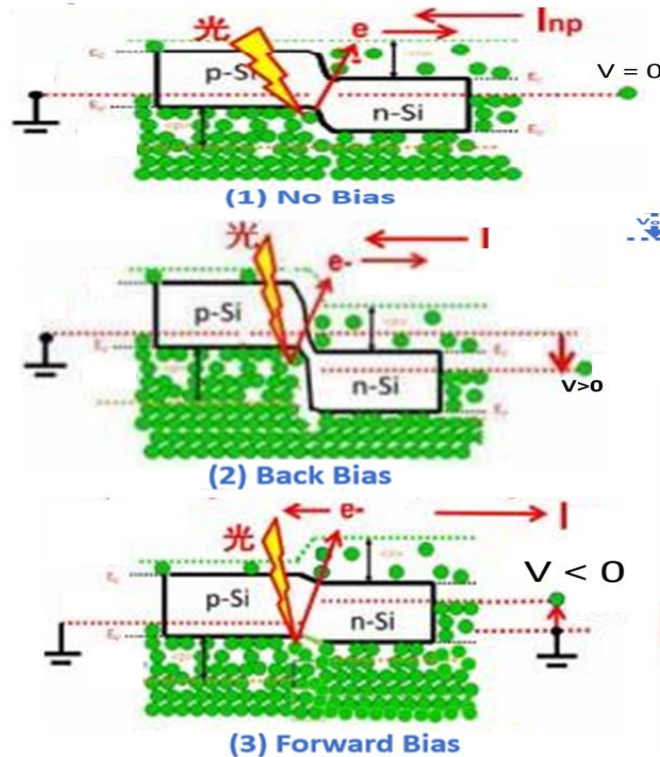


A Band Diagram of a conventional N+NPP+ single junction type solar cell.



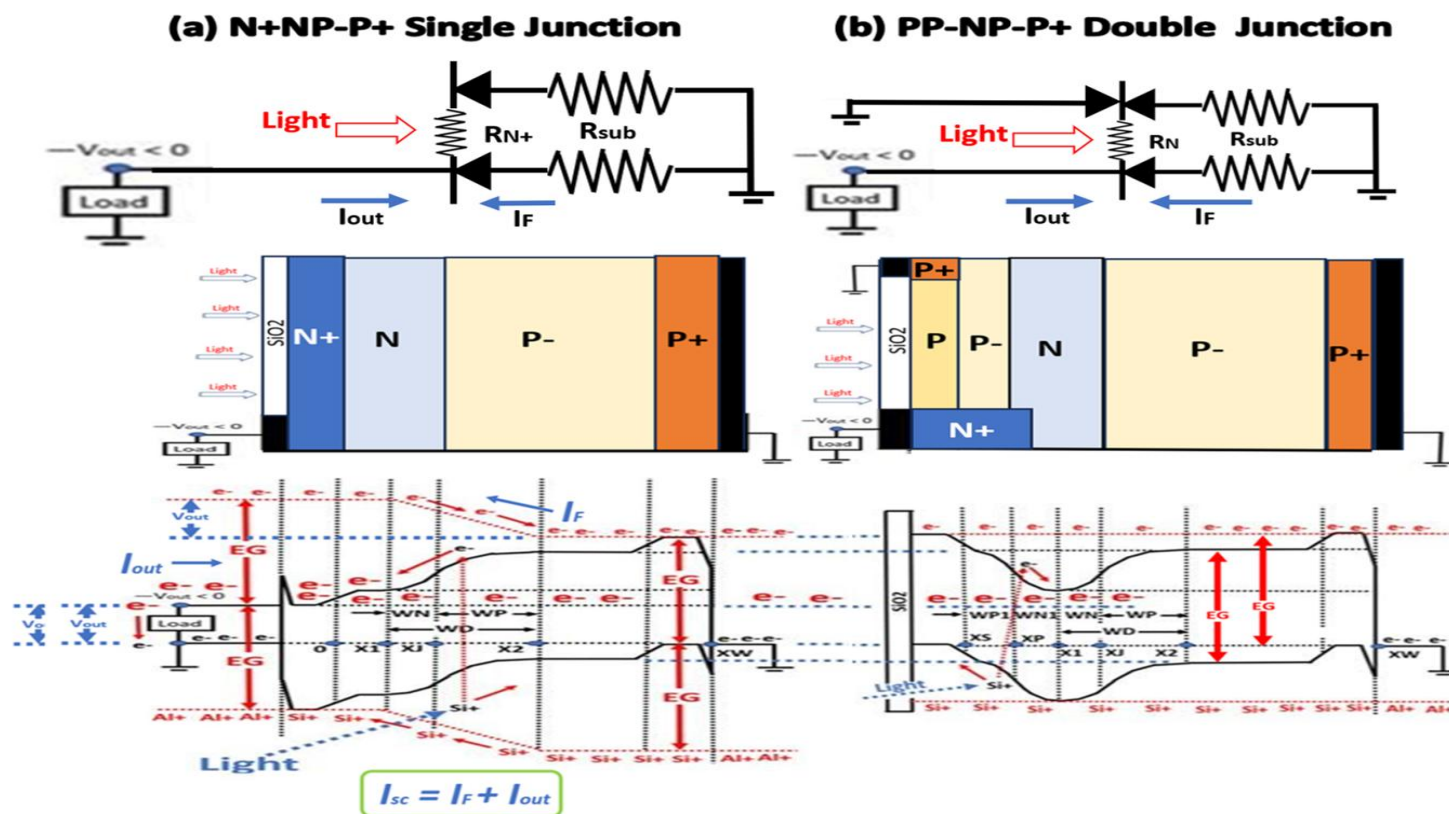
Introduction to Semiconductor Device

Physical Model of Silicon PN Single Junction



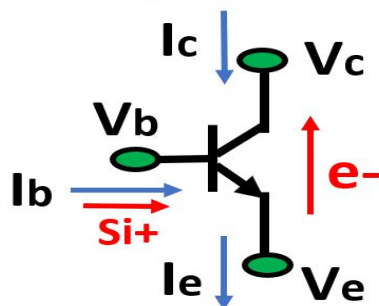
Current(I_{np}) vs Voltage (V_{out}) Curve of PN Junction Photodiode with Resistive Load Line

Introduction to Semiconductor Device

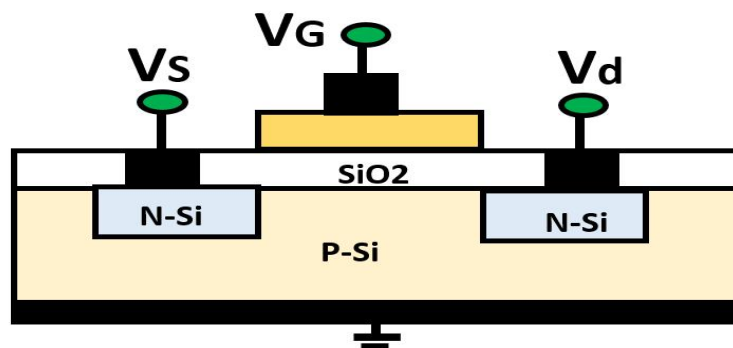
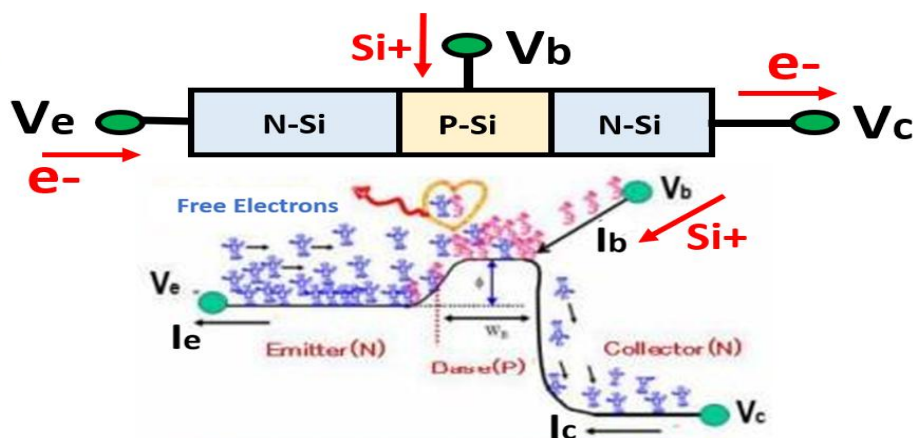
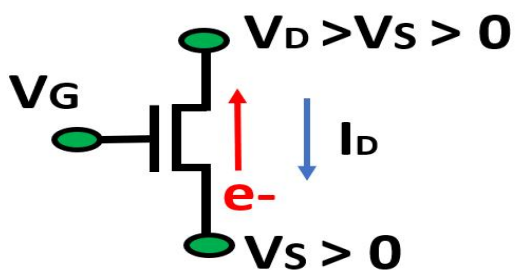


Introduction to Semiconductor Device

NPN Bipolar Transistor



NMOS Transistor



Introduction to Semiconductor Device

CHRONOLOGY OF SILICON-BASED IMAGE SENSOR DEVELOPMENT

Yoshiaki Daimon Hagiwara, IEEE Life Fellow
Sojo University, Kumamoto-city, Japan

The first PNP Double Junction Photodiode invented by Philips on March 9, 1975, with an image lag problem, caused by a RC delay time between the floating surface and the high-resistivity pinned back substrate.

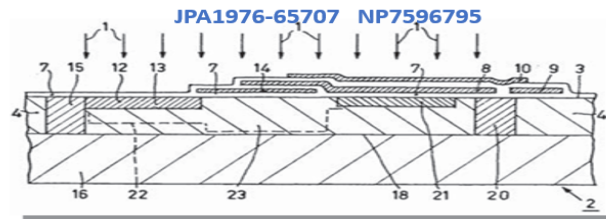


Figure 6. The double junction type buried photodiode image sensor reproduced from Netherland Patent Application NPA [6]

[6] Japanese Patent Application JPA1976-65707 (Patent No. 7596795, filed on June 9, 1975, Netherland)

[7] Y. Hagiwara, Japanese Patent Application JPA 1975-127646 on N+NP+NP-P+Triple Junction Type Pinned Photodiode with Back Light Illumination with the CCD type MOS capacitor Buffer Memory for Global Shutter Function.

Philips, March 9, 1975

The first Pinned-surface PNP Double Junction type and the first Pinned-surface Triple Junction type Photodiodes, both invented by Sony (Hagiwara) on Oct 23, 1975, with Vertical Overflow Drain (VOD) function, Electric Shutter function and Global Shutter function with MOS-Capacitor Buffer Memory that created our new digital imaging and TV era.

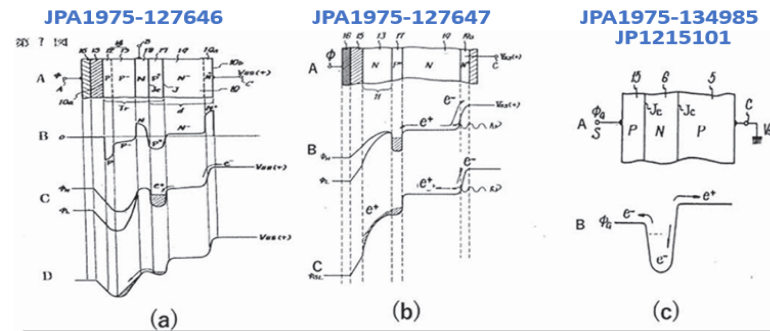


Figure 2. Reproductions from the Japanese Patent Applications of (a) the N+NP+NP-P triple junction PPD, (b) the N+NP+NP double junction PPD, and (c) the PNP double junction PPD

Sony, Oct 23, 1975

https://eds.ieee.org/images/files/newsletters/Newsletter_Jan23.pdf See pp.22-31

Introduction to Semiconductor Device

N+P+ Tunnel Diode
invented in Aug 1957
by Tetsuro Tsukamoto,
Yuriko Kurose and
analyzed theoretically
by Reona Esaki

CHRONOLOGY OF SILICON-BASED IMAGE SENSOR DEVELOPMENT

Yoshiaki Daimon, Hagiwara, IEEE Life Fellow
Sojo University, Kumamoto-city, Japan

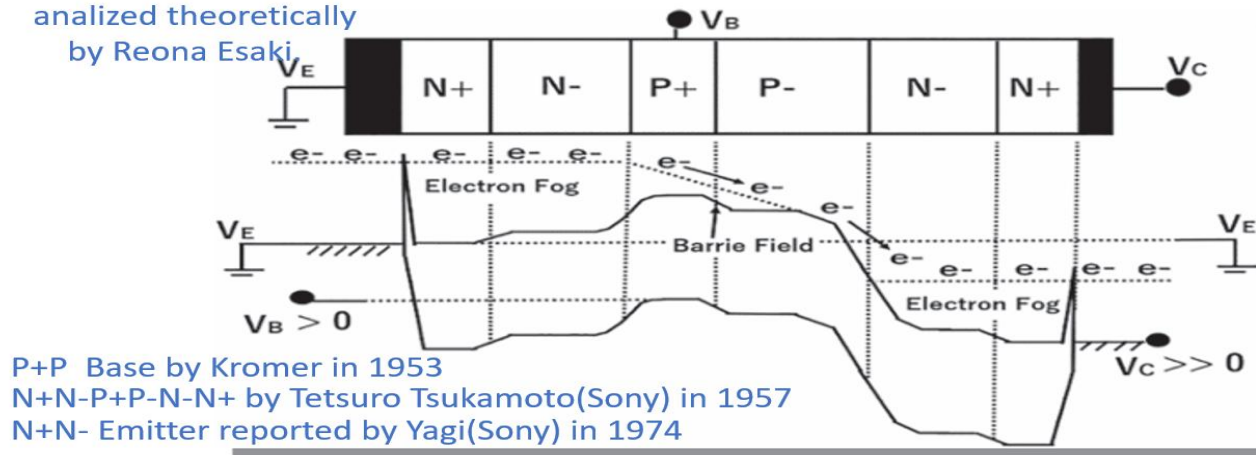


Figure 1: The drift-field transistor for high frequency operations, invented by Herbert Kroemer in 1953.

See also: Yagi H, Tsuyuki T, Koma K, Miyazawa Y. A novel bipolar device with low emitter impurity concentration structure. In *1974 International Electron Devices Meeting (IEDM)*, Washington, USA, December 9–11, 1974, pp. 262–265.

https://eds.ieee.org/images/files/newsletters/Newsletter_Jan23.pdf See pp.22-31

Introduction to Semiconductor Device

The First PNP double junction photodiode, pinned to the substrate with Serious RC delay and Image lag Problem.

Charge Transfer Gate(CTG) is BCCD/Depletion type with Negative Threshold Voltage (V_{th}).

CHRONOLOGY OF SILICON-BASED IMAGE SENSOR DEVELOPMENT

Yoshiaki Daimon Hagiwara, IEEE Life Fellow
Sojo University, Kumamoto-city, Japan

In IEDM1982 NEC reported the same PNP double junction with SCCD/Enhancement type Charge Transfer Gate(CTG).

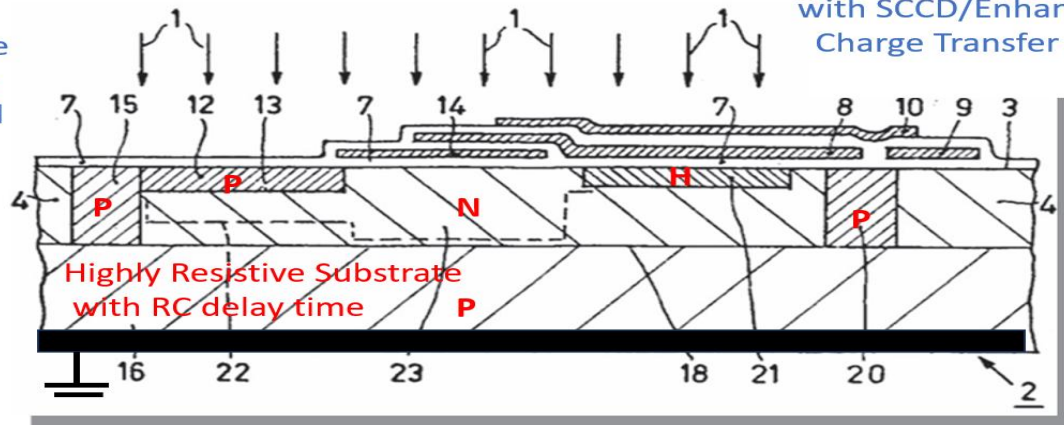


Figure 6: The double junction type buried photodiode image sensor reproduced from Netherland Patent Application NPA [6].

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[6] Japanese Patent Application JPA1976-65707 (Patent No. 7596795, filed on June 9, 1975, Netherland)

https://eds.ieee.org/images/files/newsletters/Newsletter_Jan23.pdf See pp.22-31

Introduction to Semiconductor Device

The First NPN triple Junction photodiode, pinned to the substrate.

CHRONOLOGY OF SILICON-BASED IMAGE SENSOR DEVELOPMENT

Yoshiaki Daimon Hagiwara, IEEE Life Fellow
Sojo University, Kumamoto-city, Japan

JPA1975-127646, Oct 23, 1975

JPA1975-127647, Oct 23, 1975

JPA1975-134985, Nov 10, 1975

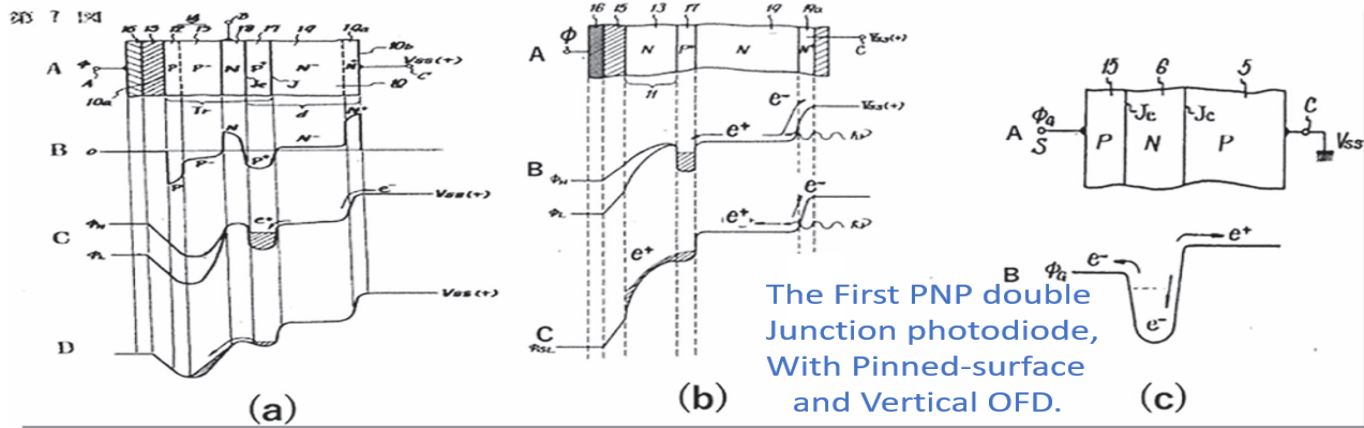


Figure 2: Reproductions from the Japanese Patent Applications of (a) the N+N-P+NP-P triple junction PPD, (b) the N+N-P+N double junction PPD, and (c) the PNP double junction PPD.

22 IEEE Electron Devices Society Newsletter ○ January 2023

[7] Y. Hagiwara, Japanese Patent Application JPA 1975-127646 on N+NP+NP-P Triple Junction Type Pinned Photodiode with Back Light Illumination with the CCD type MOS capacitor Buffer Memory for Global Shutter Function.

[8] Y. Hagiwara, Japanese Patent Application JPA 1975-127647 on N+NP+N Double Junction Type Pinned Photodiode with Back Light Illumination with the CCD type MOS capacitor Buffer Memory for Global Shutter Function.

[9] Y. Hagiwara, Japanese Patent No. 1215101 (Japanese Patent Application JPA 1975-134985) on the Pinned surface P+NP double junction type Pinned Photodiode on N-type substrate wafer, forming a P+NP triple junction dynamic photo thyristor type PPD with the VOD function.

https://eds.ieee.org/images/files/newsletters/Newsletter_Jan23.pdf See pp.22-31

Introduction to Semiconductor Device

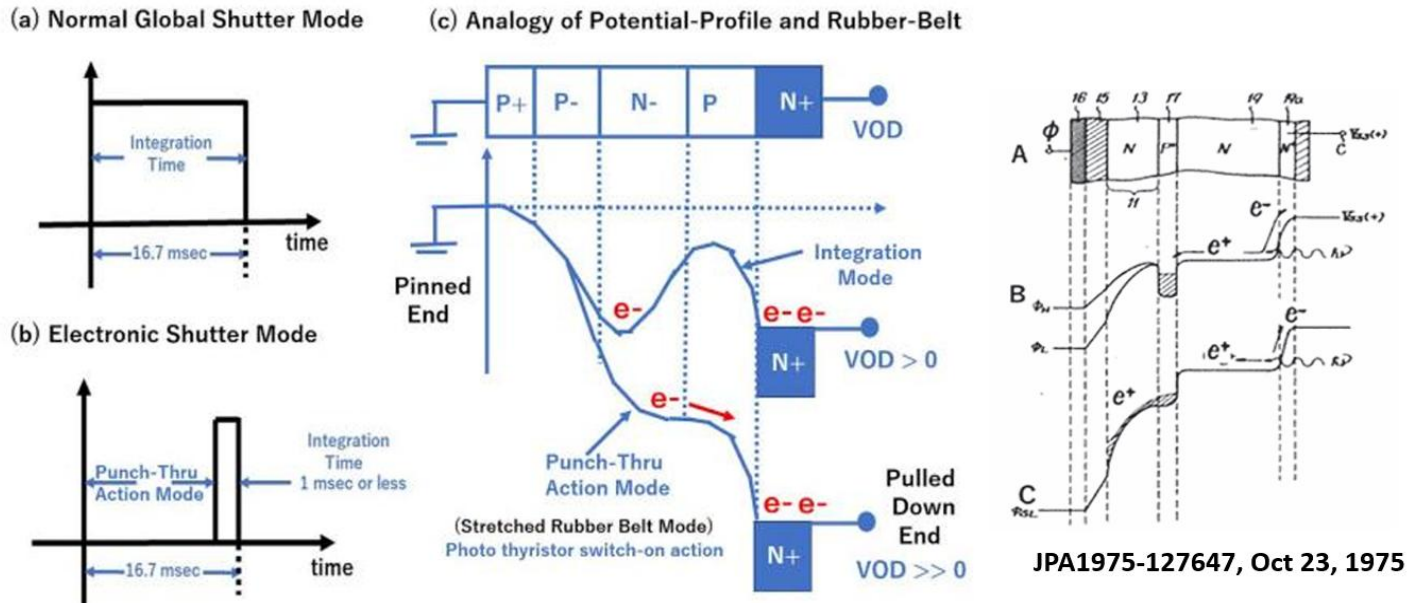


Fig. 8: (a), (b) Global shutter clocking schemes for CMOS image sensors: normal global shutter mode, electronic shutter mode; (c) the electrical potential profile of the P+PN-PN+ triple junction type PPD in the photo thyristor switch-on mode and in the integration mode.

https://eds.ieee.org/images/files/newsletters/Newsletter_Jan23.pdf See pp.22-31

SSDM1978 Conference in Tokyo Japan

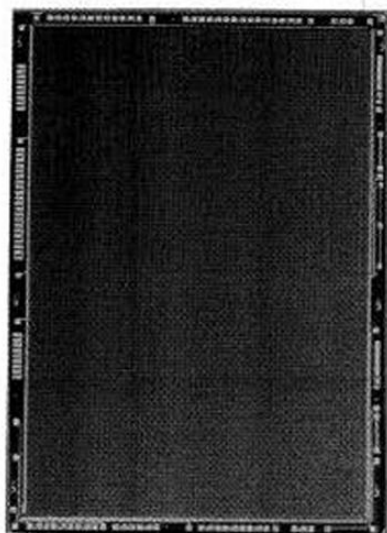


Fig. 3. Photomicrograph of the 380 H x 488 V CCD imager. The chip size is 14.6 mm by 10.1 mm.

SSDM1978 Conference in Tokyo Japan

[13] Y. Daimon-Hagiwara, M. Abe and C. Okada, "A 380H x 488V CCD Imager with Narrow Channel Transfer Gates", Proc. 10th Conf. on Solid State Devices, 1978; Japanese J. Applied Physics, Vol. 18 Sup. 18-1, 1979, 335-340.

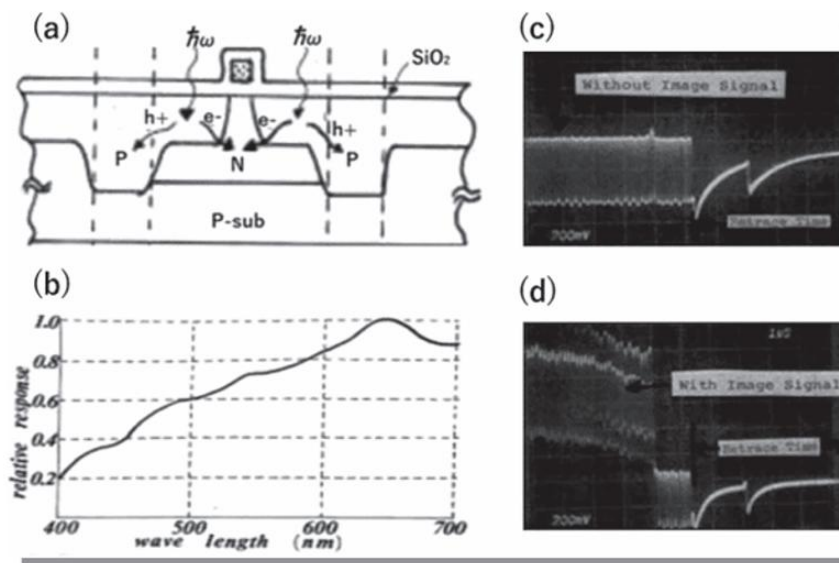


Figure 4 (a) Pinned-surface and buried-storage PNP photodiode; (b) spectral response of the blue-light sensitive imager; output signal (c) without (d) with illumination.

January 2023 ○ IEEE Electron Devices Society Newsletter 23

https://eds.ieee.org/images/files/newsletters/Newsletter_Jan23.pdf See pp.22-31

SSDM1978 Conference in Tokyo Japan

Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978;
Japanese Journal of Applied Physics, Volume 18 (1979) Supplement 18-1, pp. 335-340

A 380H × 488V CCD Imager with Narrow Channel Transfer Gates

Yoshiaki Daimon-HAGIWARA, Motoaki ABE† and Chikao OKADA†

Longer Wave Length Light (0.5~0.7 μm) has almost 100% QM ($\eta=1$) in Silicon.

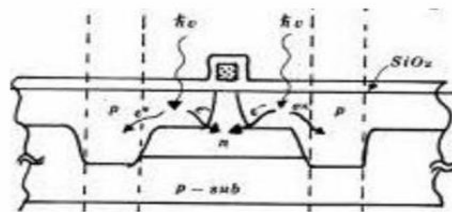


Fig. 2. cross sectional views of the electrode

This is the first original PNP Pinned Photodiode developed in 1978 with the excellent short-wave blue light sensitivity.

Hagiwara at Sony invented and formed the adjacent P+ channel stops to pin the P+ surface, using high-energy ion-implantation.

This PNP double junction Pinned Photodiode structure can be used for a solar cell with a very high quantum efficiency.

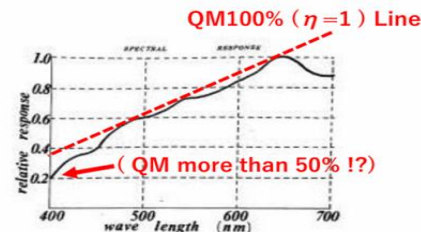


Fig. 13. Spectral Response of the photosensors.

The plantation mask, boron ions with the dose level of $2 \times 10^{13} \text{ cm}^{-2}$ are implanted into the silicon substrate throughout the exposed portions of the thermally grown oxide. This step provides self-aligned channel stops which surround the narrow-channel transfer part of each electrode. The gate oxide thickness is 130 nm throughout the device.

The transfer efficiency of the vertical and horizontal shift registers are more than 99.995% per transfer. And high image resolution of 280 TV lines/p.h. (Horizontal) and 350 TV lines/p.h. (Vertical) have been obtained.

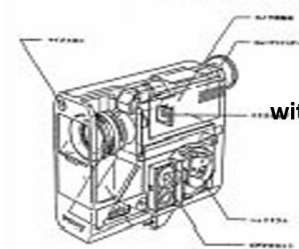
The typical dark current level is less than 3% of the maximum signal level at the room temperature of 20°C. The spectral response of the imager shows that this inherently SiO₂ exposed structure has high enough quantum efficiency at 450 nm wavelength and functions as a color imager with high sensitivity.

The typical dark current level is less than 5 nA/cm². For the particular device reported in this paper, the ion implantation dose of the buried channel is taken to be $1.7 \times 10^{12} \text{ cm}^{-2}$.

**PNP double junction pinned-surface photodiode
with No Image Lag and Electrical Shutter Capability
free from any mechanical parts.**

[13] Y. Daimon-Hagiwara, M. Abe and C. Okada, "A 380H × 488V CCD Imager with Narrow Channel Transfer Gates", Proc. 10th Conf. on Solid State Devices, 1978; Japanese J. Applied Physics, Vol. 18 Sup. 18-1, 1979, 335-340.

World-first one-chip FT CCD image sensor used in Sony Video Movie Camera on April 1, 1980.



**<FCX016> 570H x 498V One-Chip
FT CCD Color Imager, 1978**

with the PNP double junction pinned-surface photodiode sensors.



Kazuo Iwama @ Tokyo Press Conf, 1978



PNP double junction pinned-surface photodiode
with No Image Lag and Electrical Shutter Capability
free from any mechanical parts.

Origin of Digital Camera, 1980

SSDM1978 Conference in Tokyo Japan

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Longer Wave Length Light ($0.5\sim 0.7\mu\text{m}$) has almost 100% QM ($\eta=1$) in Silicon.

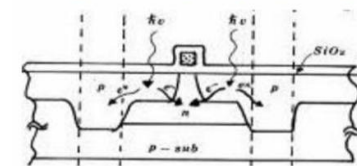


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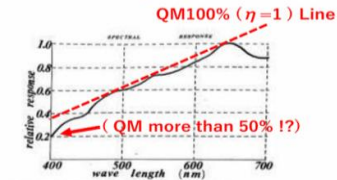


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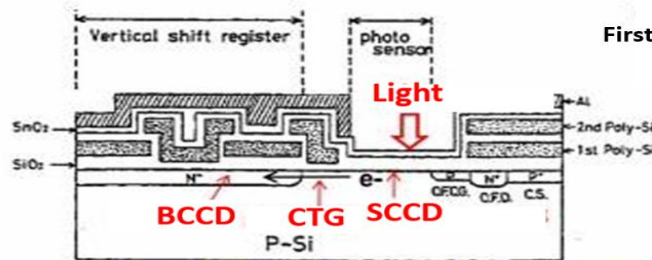
The first film-free and no-image lag video-camera without the slow mechanical shutter but with the very fast electrical-shutter with 8 mm metal tape recording media, which was replaced by Mini Floppy Disk, NVRAM and USB Memory and Hard Disk for Large Memory Capacity.

World-first commercialized two-chip CCD image sensor
video camera by Sony on April 1, 1980.

Sony ICX-008 CCD chip

XC-1 1980
Two-Chip Color Video
Camera

all solid state = robustness



First Commercialize CCD chip designed and Developed
by Sony (Yoshiaki Hagiwara), in April 1, 1980

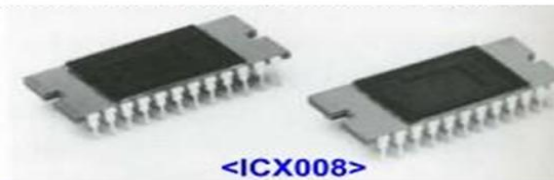
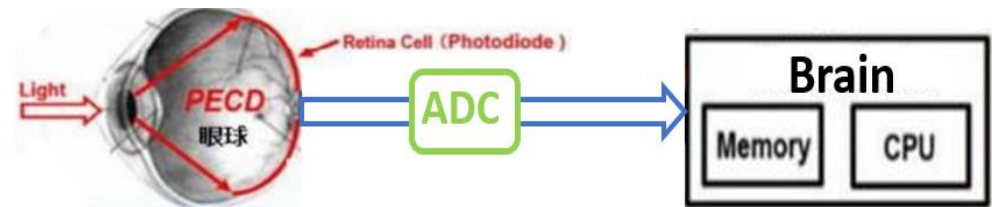


Photo Sensor is thin-polysilicon MOS gate capacitor type with the surface-channel CCD charge transfer (SCCD) mode thru the enhancement MOS charge transfer gate (CTG) to the buried-channel CCD charge transfer (BCCD) mode vertical analog-data shift-register. All CCD-mode operations and completely image-lag free achieving the electrical shutter.

Fusion of Analog and Digital Semiconductor Device and Circuit Technology for Future AI Robot Applications



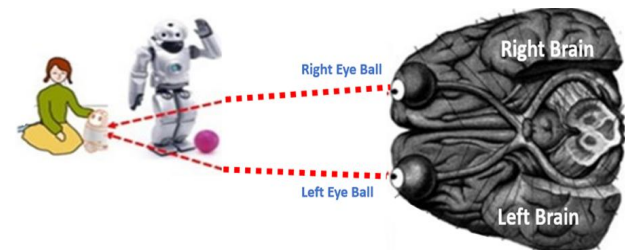
Introduction

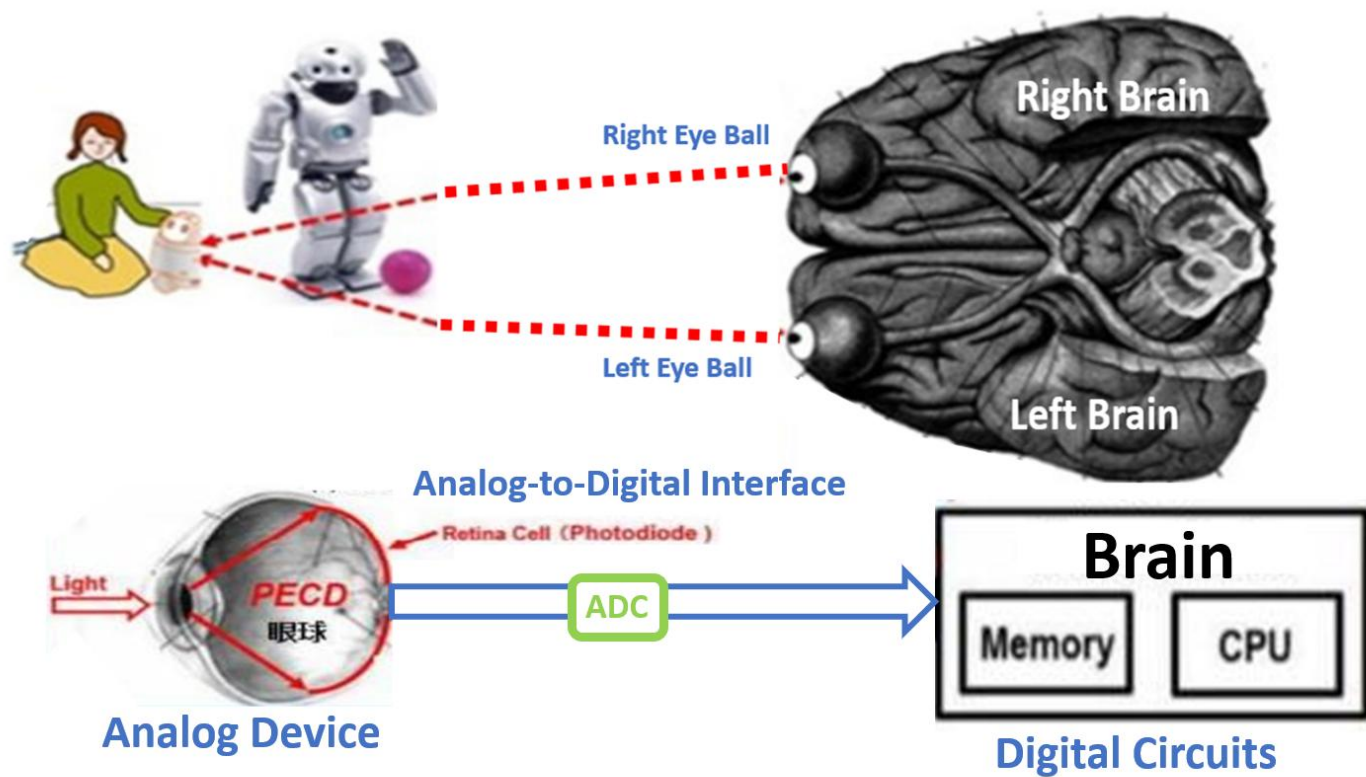
Sensor and Analog Circuit Technology

Flash ADC and DFT Technology

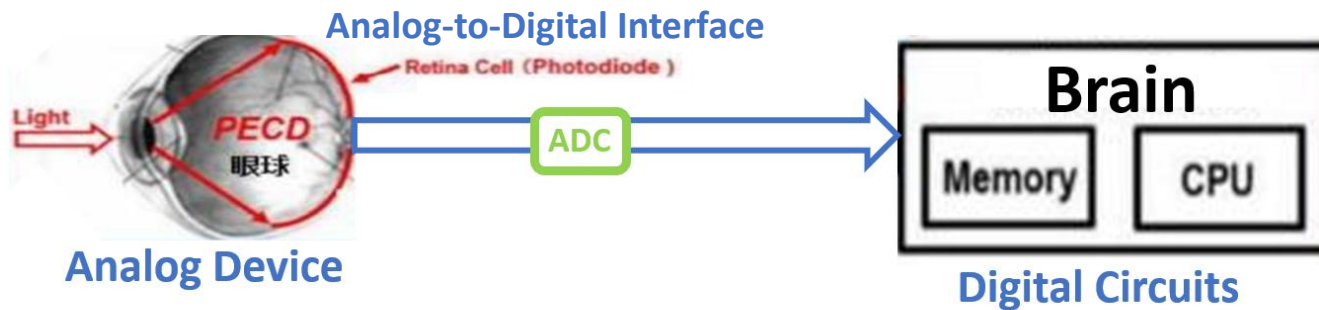
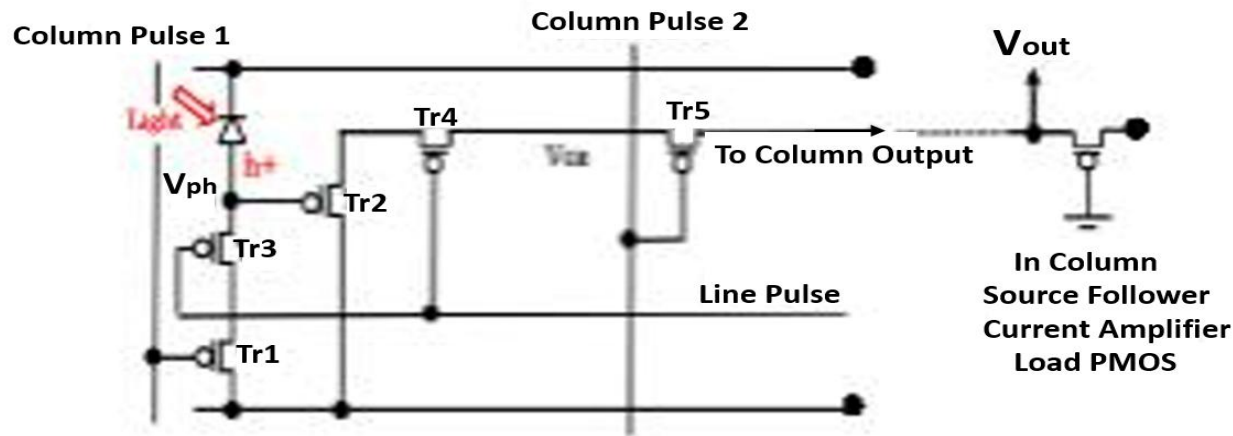
Digital Circuit Technology

Conclusion

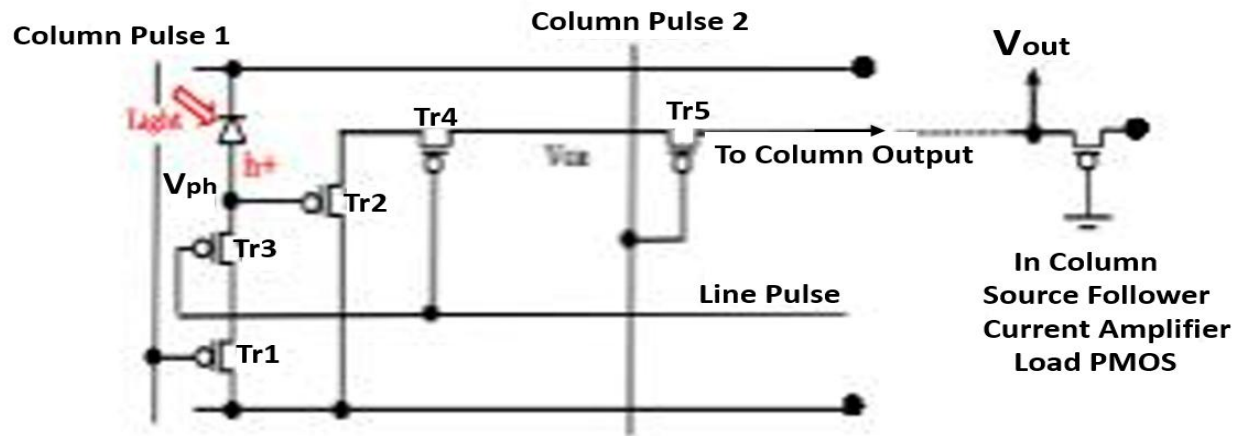




The active in-pixel source-follower type (APS)
PMOS imager invented by Peter Nobel in 1966.

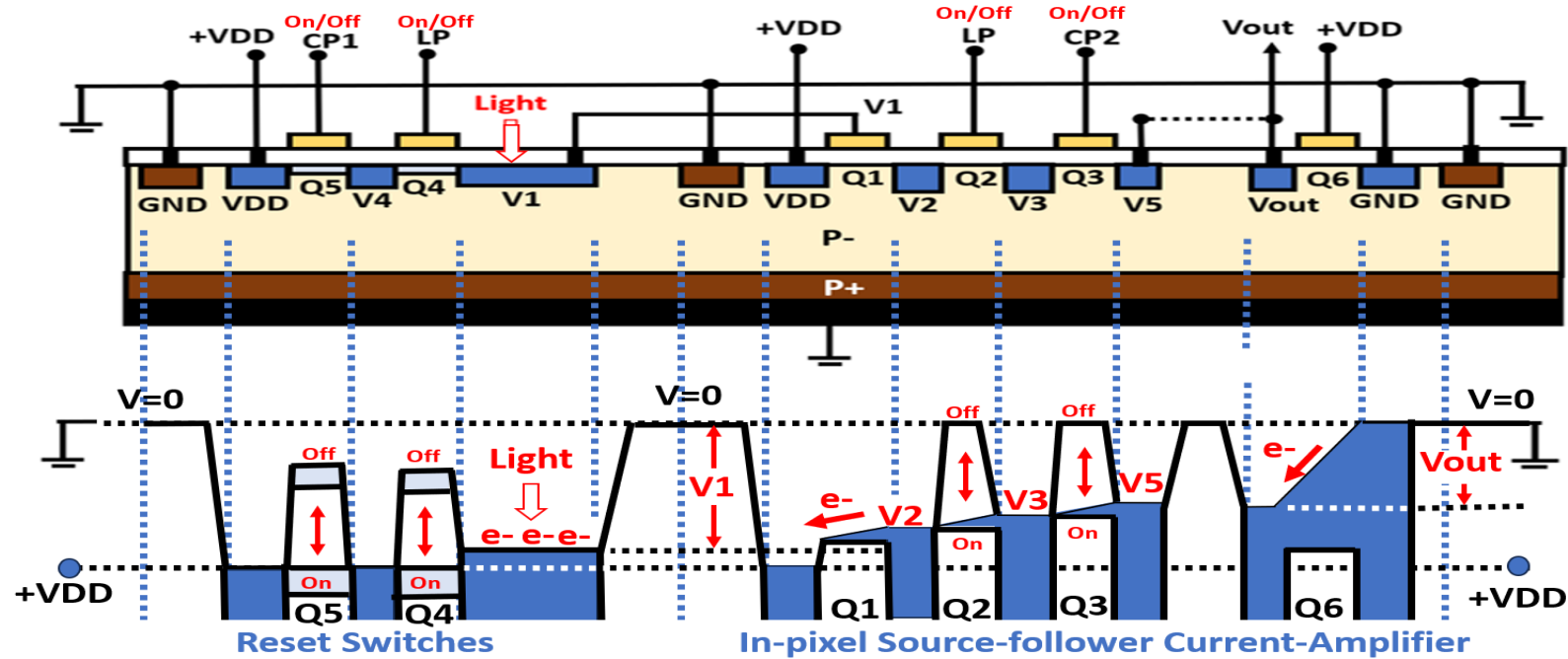


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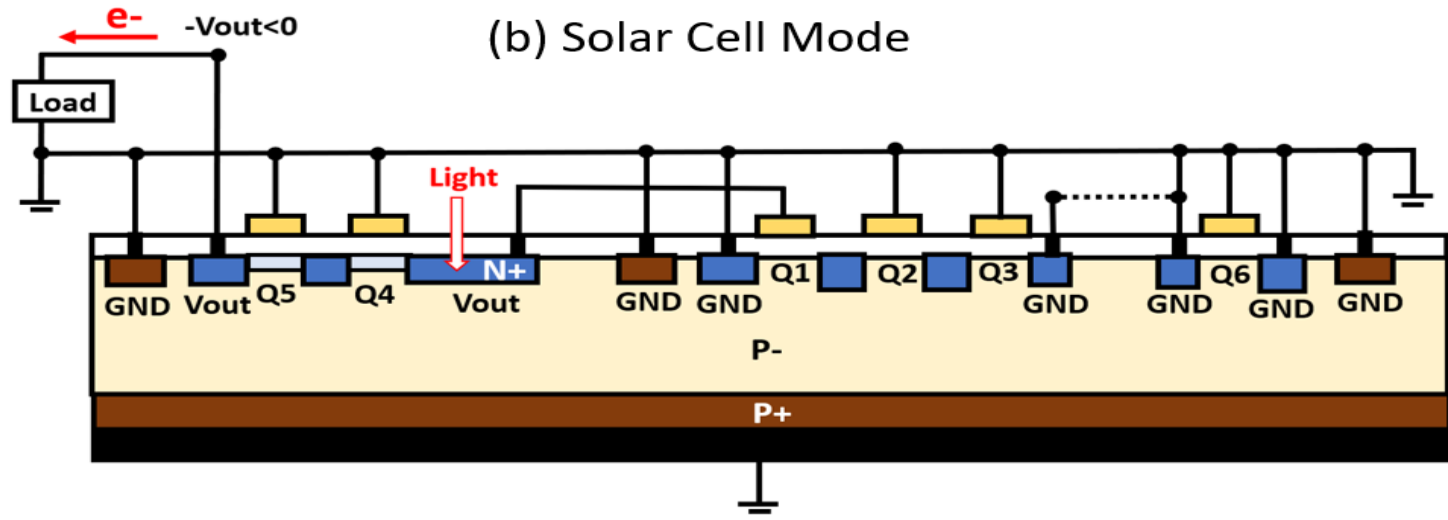


The standard CMOS APS pixel consists of a photodetector (pinned photodiode), a floating diffusion, and the so-called 4T cell consisting of four CMOS transistors, including a charge transfer gate (CTG), reset gate, selection gate and source-follower readout transistor. The pinned photodiode was originally used in Frame Transfer (FT) and interline transfer (ILT) CCDs due to its low dark current and good blue response, and when coupled with the transfer gate, allows complete charge transfer from the pinned photodiode to the floating diffusion (which is further connected to the gate of the read-out transistor) eliminating lag.

(a) Image Sensor Mode



(b) Solar Cell Mode



ISSCC1984, Sony

ISSCC 84 / WEDNESDAY, FEBRUARY 22, 1984 / IMPERIAL BALLROOM / 9:30 A.M.

SESSION IV: DATA ACQUISITION CIRCUITS

WAM 4.2: An 8b 100MS/s Flash ADC

Yoji Yoshii, Katsuaki Asano, Minoru Nakamura, Chikara Yamada

Sony Corp.

Kanagawa, Japan

Abstract:

An 8-bit flash ADC capable of operation at a sampling rate higher than 100 MHz with only 1.2 W of power dissipation is described.

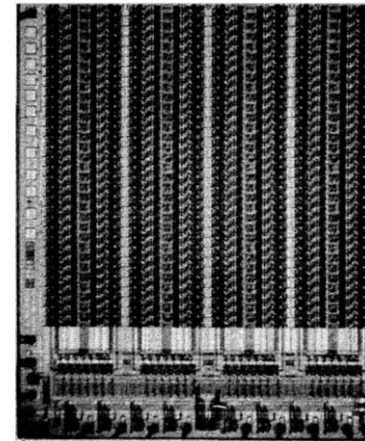
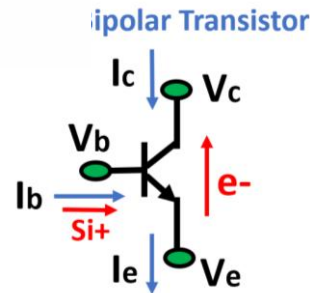


FIGURE 4—Photomicrograph of chip.

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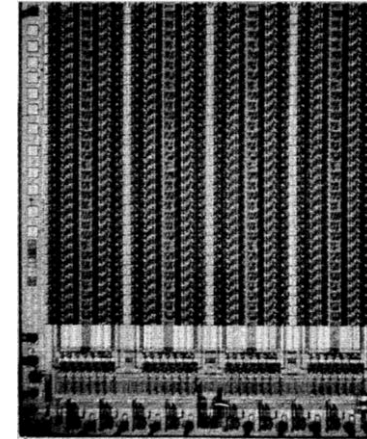
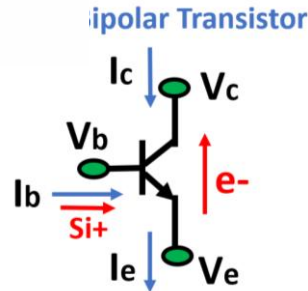


FIGURE 4—Photomicrograph of chip.

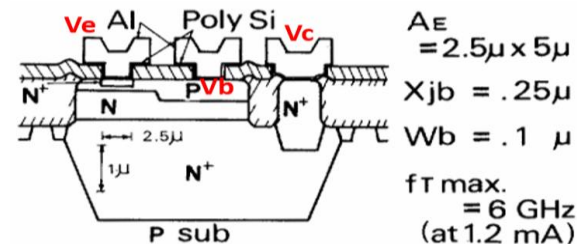


FIGURE 2—Cross sectional view of device.

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- (3) a simple comparator design with small component count.

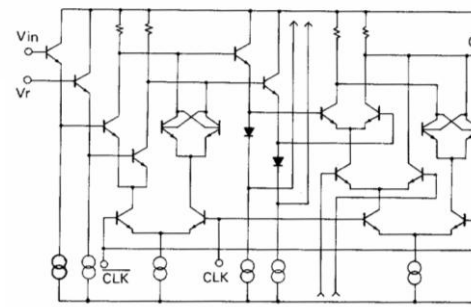


FIGURE 3—Simplified schematic of a comparator cell.

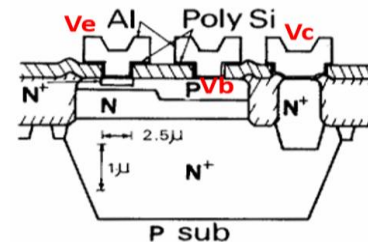
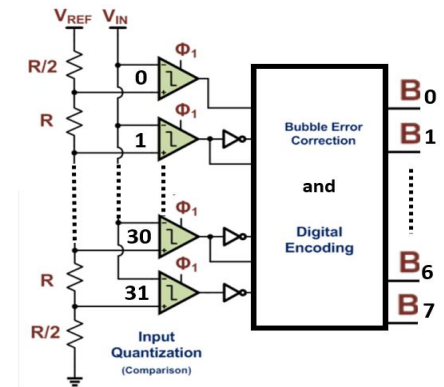


FIGURE 2—Cross sectional view of device.

$A_E = 2.5 \mu \times 5 \mu$
 $X_{jb} = .25 \mu$
 $W_b = .1 \mu$
 $f_T \text{ max.} = 6 \text{ GHz}$
 (at 1.2 mA)

8bit Flash ADC



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SESSION IV: DATA ACQUISITION CIRCUITS

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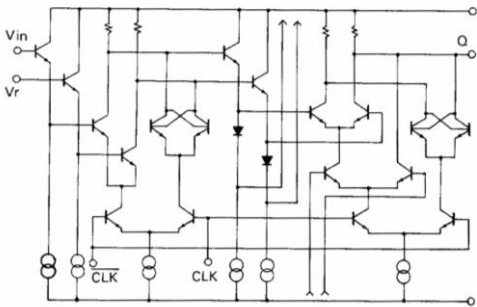
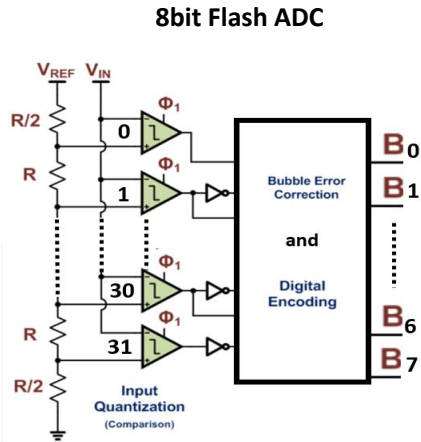


FIGURE 3—Simplified schematic of a comparator cell.



Resolution	8b $\pm 1/2$ LSB
Max. conversion rate	100MHz
Full scale input BW (−3dB)	30MHz
Differential gain	1.5%
Differential phase	0.5°
Analog input capacitance	35pF
Power dissipation	1200mW
Power supply	−5.2V
Chip size	5.45 x 4.15mm ²

TABLE 1 — Chip performance.

<https://ieeexplore.ieee.org/document/9058907>

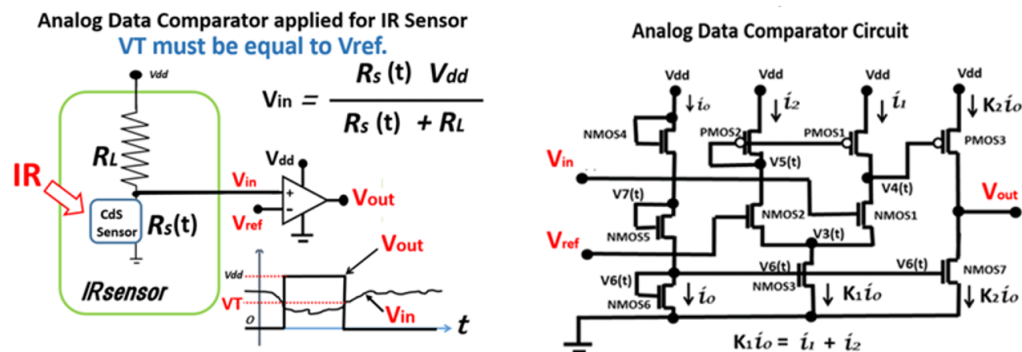
3DIC2019.4017

2019 International 3D Systems Integration Conference (3DIC)

Multichip CMOS Image Sensor Structure for Flash Image Acquisition

Yoshiaki Hagiwara

AIPS



The comparator circuit is a conventional one that can also be used for a simple IR sensor detector as shown in Fig. 12.

<https://ieeexplore.ieee.org/document/9058907>

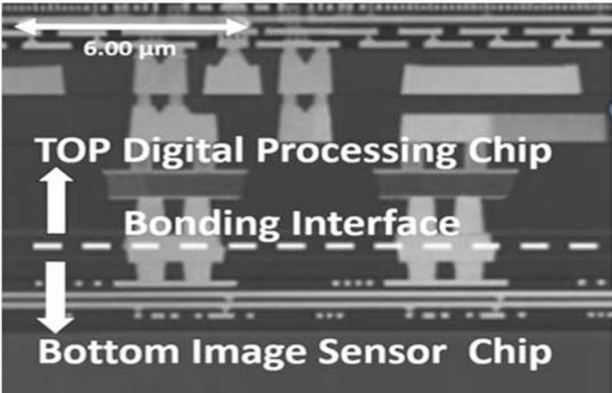
3DIC2019.4017

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AIPS



with the courtesy of Sony corporation

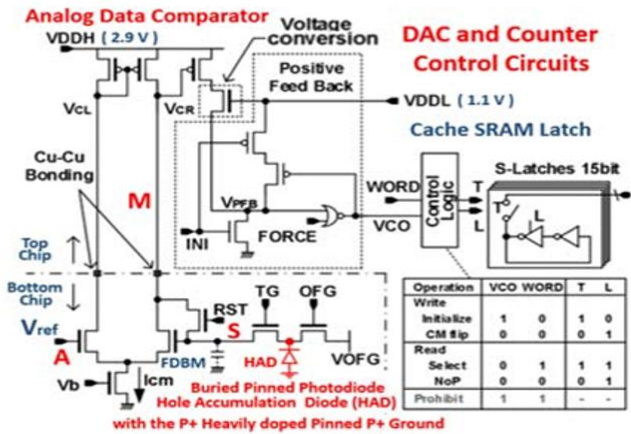


Fig. 14: Cross Sectional View of two chip stacked back-illuminated CMOS Image Sensor¹⁴ with the in-pixel analog comparator control circuits to generate the match signal M from the reference voltage A and the image sensor signal S.

Sojo University, Izumo-city, June 2014

Design and Performance Estimation of DFT Processing Circuits

Weikun Liang, Yuji Yoshida, Kishi Fukakusa ,

Yoshiaki Hagiwara (Sojo University)

DFT is essential for voice and picture recognition. Normally DFT is processed by software, and the processing time is not negligible. This paper reports a challenge to design a DFT hardware engine circuit and estimate its performance by use of a recursive design procedure.

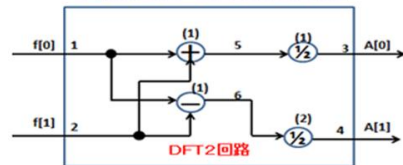
Izumo-city, Shimane-ken, Japan, July 4, 2014

電気学会 電子回路研究会

2014年7月4日 (金) 09:30~12:05

@ニューウェルシティ出雲(7/4)
島根県出雲市塩冶有原町2-15-1

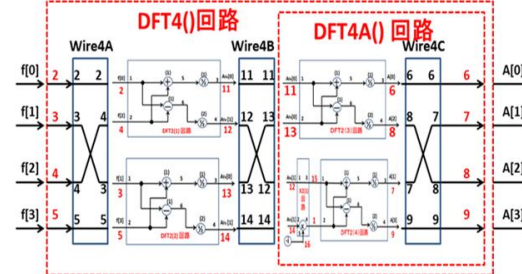
2bit DFT Circuit Block



```
define DFT2 () { input(1,2); output(3,4);
5=add(1)(1,2); 6=sub(1)(1,2);
3=half(1)(5) ; 4=half(2)(6) ; }
```

図2 2点入力DFT演算回路 DFT2()の定義

4bit DFT Circuit Block



```
define DFT4A() { input(11,13,12,14);output(6,7,8,9);
16=rom(-i); 15=12; 1= x(1)(14,16);
(6,8)=DFT2(3)(11,13); (7,9)=DFT2(4)(15,1);}

define DFT4() { input(2,3,4,5);output(6,7,8,9);
(11,12)=DFT2(1)(2,4);(13,14)=DFT2(2)(3,5);
(6,7,8,9)=DFT4A(1)(11,13,12,14);}
```

図6 4点DFT演算回路 DFT4()の定義

https://jglobal.jst.go.jp/en/detail?JGLOBAL_ID=201402211529054168

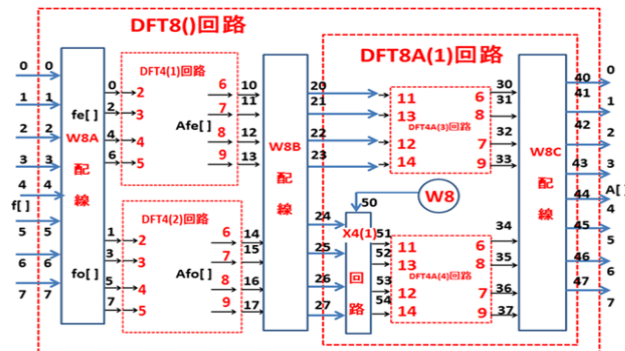
Sojo University, Izumo-city, June 2014

Design and Performance Estimation of DFT Processing Circuits

Weikun Liang, Yuji Yoshida, Kishi Fukakusa ,

Yoshiaki Hagiwara (Sojo University)

8bit DFT Circuit Block



```
define DFT8A(){ input(20-27);output(40-47);
    50=ROM(W8); (51-54)=X4(1)(50,24-27);
    (30-33)=DFT4A(3)(20-23); (34-37)=DFT4A(4)(51-54);
    (40-47)=W8C(30-37);}
define DFT8 () { input(0-7);output(40-47);
    (10-13)=DFT4(1)(0,2,4,6);(14-17)=DFT4(2)(1,3,5,7);
    (20-27)=W8B(10-17);(40-47)=DFT8A(20-27);}
```

図7 8点 DFT 演算回路 DFT8() の定義

Following this method, an 8-point DFT DFT8() can be designed also by a combination of four DFT4(). Applying this Recursive Circuit Design Procedure, DFT16(), DFT32(), DFT64(), and DFT128() circuits can be implemented.

Even though the circuit size gets bigger, by using this recursive design procedure to create a hierarchy like this, simulations and implementation design with NET coding can be carried out relatively easily.

This is very attractive with scaled CMOS process technology.

https://jglobal.jst.go.jp/en/detail?JGLOBAL_ID=201402211529054168

Sojo University, Kumamoto, June 2015

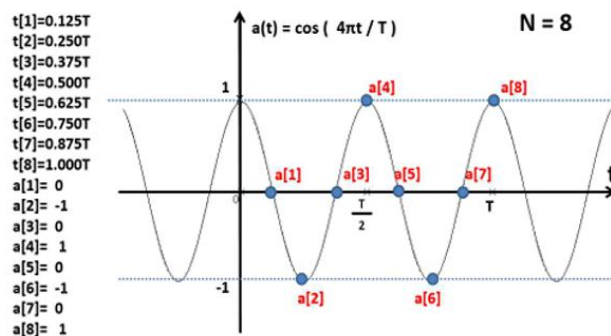
[Japanese Patent Application JPA2014_135497](#)

[Digital Frequency Transformation Circuit for Time-wise Unequally Sampled Data | Article Information | J-GLOBAL](#)

Masaru TANAKA, Weikun LIANG, and Yoshiaki HAGIWARA

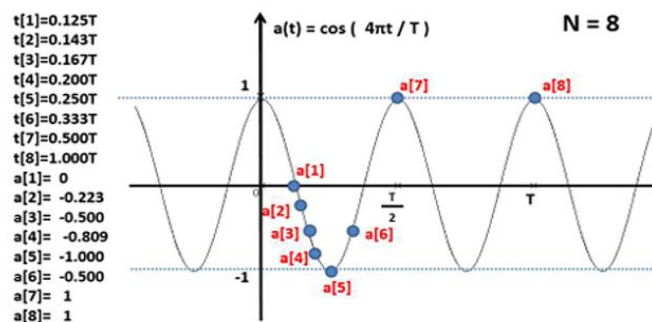
Sojo University, Kumamoto City, Japan

DFT is essential for voice and picture recognition. Normally DFT is processed for Time-wise Equally Sampled Data. This paper reports a challenge to design a DFT circuit for Time-wise Unequally Sampled Data.



$$A[] = W[] [a[]] = \{0, \frac{1}{2}, 0, 0, 0, \frac{1}{2}, 0, 0\}$$

(a) Conventional DFT Sampling



$$A[] = \text{invH}[] [a[]] = \{1.032, 1.500, 0.0, 0.0, -0.809, -0.500, -0.223, 0.0\}$$

(b) T/k Sampling (this work)

["Digital Frequency Transformation Circuit for Time-wise Unequally Sampled Data"](#)

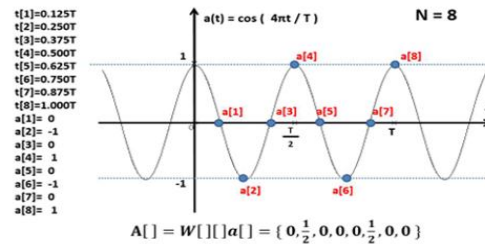
Sojo University, Kumamoto, June 2015

[Japanese Patent Application JPA2014_135497](#)

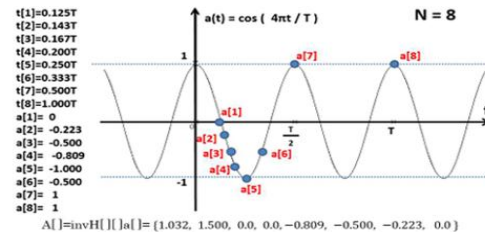
[Digital Frequency Transformation Circuit for Time-wise Unequally Sampled Data](#) | [Article Information](#) | [J-GLOBAL](#)

Masaru TANAKA, Weikun LIANG, and Yoshiaki HAGIWARA

Sojo University, Kumamoto City, Japan



(a) Conventional DFT



(b) T/k Sampling

$$N=2 \quad a[] = H2[] [] A[] \quad N=2 \quad A[] = \text{invH}2[] [] a[]$$

$$\begin{bmatrix} a[1] \\ a[2] \end{bmatrix} = \begin{bmatrix} -1 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} A[1] \\ A[2] \end{bmatrix} \quad \begin{bmatrix} A[1] \\ A[2] \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} a[1] \\ a[2] \end{bmatrix}$$

$$N=3 \quad a[] = H3[] [] A[] \quad N=3 \quad A[] = \text{invH}3[] [] a[]$$

$$\begin{bmatrix} a[1] \\ a[2] \\ a[3] \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ -1 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} A[1] \\ A[2] \\ A[3] \end{bmatrix} \quad \begin{bmatrix} A[1] \\ A[2] \\ A[3] \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 0 & 0 & 2 \\ 1 & 1 & 0 \\ 1 & -1 & -2 \end{bmatrix} \begin{bmatrix} a[1] \\ a[2] \\ a[3] \end{bmatrix}$$

$$N=4 \quad a[] = H4[] [] A[] \quad N=4 \quad A[] = \text{invH}4[] [] a[]$$

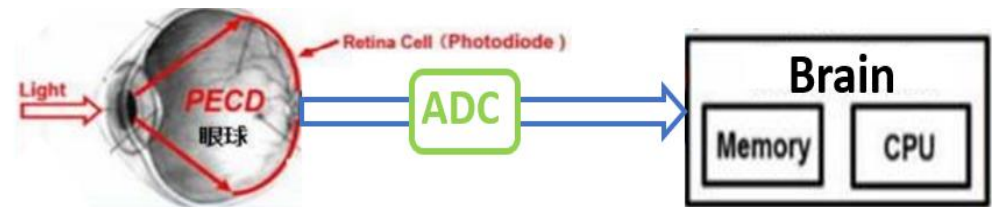
$$\begin{bmatrix} a[1] \\ a[2] \\ a[3] \\ a[4] \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ -1 & 1 & -1 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} A[1] \\ A[2] \\ A[3] \\ A[4] \end{bmatrix} \quad \begin{bmatrix} A[1] \\ A[2] \\ A[3] \\ A[4] \end{bmatrix} = \frac{1}{4} \begin{bmatrix} 1 & 1 & 0 & 2 \\ 0 & 0 & 4 & 0 \\ 1 & 1 & 0 & -2 \\ 2 & -2 & 4 & 0 \end{bmatrix} \begin{bmatrix} a[1] \\ a[2] \\ a[3] \\ a[4] \end{bmatrix}$$

$$N=8 \quad a[] = H8[] [] A[] \quad N=8 \quad A[] = \text{invH}8[] [] a[]$$

$$\begin{bmatrix} a[1] \\ a[2] \\ a[3] \\ a[4] \\ a[5] \\ a[6] \\ a[7] \\ a[8] \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 1 & 0 & -1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ -1 & -1 & -1 & -1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} A[1] \\ A[2] \\ A[3] \\ A[4] \\ A[5] \\ A[6] \\ A[7] \\ A[8] \end{bmatrix} \quad \begin{bmatrix} A[1] \\ A[2] \\ A[3] \\ A[4] \\ A[5] \\ A[6] \\ A[7] \\ A[8] \end{bmatrix} = \frac{1}{8} \begin{bmatrix} 1 & 1 & 0 & 2 & 0 & 0 & 0 & 4 \\ 0 & 0 & 0 & 0 & 0 & 0 & 8 & 0 \\ 0 & 0 & 4 & 0 & 4 & 0 & 0 & 0 \\ 0 & 0 & 0 & 8 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 2 & 0 & 0 & -4 & 0 \\ 0 & 0 & 4 & 0 & -4 & 0 & 0 & 0 \\ 2 & -2 & -4 & -4 & 0 & -4 & 0 & 0 \\ 4 & -4 & -4 & 0 & -8 & 4 & -8 & 0 \end{bmatrix} \begin{bmatrix} a[1] \\ a[2] \\ a[3] \\ a[4] \\ a[5] \\ a[6] \\ a[7] \\ a[8] \end{bmatrix}$$

["Digital Frequency Transformation Circuit for Time-wise Unequally Sampled Data"](#)

Fusion of Analog and Digital Semiconductor Device and Circuit Technology for Future AI Robot Applications



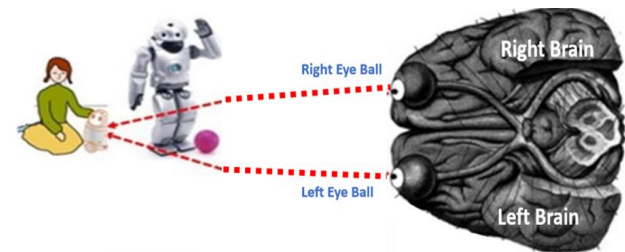
Introduction

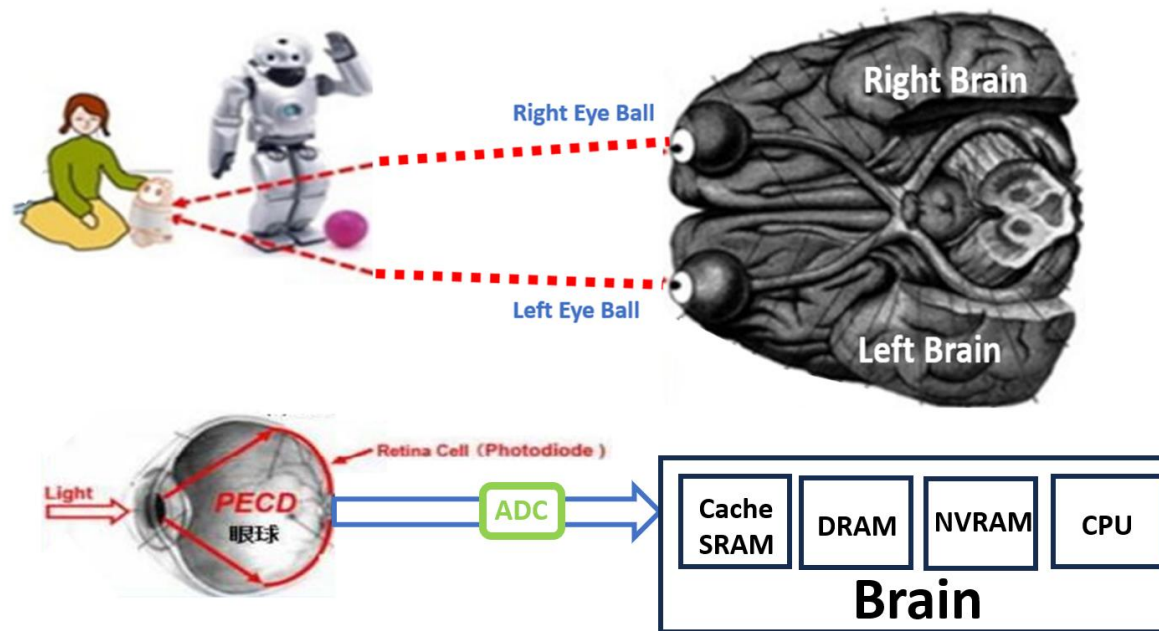
Sensor and Analog Circuit Technology

Flash ADC and DFT Technology

Digital Circuit Technology

Conclusion





To make AI robots a reality, it's important to reliably combine three key technologies:

- (1) analog circuit technology, essential for controlling mechanisms like sensors and robot arms,
- (2) digital circuit technology that enables high-speed information processing using large-capacity DRAM, cache SRAM, and NVRAM, and
- (3) high-speed real-time flash AD converter technology.

"A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads"

A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads

FUMIO MIYAJI, YASUSHI MATSUYAMA, YOSHIKAZU KANAISHI,
KATSUNORI SENOH, TAKASHI EMORI, AND
YOSHIAKI HAGIWARA, MEMBER, IEEE

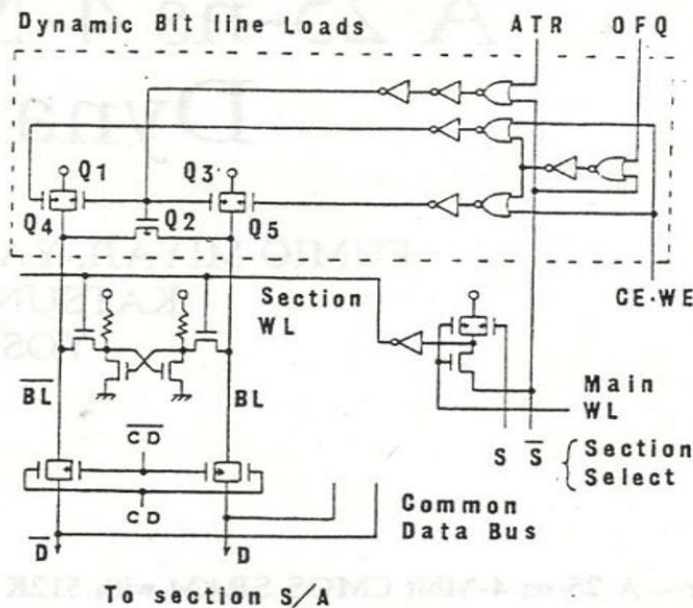


Fig. 4. DBL circuit.

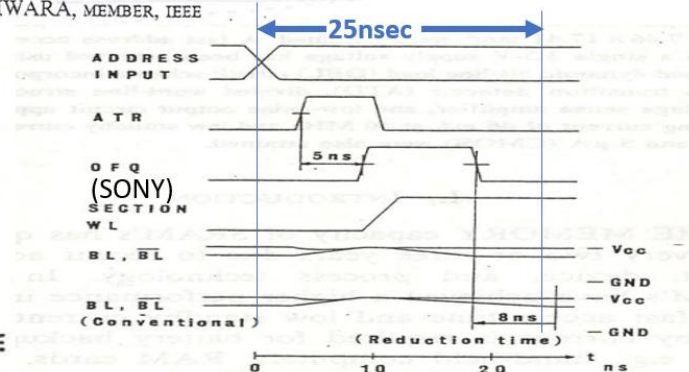


Fig. 5. Timing diagram for the read operation.

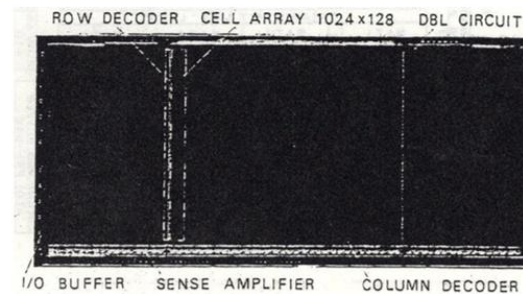


Fig. 3. Photomicrograph of the chip.

IEEE ISSCC1989, paper on SONY 4MBit Cache SRAM

<https://www.elsepub.com/pdf/doi/10.55092/20250003>

May 23-25, 2025

Past, Presence and Future Applications of Buried-channel Double-junction Sony Hole Accumulation Diode (HAD) type Image Sensors and Solar Cells with Pinned Surface and Empty Potential Well.
Yoshiaki Daimon Hagiwara

2. Multi-chip 3DIC back-light illuminated CMOS image sensor for real-time AI robot vision

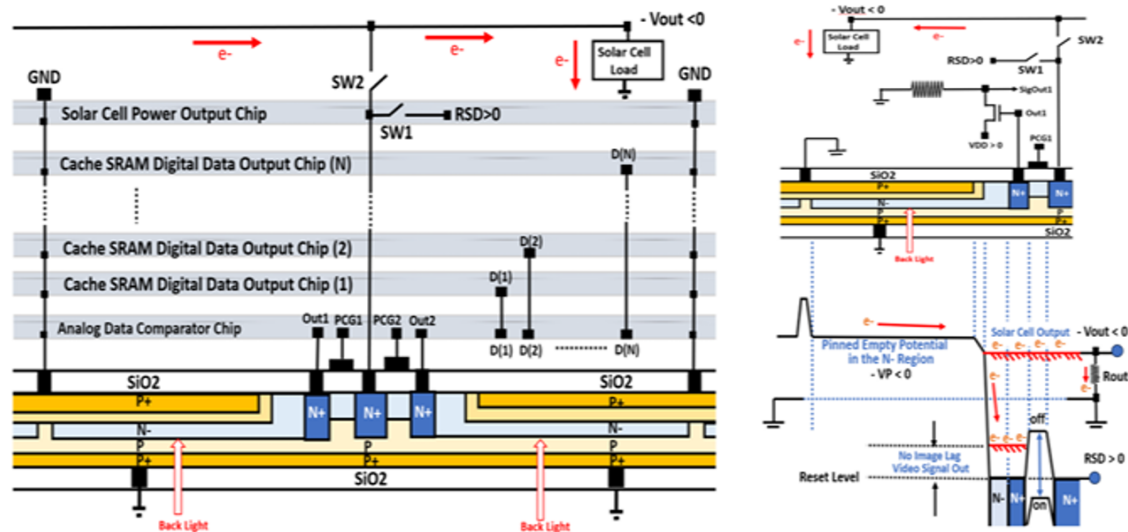


Figure 4. A cross-sectional view of a new AI Robot Vision chip in 3DIC multichip architecture.

Yoshiaki Hagiwara

"Micro-Electronics for Home Entertainment"

Sony Corpoartion, Tokyo Japan
yoshiaki.hagiwara@jp.sony.com

an invited ESSCIRC2001 Plenary Talk,

Technical Digest of IEEE ESSCIRC2001 International Conference (ESSCIRC2001),

Villach, Austria, September, 2001.

Abstract

A brief historical overview of a first home entertainment consumer electronic gadget, called a portable transistor radio is given, and then some introductory comments on the basic semiconductor device concepts are explained. They are strongly related to the microelectronics of the present home entertainment LSI chips with regard to the product specifications and performance aspects of the home entertainment LSI chip sets, such as for digital cameras, home robotics and games.

3.1 Digital Still Camera.

The picture in the Fig. 7 shows a 2/3 inch 190K pixel IT CCD Imager, ICX016/XC-37 which I designed when I was still a young CCD design engineer in early 1981. This model became the model of the world first consumer CCD video camera for mass production in 1983.



Fig. 7 The World First Consumer CCD Video Camera for Mass Production 1983

All CCD Image sensor with Electrical Shutter Capability for Robot Vision

"Micro-Electronics for Home Entertainment"

an invited ESSCIRC2001 Plenary Talk, Villach, Austria, September, 2001.

Yoshiaki Hagiwara

Sony Corpoartion, Tokyo Japan

yoshiaki.hagiwara@jp.sony.com

Abstract

A brief historical overview of a first home entertainment consumer electronic gadget, called a portable transistor radio is given, and then some introductory comments on the basic semiconductor device concepts are explained. They are strongly related to the microelectronics of the present home entertainment LSI chips with regard to the product specifications and performance aspects of the home entertainment LSI chip sets, such as for digital cameras, home robotics and games.

AIBO 2nd Generation, ERS-210

Sony Dream Robot, SDR-3



Fig. 10 New AIBO Models, ERS-210 and SDR-3

- (3) M. Fujita and H. Kitano: "{D}evelopment of and {A}utonomous {Q}uadruped {R}obot for {R}obot {E}ntertainment", Autonomous Robots vol.5, pp.7-8, Kluwer Academic Publishers, 1998.

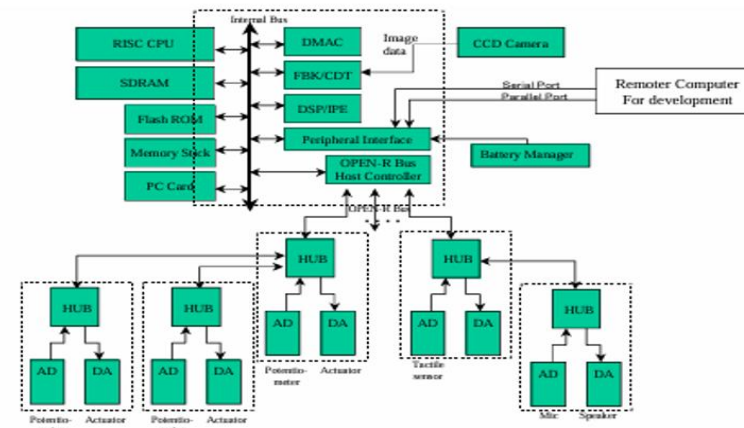


Fig. 11 Logical Hardware Block Diagram

- (4) Kohtaro Sabe, " Architecture of Entertainment Robot - Development of AIBO -", IEEE Computer Element MESA Workshop 2001, Mesa Arizona, Jan 14-17, 2001

"Micro-Electronics for Home Entertainment"

an invited ESSCIRC2001 Plenary Talk, Villach, Austria, September, 2001.

Yoshiaki Hagiwara

Sony Corpoartion, Tokyo Japan

yoshiaki.hagiwara@jp.sony.com

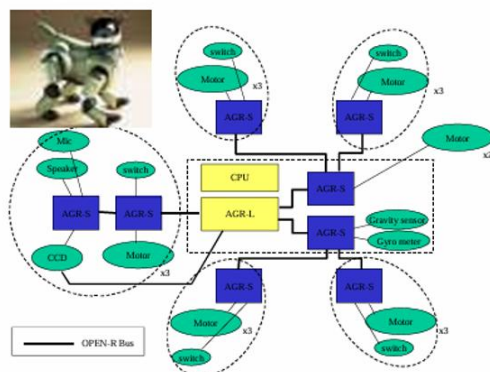


Fig. 12 Topology of ERS-110

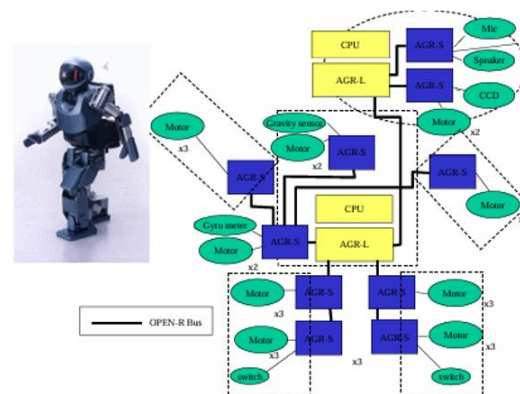


Fig. 13 Topology of SDR-3x

- (3) M. Fujita and H. Kitano: "{D}evelopment of and {A}utonomous {Q}uadruped {R}obot for {R}obot {E}ntertainment", Autonomous Robots vol.5, pp.7-8, Kluwer Academic Publishers, 1998.

- (4) Kohtaro Sabe, "Architecture of Entertainment Robot - Development of AIBO -", IEEE Computer Element MESA Workshop 2001, Mesa Arizona, Jan 14-17, 2001

"SOI Design in Cell Processor and Beyond"

an invited ESSCIRC2008 Plenary Talk, Technical Digest of IEEE
ESSCIRC2008 Conference,
Edinburgh, Scotland UK, September 2008.

SOI Design in Cell Processor and Beyond

Yoshiaki Daimon Hagihara

Chairman and CEO, AIPS/AINS Consortium

(Ex-Sony Fellow, Semiconductor Strategic Planning)

Hagihara-Yoshiaki@aiplab.com

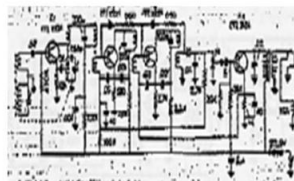
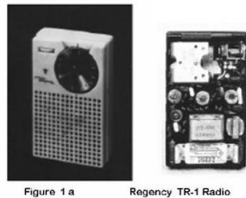
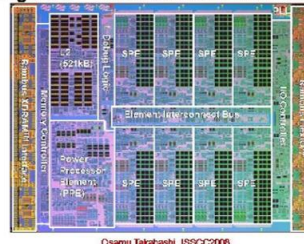


Figure 1b Circuits Diagram of Regency TR-1 Radi

Figure 8 45nm Cell/B.E. Die Photo



By 1994, the games were just starting to move to 0.5-micron processes, while the leading process was 0.35 micron. Eventually over time, the game chips migrated to smaller processes to increase integration and reduce costs. Now games

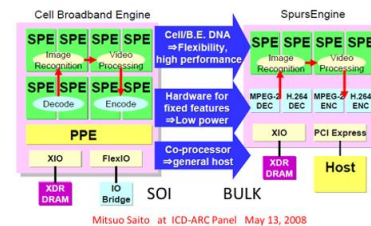


Figure 10 Cell/B.E. and Toshiba SpursEngine

Fusion of Analog and Digital Semiconductor Device and Circuit Technology for Future AI Robot Applications

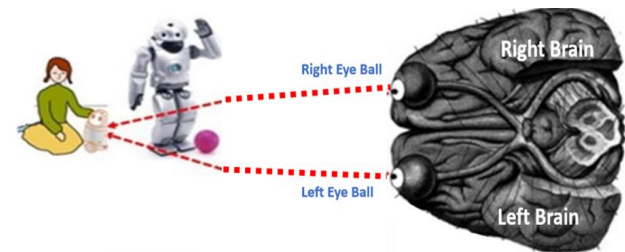
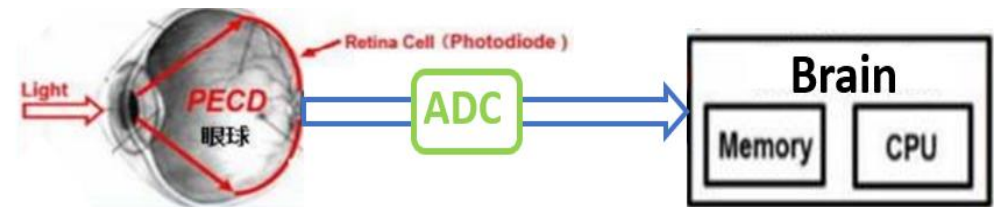
Introduction

Sensor and Analog Circuit Technology

Flash ADC and DFT Technology

Digital Circuit Technology

Conclusion



"Prospect of Developing AIPS Robots for Home Total Supporting Systems"

IEICE technical report, December 12, 2008, ICD2008 Conference, Tokyo, Japan, Vol 108-247, pp.85-90

在宅総合支援AIPSロボット開発の展望

Prospect of Developing AIPS Robots for Home Total Supporting Systems

～ ソフトメカエレキの融合技術が鍵 ～

-- The key is the combined technology of Software, Mechanical and Electronics --

萩原良昭

Yoshiaki Hagihara

(NPO 法人) AIPS コンソーシアム

(NPO) Artificial Intelligent Partner Systems Consortium

Kazuo Iwama in ISSCC1954

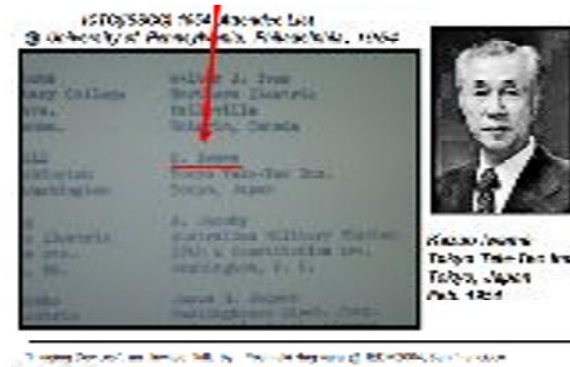


図1) 1954年岩間和夫氏第1回 ISSCC 出席

2006 PS3
Cell Processor

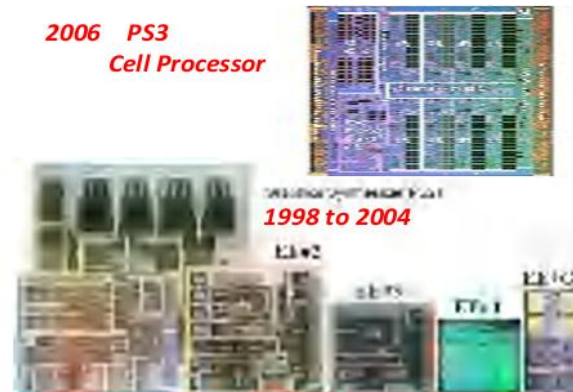


図4) CELL プロセッサ

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IEICE technical report, December 12, 2008, ICD2008 Conference, Tokyo, Japan, Vol 108-247, pp.85-90

在宅総合支援AIPSロボット開発の展望

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萩原良昭

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(NPO 法人) AIPS コンソーシアム

(NPO) Artificial Intelligent Partner Systems Consortium



図2) 1972年128bit比較器開発プロジェクト

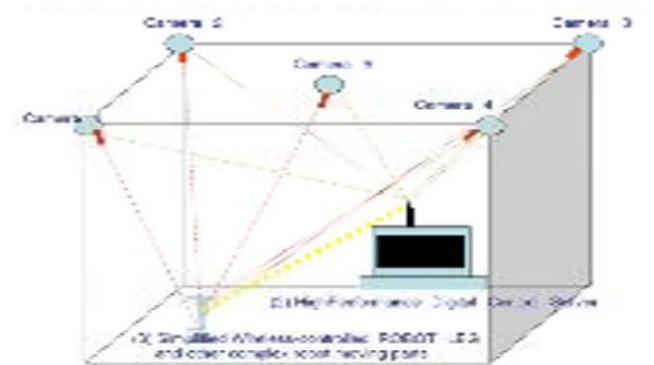


図5) 在宅介護総合AIPSの概念図

"Prospect of Developing AIPS Robots for Home Total Supporting Systems"

IEICE technical report, December 12, 2008, ICD2008 Conference, Tokyo, Japan, Vol 108-247, pp.85-90

在宅総合支援AIPSロボット開発の展望

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(NPO) Artificial Intelligent Partner Systems Consortium



図3) 1995年 Vail Computer Workshop



図6) AIPSロボットの応用例

<https://www.fifa.com/en/tournaments/mens/worldcup/qatar2022>
2

Evidently, the ball bottom point is touching at the ground point outside of the field line .

However, the ball is still on the line when looked from the top.

Qatar World Cup 2022: VAR semi-automatic offside technology

VAR at the 2022 World Cup in Qatar has 12 dedicated cameras. These camera have the triple junction type Pinned Photodiode, with the very high light sensitivity and the no image lag problem, realizing very fast action pictures with Global Shutter Function and completely mechanical-parts-free Electronic Shutter Function. Hagiwara at Sony invented Pinned Photodiode in 1975 and developed originally in 1978. See JPA1975-127646 applied on Oct 23 in 1975 and the SSDM1978 Conference Paper reported by Yoshiaki Hagiwara at Sony in Tokyo Japan in Sept 1978.



FIFA's use of VAR at the 2022 World Cup in Qatar will be different from the Premier League's use with the addition of a semi-automatic offside system. The new element uses 12 dedicated cameras that will track the ball and all players to calculate their exact position on the pitch.

CHRONOLOGY OF SILICON-BASED IMAGE SENSOR DEVELOPMENT

Yoshiaki Daimon Hagiwara, IEEE Life Fellow
Sajo University, Kumamoto-city, Japan

https://eds.ieee.org/images/files/newsletters/Newsletter_Jan23.pdf

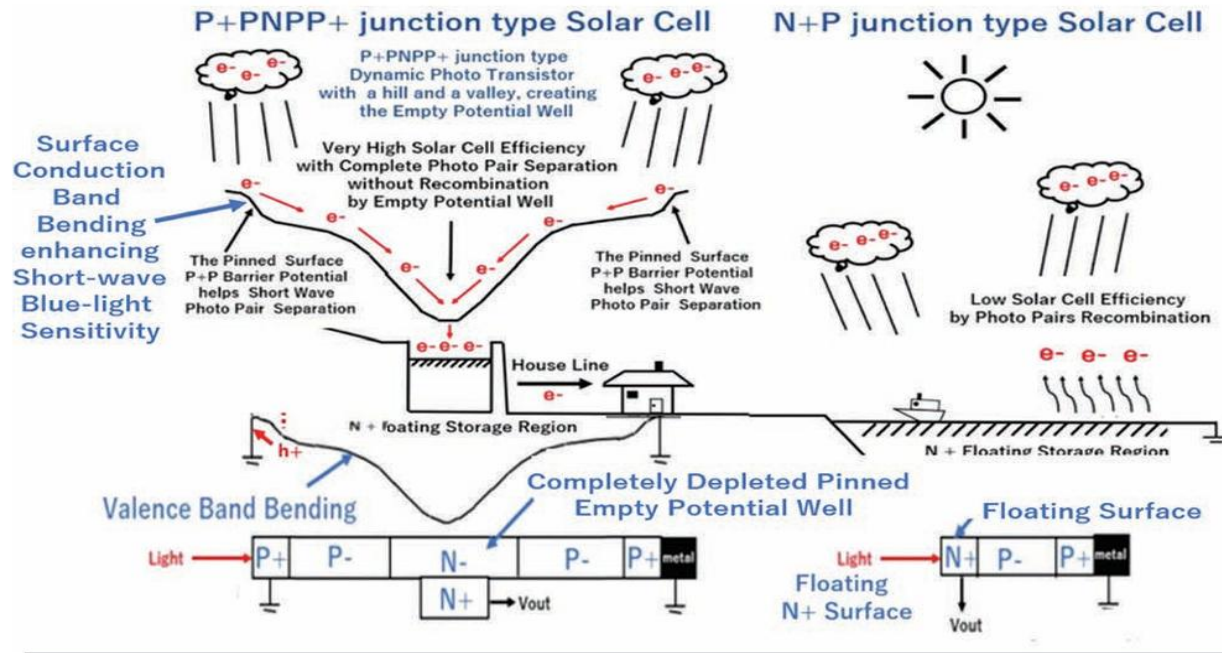
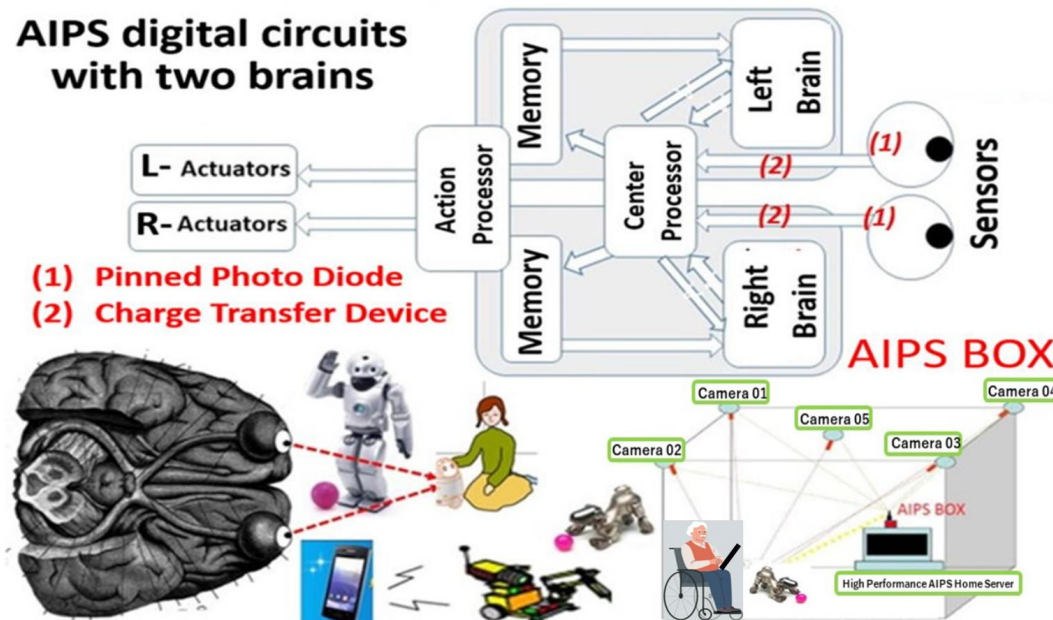


Figure 11. The PNP double-junction PPD with the completely depleted N region and the floating N+ storage region has an excellent quantum efficiency (QE) for the bluelight. The floating-surface N+P single-junction-type photodiode has no surface electric field, where the photogenerated electron and hole pairs do not move and eventually they recombine with each other, resulting in a poor QE for the short-wave blue-light

https://eds.ieee.org/images/files/newsletters/Newsletter_Jan23.pdf

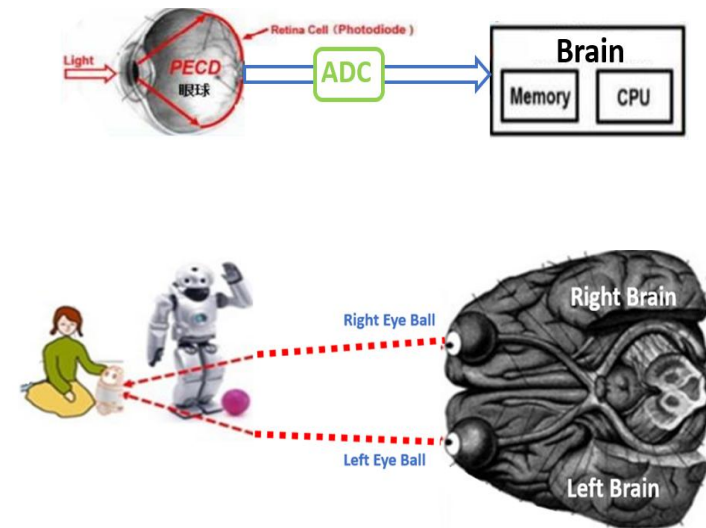
Concept of Artificial Intelligent Partner System (AIPS) proposed by Yoshiaki Hagiwara, May 2008

AIPS digital circuits with two brains



CHRONOLOGY OF SILICON-BASED IMAGE SENSOR DEVELOPMENT

Yoshiaki Daimon Hagiwara, IEEE Life Fellow
Sojo University, Kumamoto-city, Japan



Fusion of Analog and Digital Semiconductor Device and Circuit Technology for Future AI Robot Applications



Thank you very much !

Yoshiaki Daimon Hagiwara
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LOCOMTECH

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243-0201 Japan
hagiwara@aiplab.com

<https://locomtec.jp/harl-1>

[HAGIWARA AIPS Library](#)

[2026 07 07 ICCAS2026 Key Note Slides.pdf](#)
[2026 07 07 ICCAS2026 IDCS26-8837 6pages.pdf](#)
[2026 07 07 ICCAS2026 IDCS26-8837 Slides.pdf](#)

+++++

Yoshiaki Daimon Hagiwara Ph.D.,

IEEE Life Fellow, AAIA Fellow,

Caltech Distinguished Alumni,

Armenia Global High Technology Award 2024 Laureate

<https://www.primeminister.am/en/press-release/item/2025/05/14/Nikol-Pashinyan-Award-Ceremony/>

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<https://locomtec.jp/harl-1>

hagiwara@ssis.or.jp

<https://www.ssis.or.jp/>

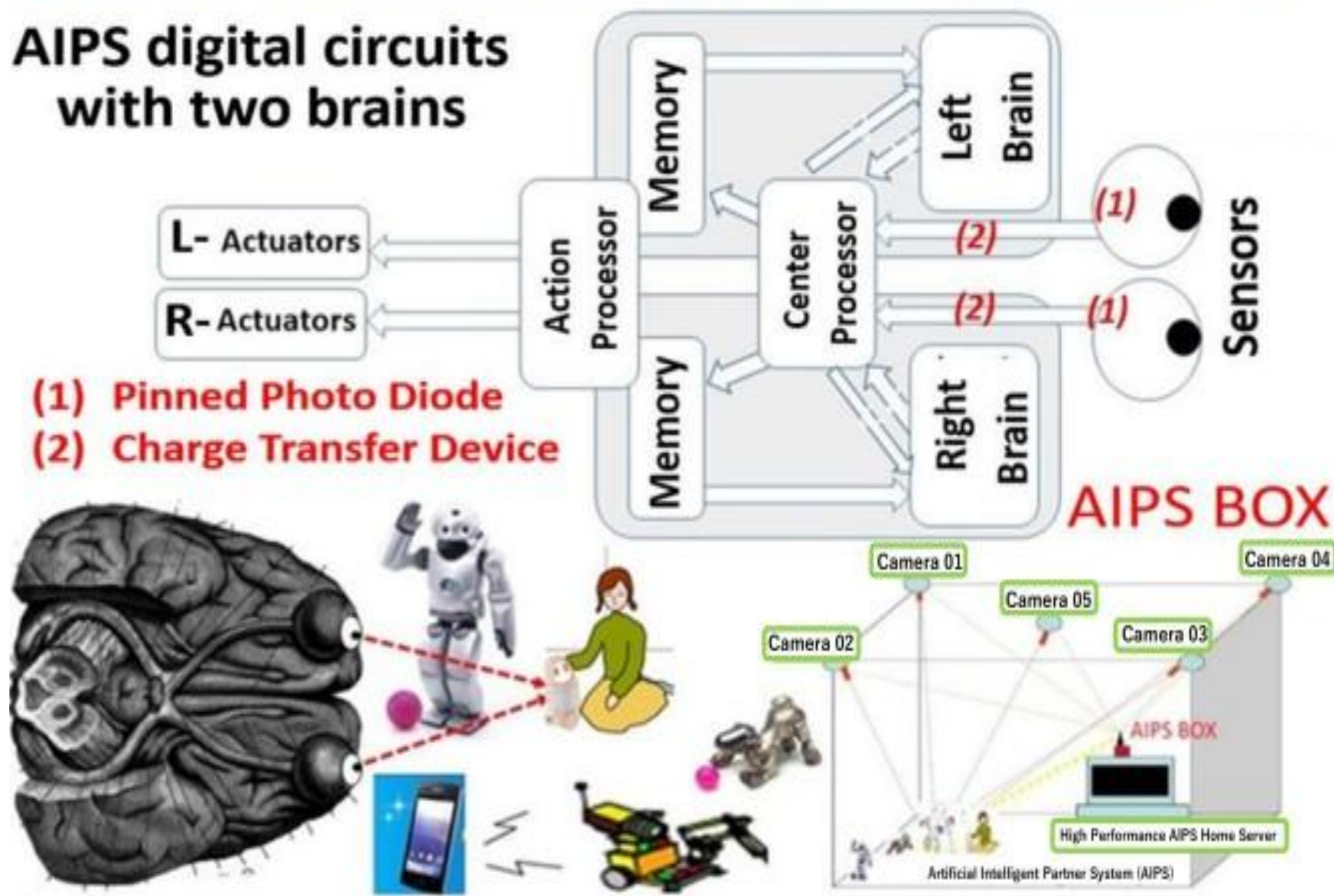
hagiwara@ofc.sojo-u.ac.jp

<https://www.sojo-u.ac.jp/>

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[Publication List by Yoshiaki Hagiwara.html](#)

AIPS digital circuits with two brains



MOS カメラから CCDカメラへ、そして、CCDカメラからCMOSカメラへ

Artificial Intelligence in Robot Vision



Mighty ATOM
/ ASTRO BOY © Osamu Tezuka



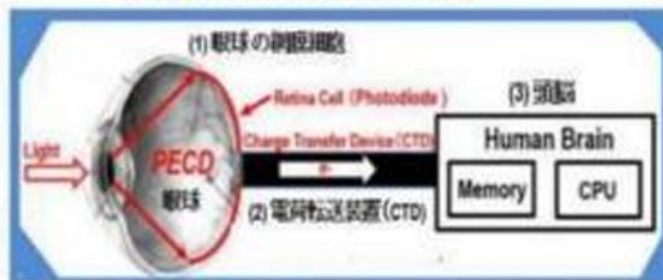
WALL-E © 2008 The Walt Disney Studios



理解度アップの基本復習問題

- 受光素子とは何か？
- 電荷転送装置 (CTD) とは？
- 感度 [Sensitivity] とは？
- CCD Image Sensor とは？
- CMOS Image Sensor とは？

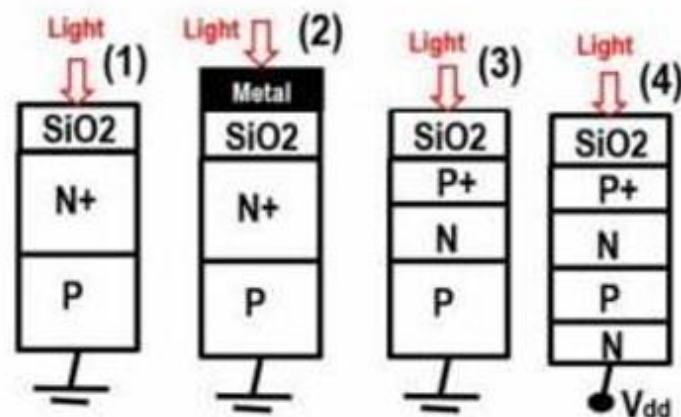
hagiwara-yoshiaki@aiplab.com
<http://www.aiplab.com/>



目次

1. イメージセンサとは
2. イメージセンサの歴史と市場動向
3. イメージセンサの基本構造
4. イメージセンサの動作原理
5. 賢いイメージセンサとは？

●イメージセンサーのいろいろな特徴



●イメージセンサーは感度が命



1. イメージセンサとは



Image Sensor Size



1. イメージセンサとは

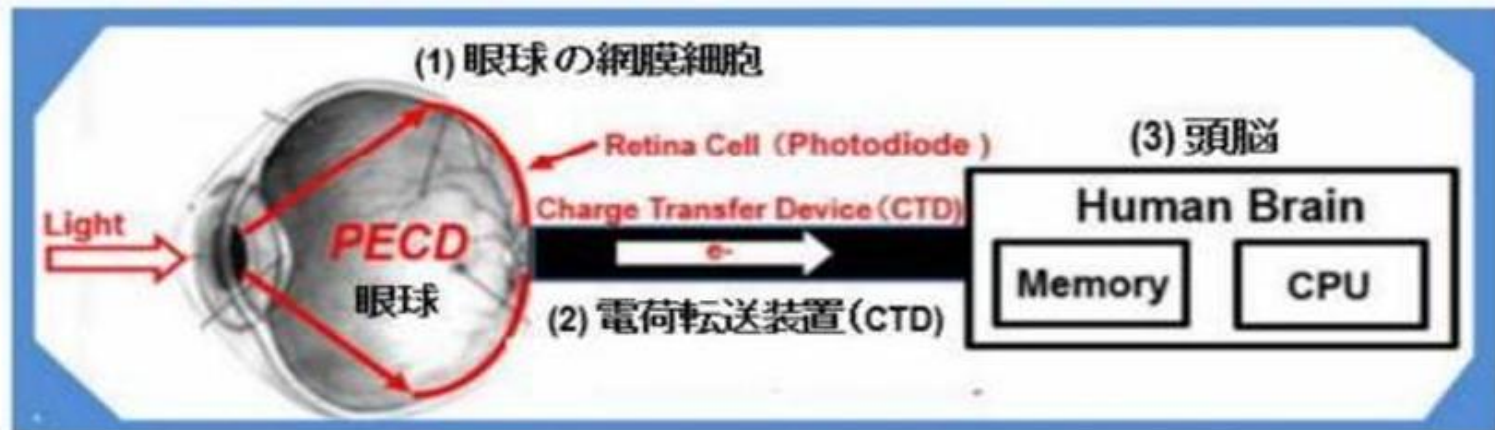
Image Sensorの基本構造は2つの重要な部分に分岐 & 進化。

(1) 人間の目の網膜細胞に相当する、光を電気信号に変換する半導体受光素子。

- (A) N+P接合型 (光感度が悪く、青色感度不足し、残像がひどかった。)
- (B) P+NP 型接合 (光感度良好、残像なし。しかし過剰照射光からの画像保護機能なし。)
- (C) P+NPNsub接合型 (別称HAD、光感度良好、残像なし、かつ過剰照射光保護機能あり。)

(2) 信号電荷を脳まで伝達する神経細胞の束に相当する、電荷転送装置 (CTD)

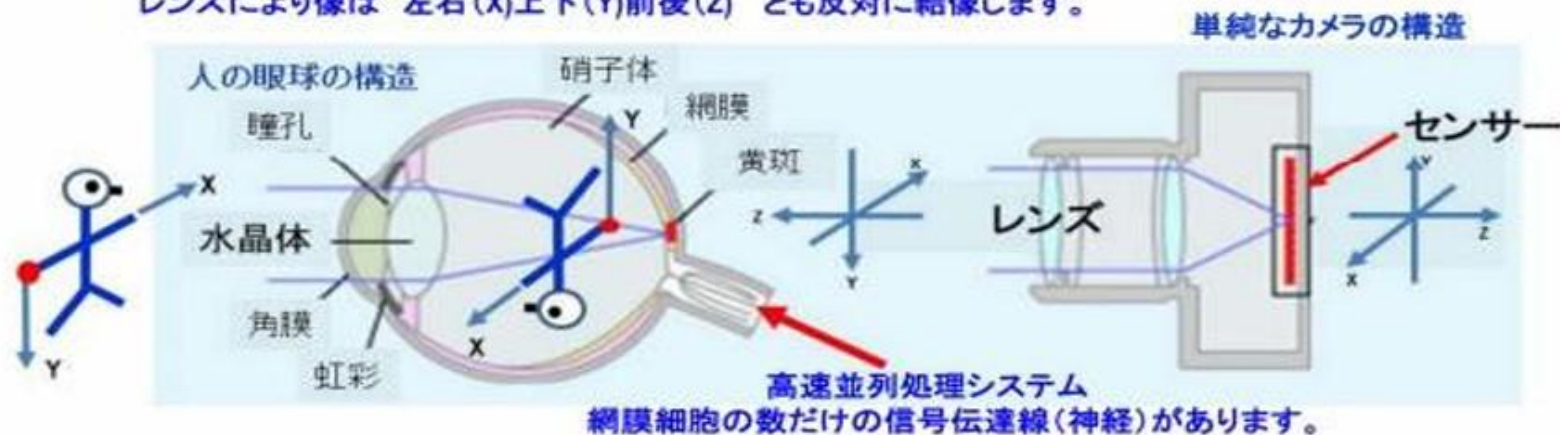
- (A) MOS 型電荷転送装置 (配線容量雑音とClock雑音が大きかった。)
- (B) CCD型電荷転送装置 (配線容量雑音もClock雑音なし、しかし消費電力が大きい。)
- (C) CMOS型電荷転送装置 (配線容量雑音もClock雑音なし、消費電力も小さい。)



1. イメージセンサとは

- レンズからの光を電気信号に変換する半導体(撮像素子) : 例 人間の目の網膜
- その性能(感度と解像度)がデジタルカメラの画質を左右

レンズにより像は 左右(X)上下(Y)前後(Z) とも反対に結像します。

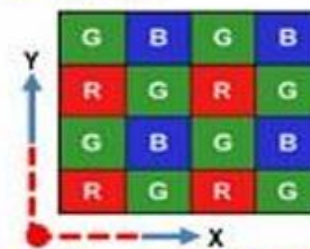


- ・ フォトセンサと呼ばれる小さな素子を多数、平面状の2次元行列に配置
- ・ 光の像を検知し、それを電気信号に変換
- ・ 変換した電気信号の取り扱い方法が2種類: CCDとCMOSイメージセンサ

CCD: Charge Coupled Device (電荷結合素子)

MOS: Metal Oxide Semiconductor (金属・酸化膜・半導体)

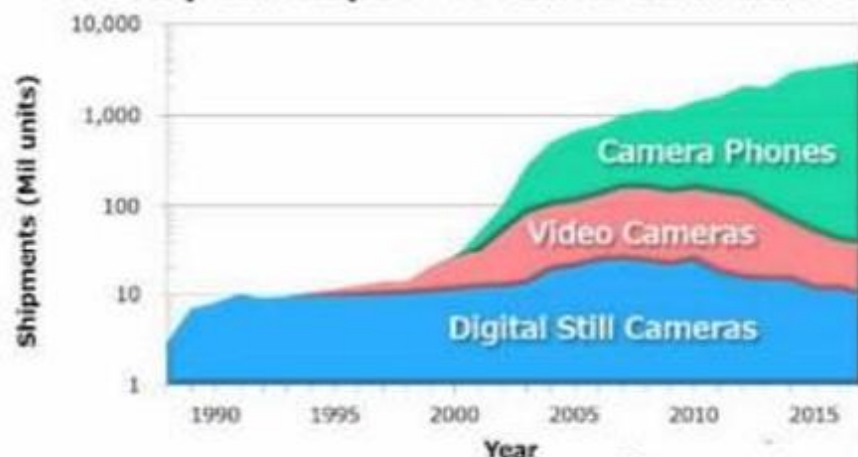
色の識別はカラーフィルターをチップの上に置き、それぞれの色の光を電気信号に変換します。



原色RGBフィルターの2次元配列の場合

2. イメージセンサの歴史と市場動向

History & Prospects of Camera Products



[Source: TSR et al.]

●世界のCMOSイメージセンサ市場

2017年 1.3兆円 前年比 +19% (出典 Insights)

2019年 SONYの半導体売上高が国内TOPとなる。
イメージセンサの売上高が大きく貢献。

●SONYのCMOSイメージセンサ市場シェア

世界シェア50%以上、世界のスマホの約60%、
世界のデジカメの約80%のシェアをSONYが持つ。

2018年 CIS* 2兆円市場用途別シェア

用途	シェア	前年比
モバイル向け	66.4%	12%
コンピュータ向け	8.2%	-7%
コンシューマ向け	7.8%	3%
セキュリティ向け	6.4%	20%
車載向け	6.3%	27%
産業向け	4.4%	17%
医療向け	0.6%	20%

国内半導体メーカーの売上高 単位: 億円

国内メーカー	2019年度	2018年度
ソニー	10,400	8,793
キオクシア	9,700	12,639
ルネサス	...	7,050
シャープ	...	4,990
ローム	3,900	3,989
東芝	3,430	3,549
日亜化学	3,100	2,914
三菱電機	1,850	1,700

出典: マイナビニュース

●国内半導体15社の2019年度売上高は前年比3%減の5.1兆円の規模に。

2. イメージセンサの歴史と市場動向

1969年: CCDはベル研究所で発明 残像のないCCD型受光素子と同時に、clock 雑音のないCCD型電荷転送装置を実現

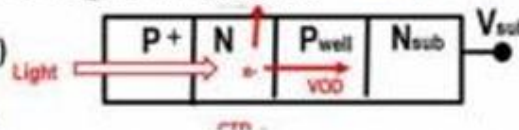
1972年: 国内でCCD構造の半導体で文字の撮影に成功

8 * 8 = 64画素で「S」の字を表示



●P+NP_{sub} 接合型HAD受光素子 (JAP 1975-134985)

萩原(1975) 基板(N_{sub})にP+NP接合を形成する。



1978年: P+NP接合のDynamic Photo Transistor (PPD) 型受光素子の開発に成功。FT方式CCD に採用してSSDM1978で発表。

残像のない、超感度 CCD カメラの商品化の動きが本格化。

1980年4月: Sony は CCD/MOS 容量型受光素子を採用した 2chip ILT方式CCD カメラの商品化。全日空ジャンボ機に搭載

1980年7月: 世界初のOne Chip CCD video camera 発表

光超感度の要因は独自考案のP+NP接合型のDynamic Photo Transistor 型 受光素子(PPD)の採用



1982年 残像のあるPNP接合BPDをILT方式CCDを開発(NEC)

1984年 残像のないP+NP接合PPDをILT方式CCDを開発(KODAK)

1987年 P+NP_{sub} 接合の電子shutter 機能付きHADをILT方式CCDカメラを開発(SONY)

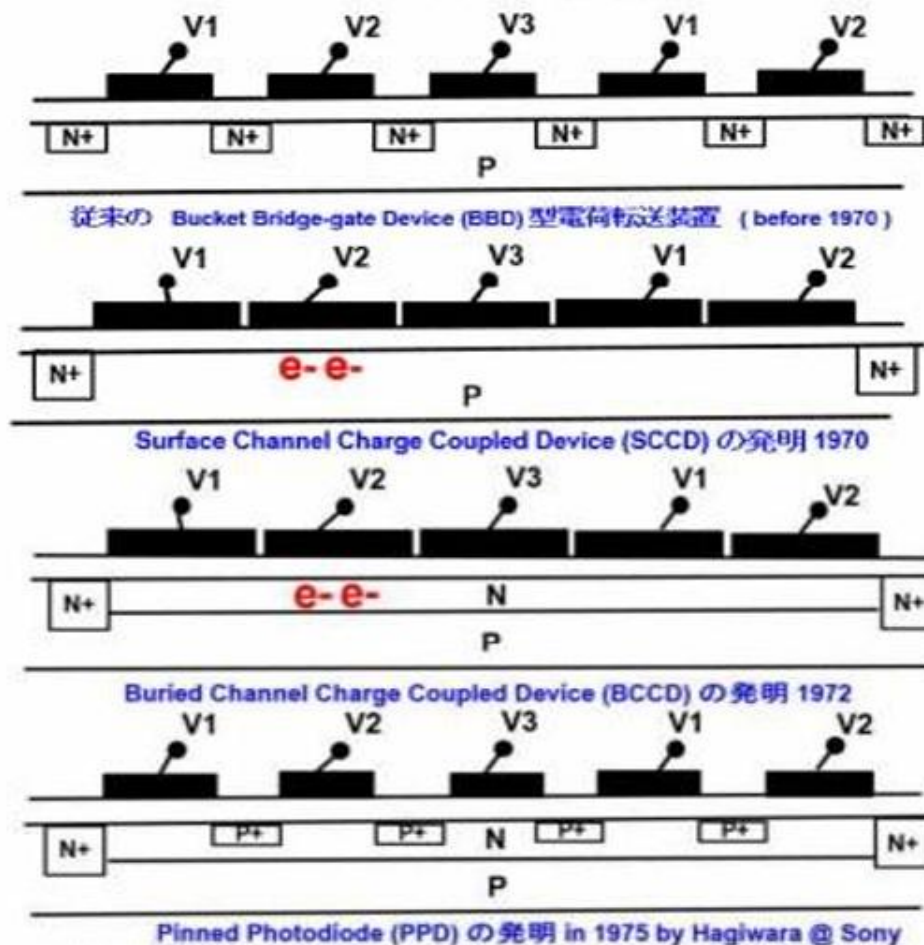
2020年: 撮像・演算 1 チップ化 & 3次元

集積回路の実現: 自動運転に応用



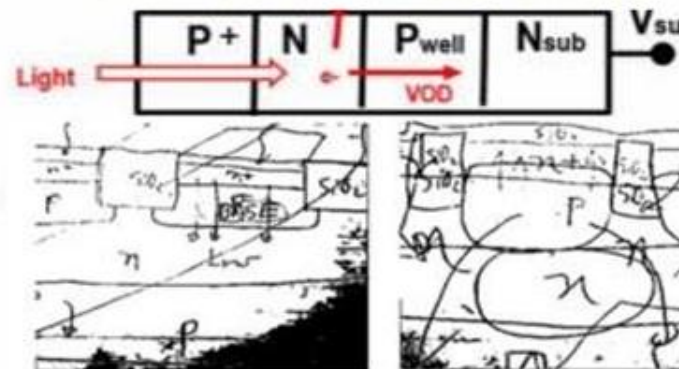
出典: テスラ

2. イメージセンサの歴史と市場動向

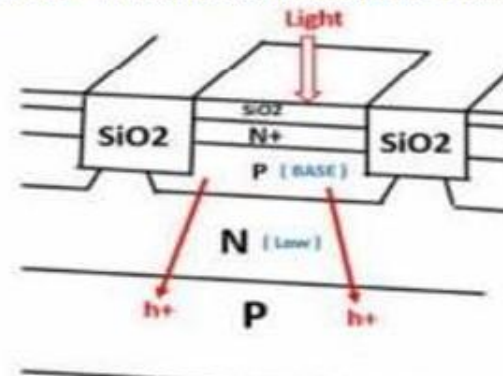


●P+NPsub 接合型HAD受光素子 (JAP 1975-134985)

萩原(1975) 基板(Nsub)にP+NP接合を形成する。



Hagiwara Lab Note at Sony February 1975 on the N+PNP type Pinned Photodiode with Shallow Trench SiO2 Isolation and the N+ channel stops beneath the oxide.



2. イメージセンサの歴史と市場動向

●イメージセンサーの開発背景(感度が命)

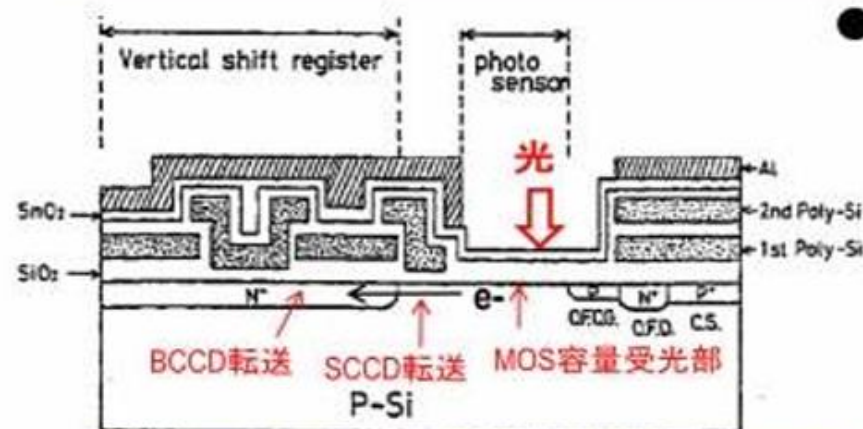
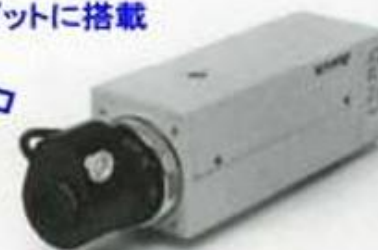
全日空ジャンボ機に2チップ構成カメラとしてソニーが商品化
ジャンボ機の離着時の様子を機内スクリーンに映し出す



XC-1 1980
Two-Chip Color Video
Camera

all solid state = robustness

ジャンボ機の
コックピットに搭載



●CCD/MOS容量型 Dynamic Photo Capacitor を
採用して完全電荷転送を実現して残像の
ない。高速撮影が可能な映像を実現した



<ICX008>

MOS 容量で受光して CCD 転送で 残像のない映像を実現した。

発明協会の公式WEBにも掲載

MOS カメラから CCDカメラへ、そして、CCDカメラからCMOSカメラへ

Interline 方式 CCD イメジャー

- ①光信号電荷のかたまり(charge packet)を各画素の接合容量に蓄積する。
- ②垂直CCD registerへの全画素(行と列)の同時露光一括読み出し。
- ③1行ごとに水平CCD registerに高速CCD転送modeで転送される。
- ④水平CCD registerの信号電荷を順次に最終段の出力回路で出力される。

(長所)出力段の端子容量Cが小さくてすむ。

容量 CkT 雑音が小さい。低照度でも雑音が少なく感度がよい。

(短所)転送効率に限界がある。CR充放電による消費電力が大きい。



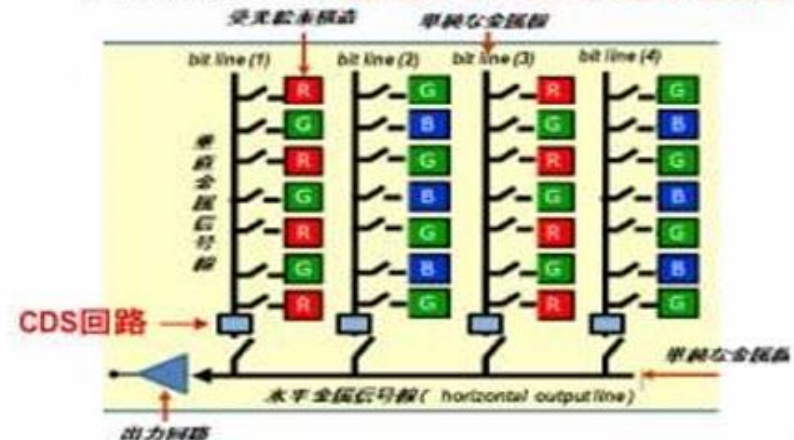
Active Pixel Amp 方式 CMOS イメジャー

- ①光信号電荷のかたまり(charge packet)を各画素の接合容量に蓄積する。
- ②各絵素のGlobal Shutter Memoryへの全画素(行と列)の同時露光一括読み出し。
- ③テレビの走査線と同期させて順次に各絵素の電流増幅回路(Active Pixel 回路)で信号増幅して金属線(bit line)へ出力する。信号が大きい。
- ④さらに(CDS=correlated double sampling) 回路でCLOCK雑音が除去され、大電流が水平信号線に出力。

(長所) CkT 雑音は大きいがそれ以上に信号が大きい。

絵素数に関係なく、大きな信号電流を得ることが可能。4Kや8Kなど高解像度映像に最適である。

CMOS Scaling 技術の進歩により、微細化が実現し、CR充放電による消費電力が小さい。(短所なし)。



MOSカメラから CCDカメラへ、そして、CCDカメラからCMOSカメラへ

まず、基本構造の材料となる
金属と絶縁体や、抵抗体と
半導体の性質を理解する。

SCCD 構造 と BCCD 構造 が
考案される前には BBD 構造
(バケツリレー転送)があった。
その開発背景はどうだったか？
結局 BBD 構造 が生き残った！

●いろいろな受光素子構造

光電子増幅管 (AI)
PIN photo diode (Si)
pinned photo diode (Si)
Avalanche Photo Diode (Si)
高周波数 FET (GaAs)
Gbps 光通信 (InGaAs)
光伝導Cell (CdS)

さらに原子構造から理解する！

II	III	IV	V	VI
	B ₅	C ₆	N ₇	O ₈
	Al ₁₃	Si ₁₄	P ₁₅	S ₁₆
Zn ₃₀	Ga ₃₁	Ge ₃₂	As ₃₃	Se ₃₄
Cd ₄₈	In ₄₉	Sn ₅₀	Sb ₅₁	Te ₅₂
Hg ₈₀	Tl ₈₁	Pb ₈₂	Bi ₈₃	Po ₈₄

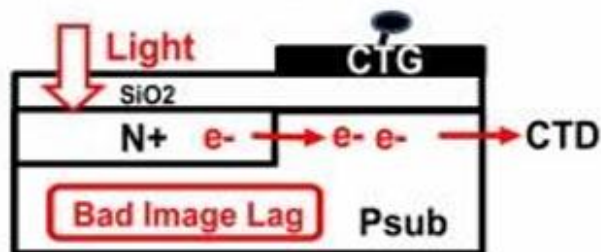
●いろいろな電荷転送素子 (CTD = Charge Transfer Device) の構造

BBD (Bucket Brigade Device)
PCD (Plasma Coupled Device)
CSD (Charge Sweep Device)
CID (Charge Injection Device)
CPD (Charge Priming Device)
CCD (Charge Coupled Device)
CMD (Charge Modulation Device)
BASIS (Base-Stored Image Sensor)
MOS image Sensor (Passive, Original)
CMOS image Sensor (Active Pixel Sensor)
AMI (Amplified MOS Intelligent Imager)

3. イメージセンサの基本構造

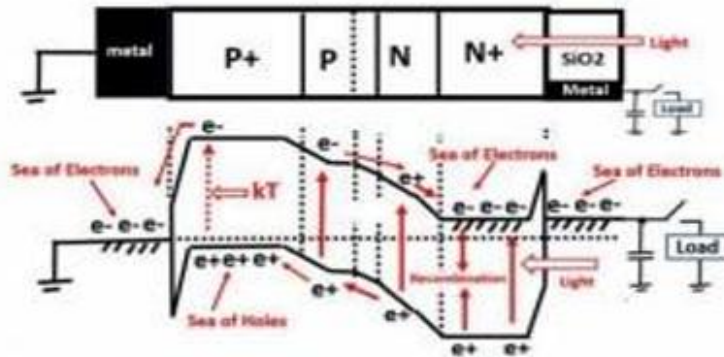
いろいろな受光素子構造

(1) N+P junction Photodiode in 1960s

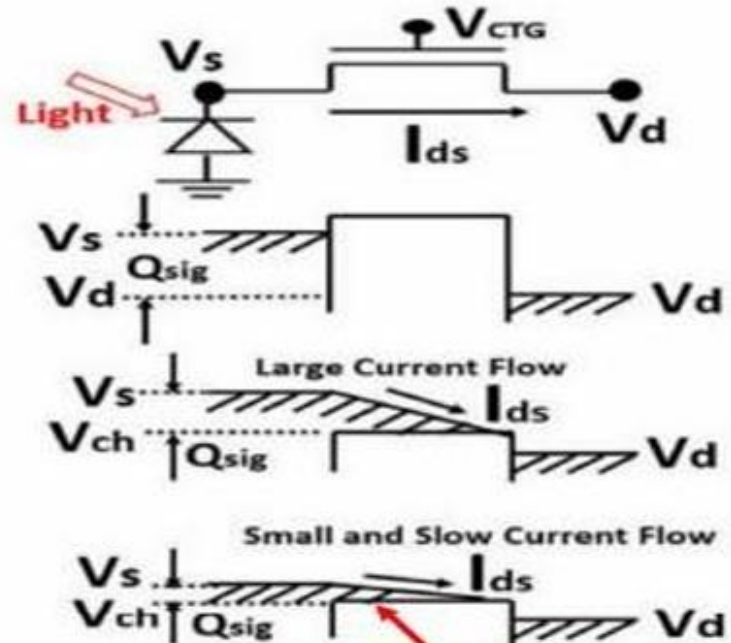


もうひとつの欠点

短波長青色光は空乏層に届かない



Single 接合 N+P 型 太陽電池は
量子効率が悪い~20%程度



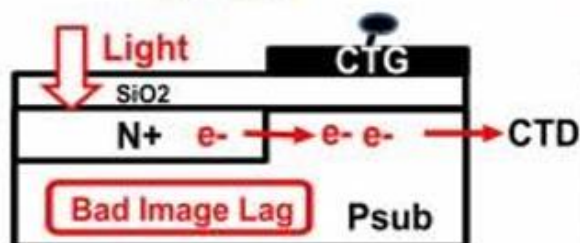
電荷転送電極の実行抵抗が
大きくなり S/D間の電流が少なく
残留信号電荷により残像がある。



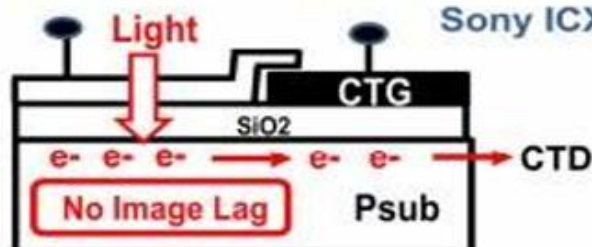
3. イメージセンサの基本構造

いろいろな受光素子構造

(1) N+P junction Photodiode in 1960s



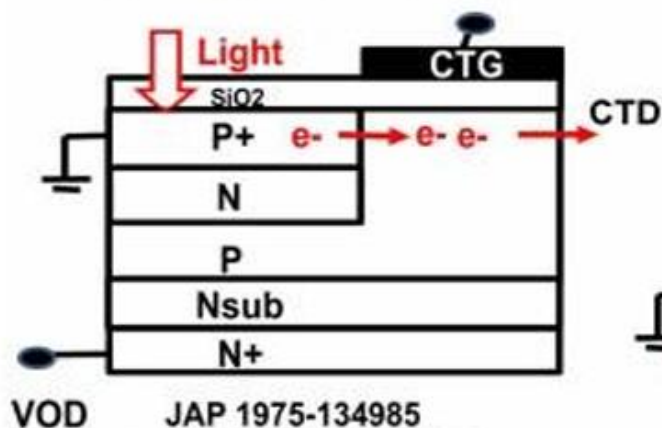
(2) Transparent Electrode CCD/MOS Photo Capacitor (1980)



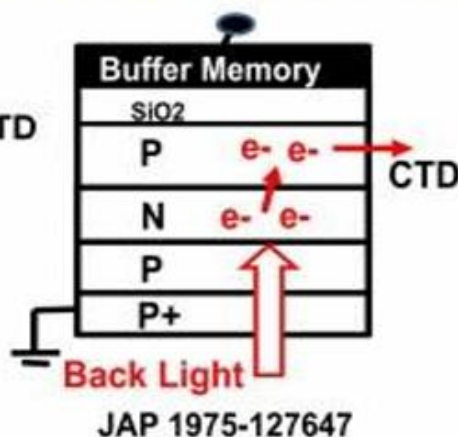
Sony ICX-008 CCD chips (1980)



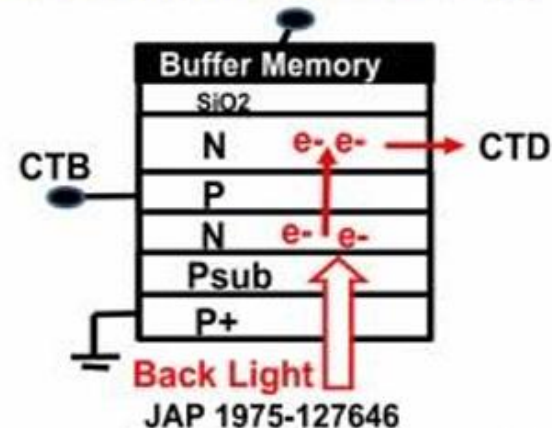
(3) P+NPNsub 接合型 Photodiode Hole Accumulation Diode (HAD)



(4) P+PNP 接合型 Photodiode Global Shutter Buffer MOS Memory



(5) P+PNPN接合型 Photodiode Global Shutter Buffer MOS Memory



4. イメージセンサの動作原理

●P+NPNsub 接合型HAD受光素子 (JAP 1975-134985)

萩原(1975) 基板(Nsub)にP+NP接合を形成する。

●NPNsub 接合型VOD受光素子 (JAP 1978-1971)

山田(1978) 基板(Nsub)にNP接合を形成する。

●PNPsub 接合型埋込み型受光素子 (JAP 1980-138026)

寺西(1980) 基板(Psub)にPN接合を形成する。



Comparison of Various Light Detecting Photo Sensor Structures

feature \ type	Classical N+Psub Photodiode	Surface Channel CCD	Buried Channel CCD	Yamada 1978 NPNsub	Teranishi 1980 PNPsub	Hagiwara 1975 PNPNsub
Blue Light Sensitivity	△	X	X	○	○	○
Low Image Lag	X	○	○	X	○	○
Surface Dark Current	○	X	X	X	○	○
Surface Trap Noise	○	X	○	X	○	○
Vertical OFD (VOD)	X	X	X	○	X	○
Electrical Shutter	X	X	X	X	X	○

3. イメージセンサの基本構造

表面照射型(1)

光集率が悪い

表面照射型(2)

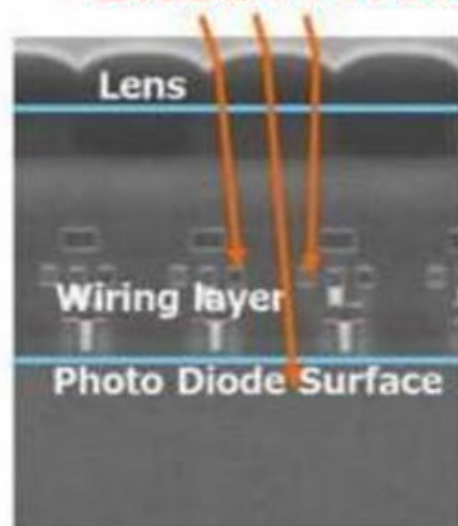
光集率の改善(光ガイド構造)

裏面照射型

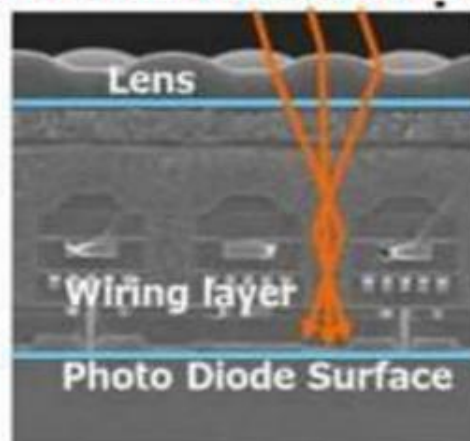
光集率の最適化(積層型集積回路の実現)

構造断面写真

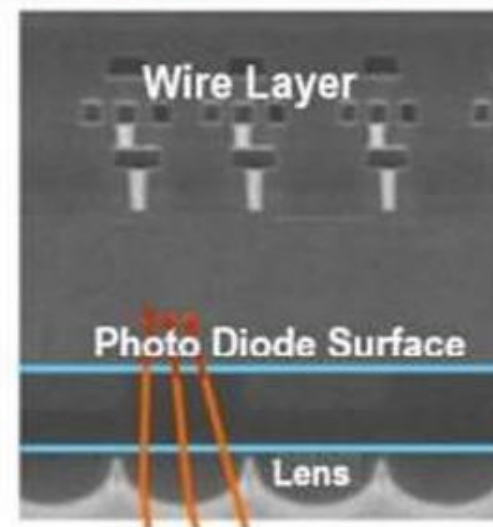
金属配線やトランジスタなどの回路が形成されている面を表面側と定義します。



表面照射型(1)



表面照射型(2)



裏面照射型

2. イメージセンサの歴史と市場動向

CMOSイメージセンサ(CIS: CMOS Image Sensor)産業は、急速に変化している。

携帯電話機市場と自動車市場にけん引されて、CIS市場は2014年から2020年の間に年平均成長率(CAGR)10.6%で成長し、2020年には200億ドル(2兆円)規模へと成長。大きなビジネスチャンスが出現した応用分野は、自動車と医療機器、そして監視カメラといったところである。安全性を高める用途だけでなく、イメージングを「自動化」する用途に使われるためだ。



2017年のCMOSイメージセンサ市場は前年比19%増の125億ドル規模に達した。(Insights調査報告)
2019年度のSONYのイメージセンサの売り上げは1兆円を超え、世界シェア50%以上に。

See <https://news.mynavi.jp/article/20190717-860632>

2. イメージセンサの歴史と市場動向

CMOSイメージセンサの製造企業

設計・製造技術の進化が CMOSイメージセンサの性能向上を推し進め、それにより CIS の応用事例にも 変化が生じている。スマートフォン が 小型カメラに取って代わり、そしてアクションカメラが ビデオカメラに取って代わってしまった。

2015年 ランク	2015年 シェア	2019年 ランク	2019年 シェア
(1) Sony	32%	(1) Sony	50%
(2) OmniVision	22%	(2)samsung	24%
(3) Samsung	19%	(3)OmniVision	14%
(4) Sharp	12%	(4)STMicoro	6%
(5) SK Hynix	8%	(5)Panasonic	1%
Others	7%	Others	5%
売上高合計	100% 62.5億 \$	売上高合計	100% 200億 \$



See <https://news.mynavi.jp/article/20190717-860632>

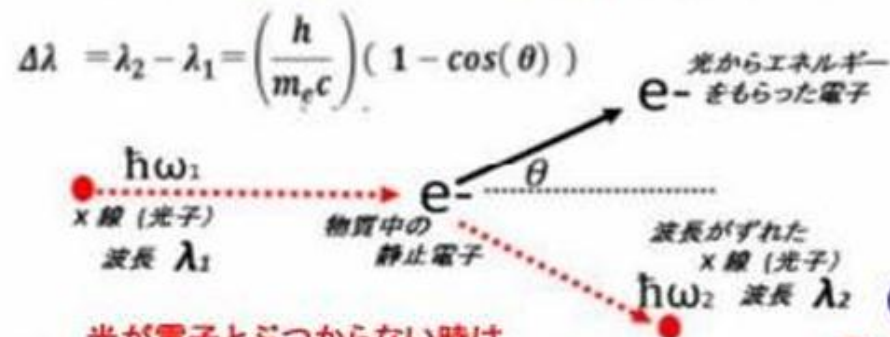
出典: イーサプライ

2017年のCMOSイメージセンサ市場は前年比19%増の125億ドル規模に達した。(Insights調査報告)
2019年度のSONYのイメージセンサの売り上げは1兆円を超え、世界シェア 50% 以上に。

4. イメージセンサの動作原理

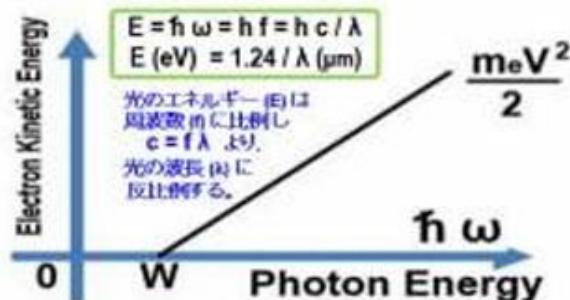
● 光は波でもあり、また粒子(光子)でもある (Albert Einstein 1900)

- 玉突きと同じ古典物理モデルで記述できる。
- 反射光の角度と波長の関係から電子の質量が求まる！



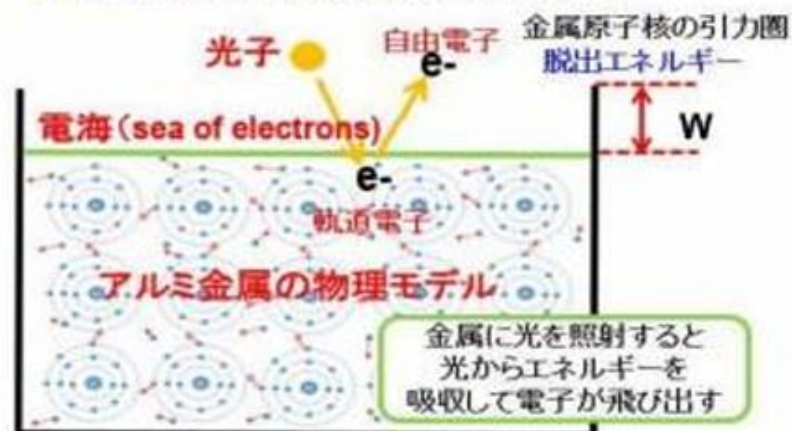
光が電子とぶつからない時は
 $\theta=0$ で光は直進し波長の変化はない。

光の速度 $C = 2.99792458 \times 10^{10}$ cm/sec
 Planck 定数 $h = 6.62606957 \times 10^{-34}$ Joule $\cdot$ sec
 電子の質量 $m_e = 9.10938291 \times 10^{-31}$ kg

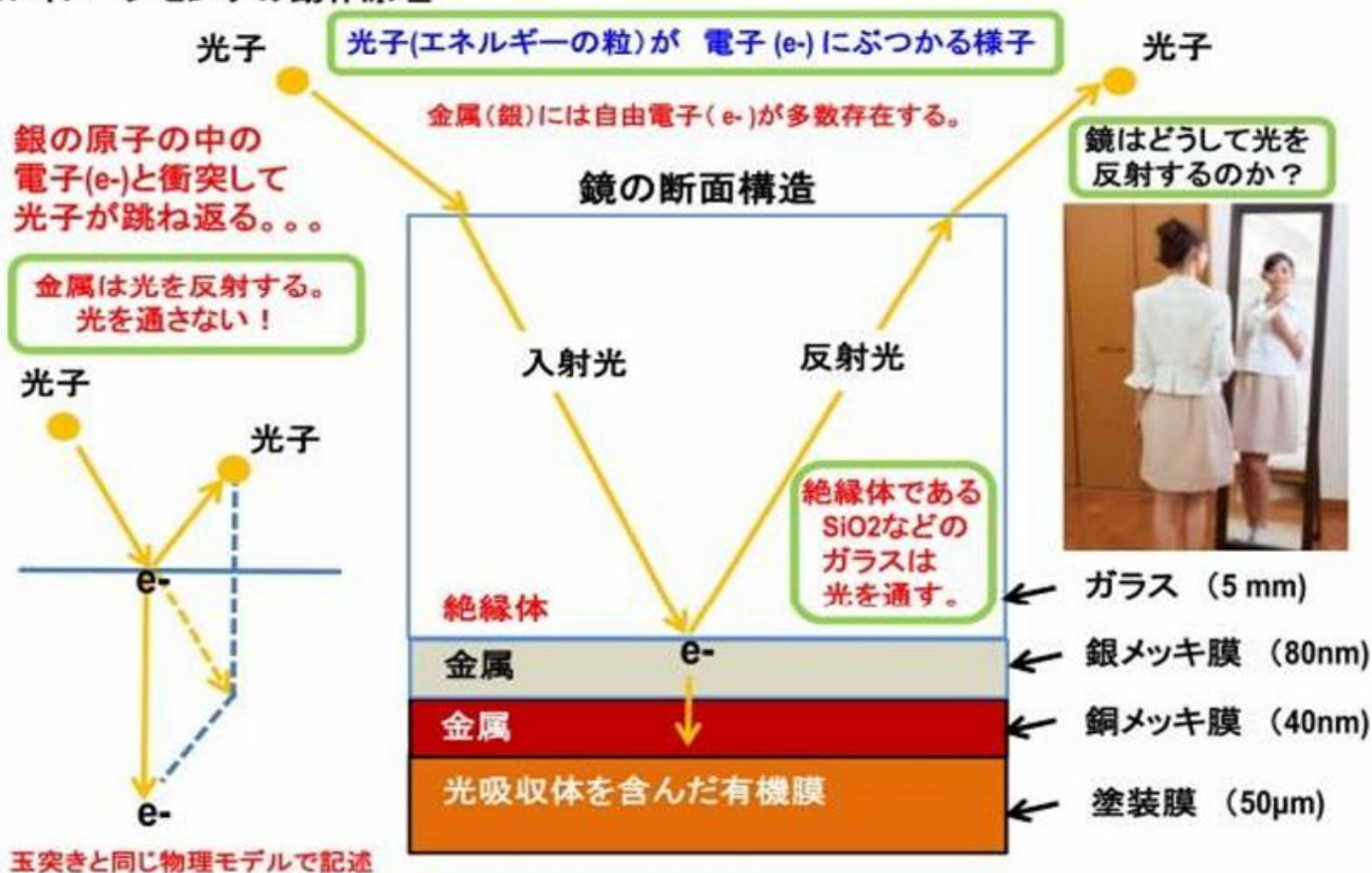


(脱出エネルギー) = 半導体の Energy Gap
 For Silicon, $E_g = 1.10$ eV and $\lambda = 1.12 \mu\text{m}$

- 金属の物理モデル (器の中に入った水モデル)



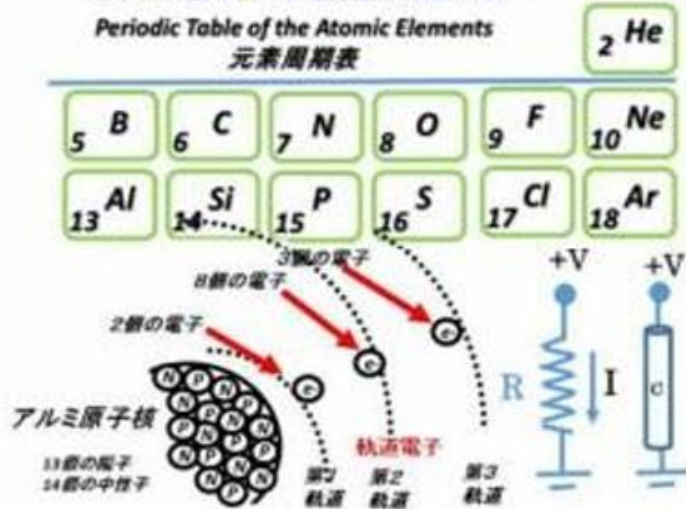
4. イメージセンサの動作原理



4. イメージセンサの動作原理

軌道電子の物理モデルは
地球や火星などの軌道惑星に類似する。

Periodic Table of the Atomic Elements
元素周期表



●自由電子は当然空間を自由に浮遊し移動する。しかし、結晶体の中でも、結晶体の原子核の引力圏の外では自由に電子は浮遊することができる。

●シリコン結晶体では、電子を1つ失ったシリコンイオン(Si^+)は隣接する中性のシリコン原子から電子を1つ盗み、中性にもどる。その電子を盗まれた、シリコンイオン(Si^+)は、また別の中性のシリコン原子から電子を盗む。ホールはこうして移動する。

●原子構造(原子核と電子)と太陽系(太陽と惑星)の類似

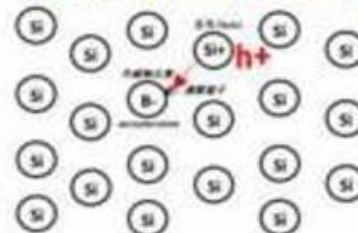
アルミ原子(中性) $_{13} =$ アルミイオン(Al^+) $_{12} +$ 自由電子(e^-)

シリコン原子(中性) $_{14} =$ シリコンイオン(Si^+) $_{13} +$ 自由電子(e^-)

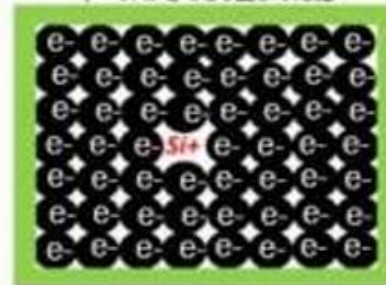
りん原子(中性) $_{15} =$ りんイオン(P^+) $_{14} +$ 自由電子(e^-)

ボロンの原子(中性) $_5 +$ 自由電子(e^-) = ボロンイオン(B^-) $_6$

P型半導体の物理モデル

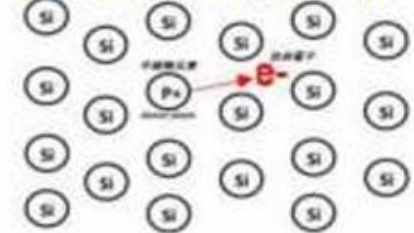


ボールがぶつちり回った跡



Holeが主役

N型半導体の物理モデル



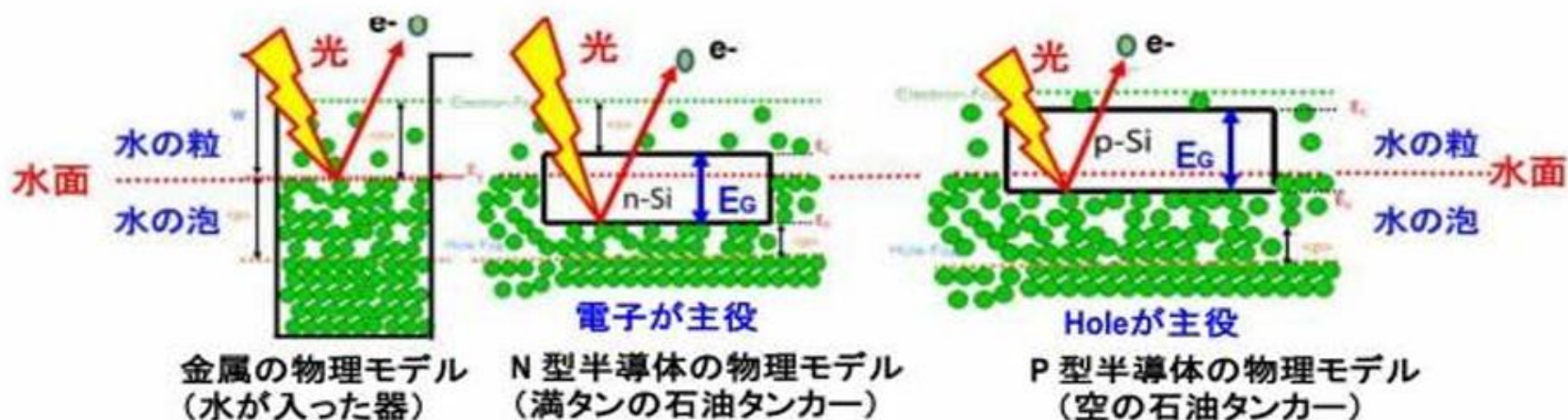
空っぽの箱



電子が主役

4. イメージセンサの動作原理

- 金属の物理モデルは、器に入った水にたとえる事が可能。
- N型半導体の物理モデルは満タンの石油タンカー船に、
- P型半導体の物理モデルは空の石油タンカー船に似ている。



$$E = \hbar \omega = h f = h c / \lambda$$

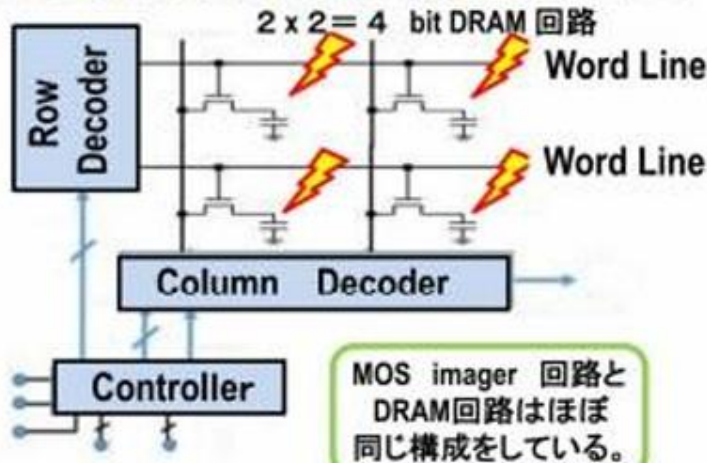
$$E \text{ (eV)} = 1.24 / \lambda \text{ (}\mu\text{m)}$$

For Silicon, $E_G = 1.10 \text{ eV}$ and $\lambda = 1.12 \mu\text{m}$

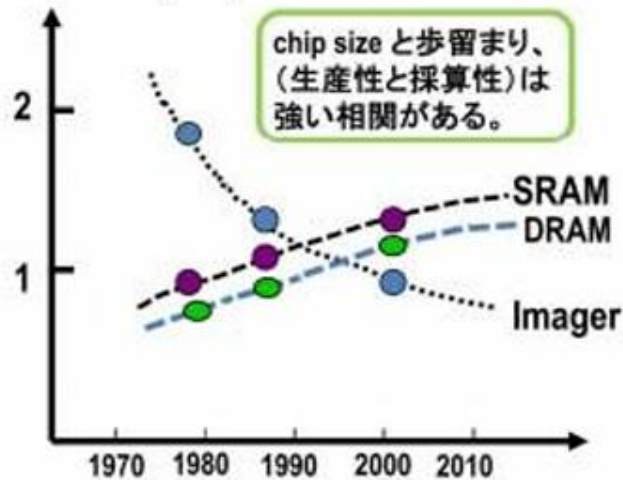
光のエネルギー (E) は周波数 (f) に比例し
 $c = f \lambda$ より、光の波長 (λ) に反比例する。

4. イメージセンサの動作原理

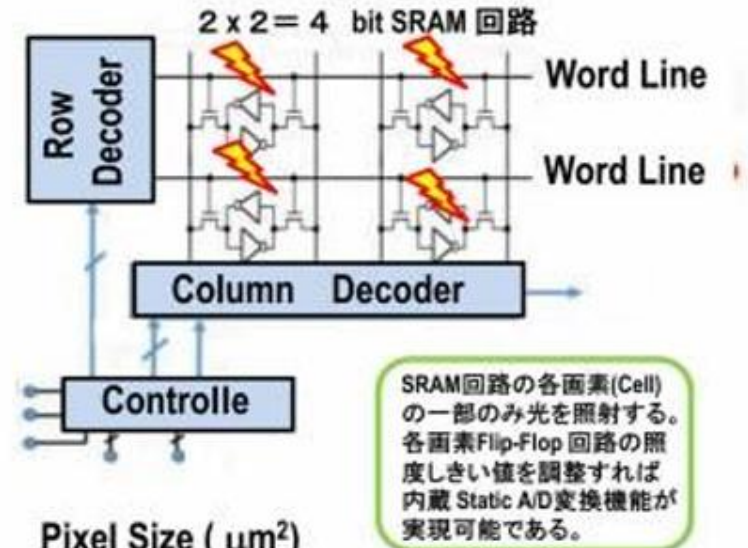
●1T1C型DRAM電荷転送 mode で動作する



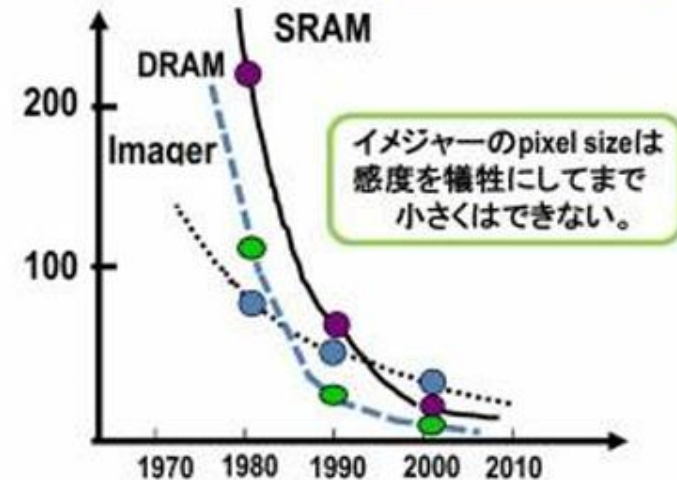
Chip Size (cm²)



●SRAM回路をアナログdata比較回路に使う

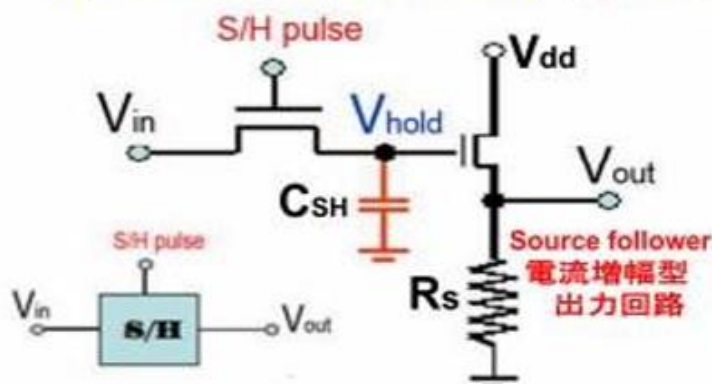


Pixel Size (μm²)



4. イメージセンサの動作原理

●CMOS イメージャー が有利になった理由は、最初は CCDイメージャーに応用された技術であった、S/H 回路を3個使う手法 (Correlated Double Sampling Hold 回路 by M. White, 1972) により、雑音が激減し実用に耐えるレベルになったことが大きい。



従来の Single Sampling Hold 回路

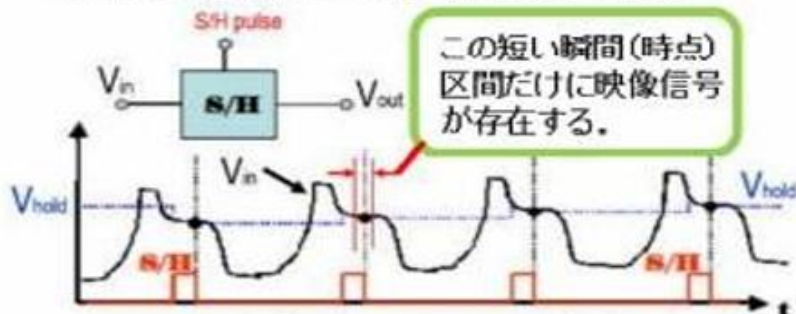
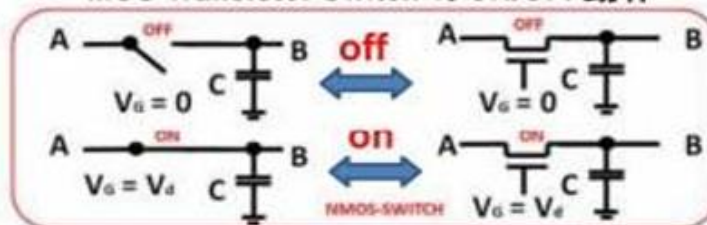
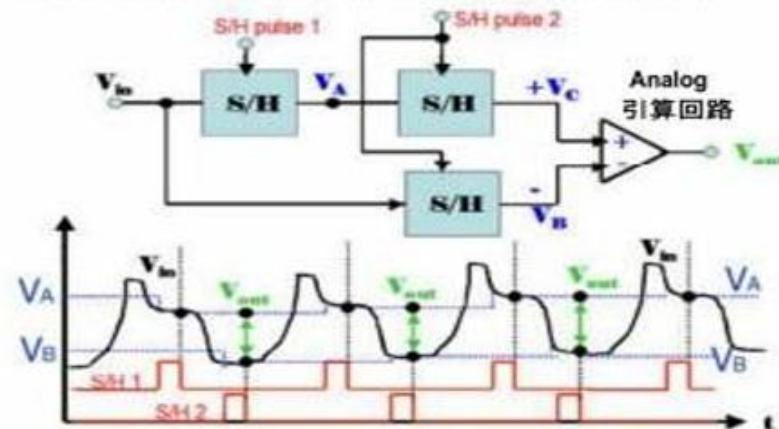


Image sensor の映像信号は雑音の中に埋もれている！

MOS Transistor Switch のON/OFF動作

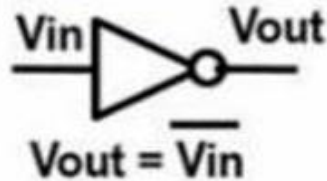


Correlated Double Sampling Hold 回路

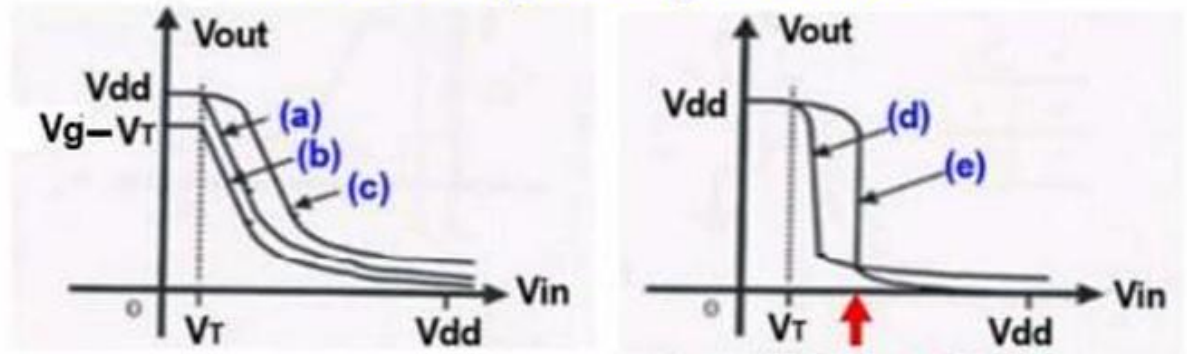


4. イメージセンサの動作原理

Inverter



Inverter Input Output Curves

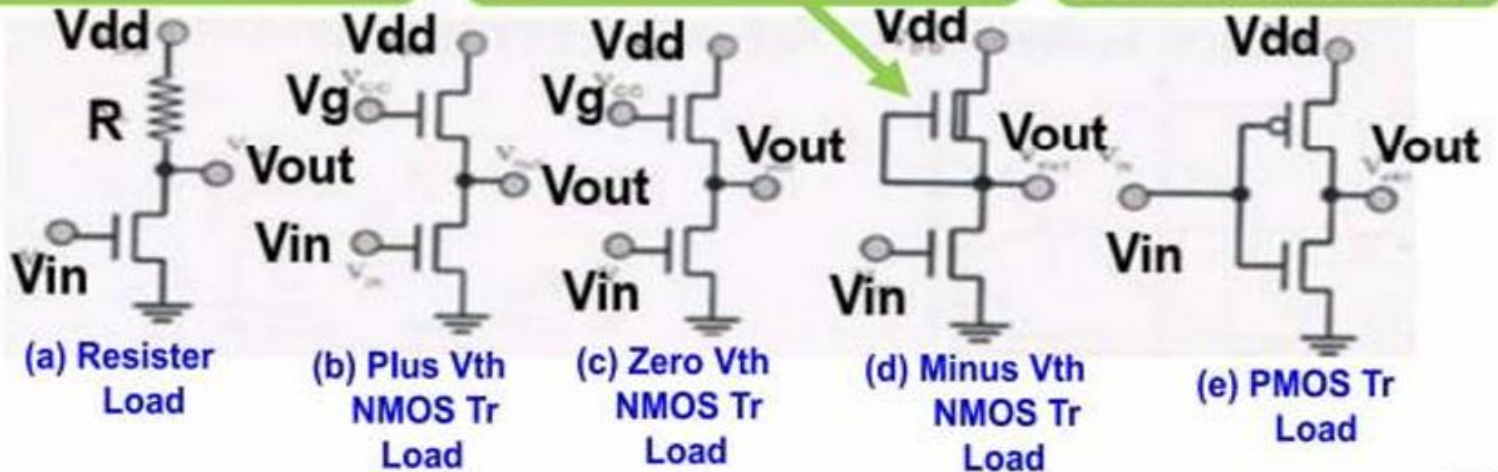


Logical $V_{th} = V_{dd} / 2$

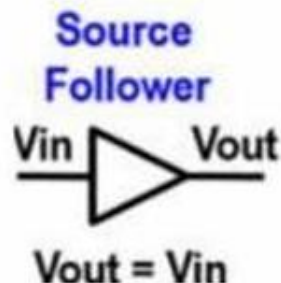
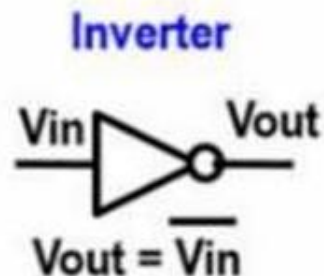
電流が流れている！

少量の電流が流れる

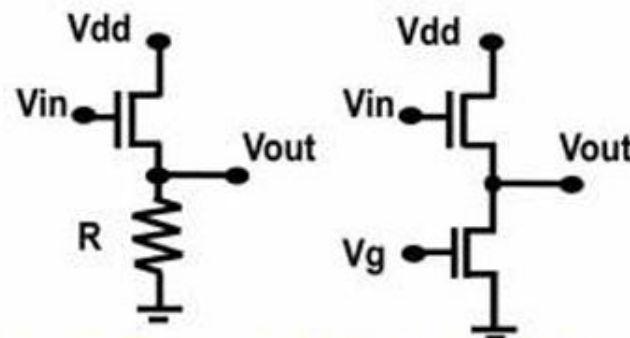
CMOS Inverter



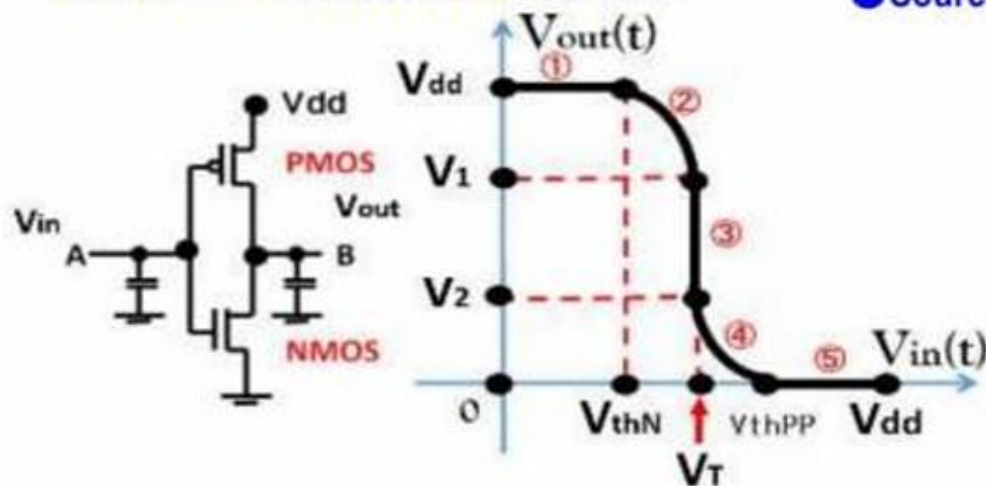
4. イメージセンサの動作原理



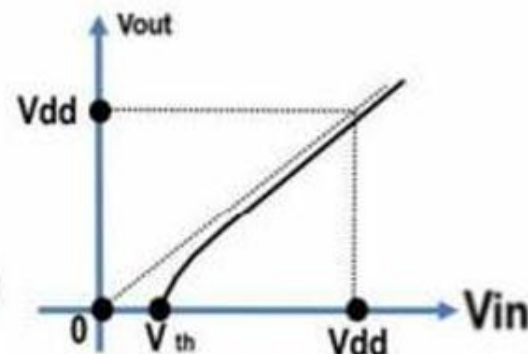
Source Follower Current Amplifier



● CMOS inverter回路の入出力特性



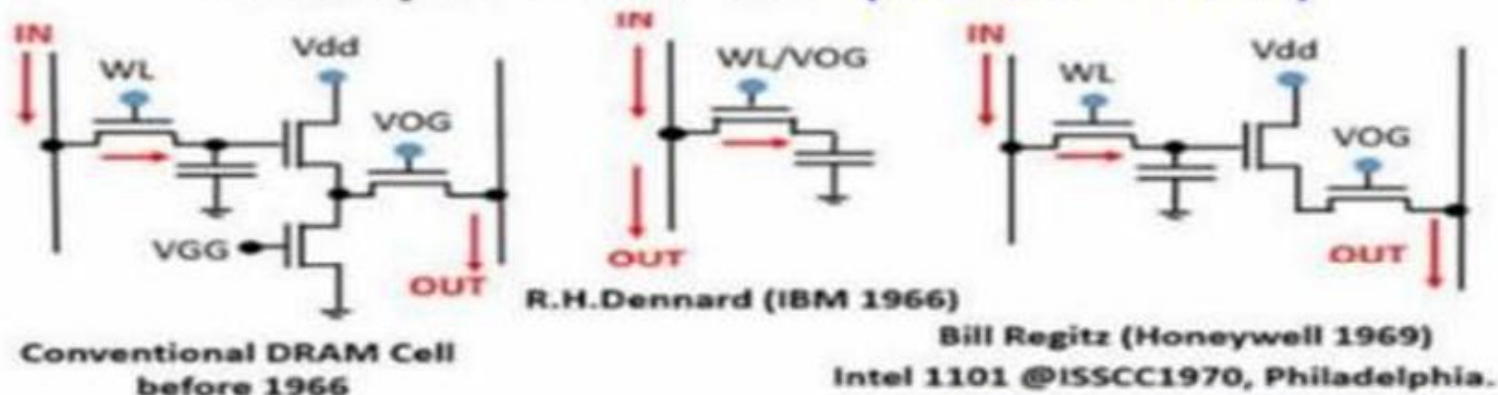
● Source Follower 回路の入出力特性



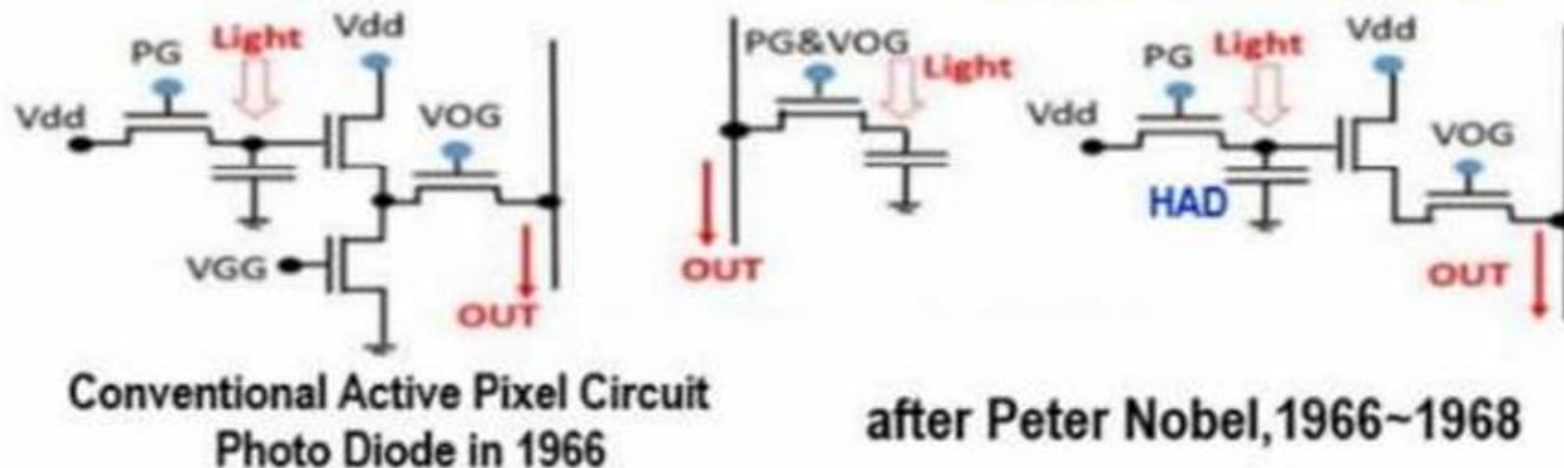
最終的に CMOS Inverter のみ生き残った。

4. イメージセンサの動作原理

History of DRAM Cell (Source Follower)



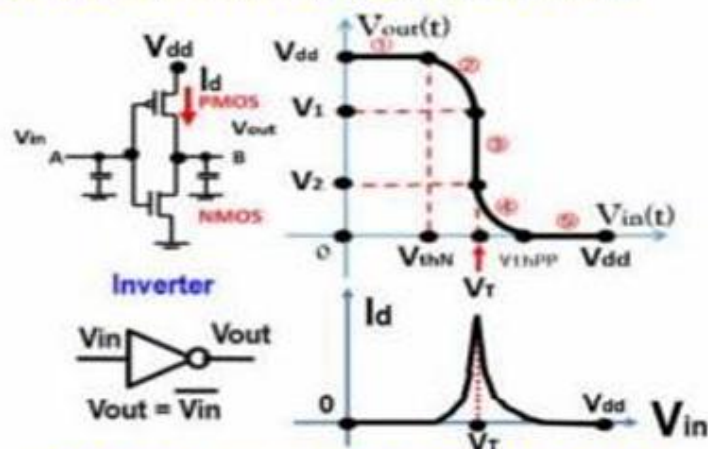
History of Photo Diode Cell (Source Follower)



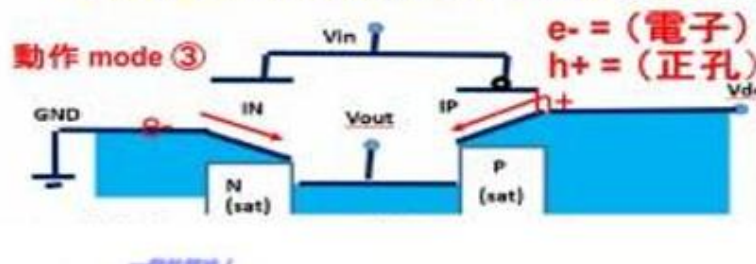
4. イメージセンサの動作原理

- CCDイメージャーより CMOSイメージャーが有利になった理由は、低消費電力のCMOS デジタル回路が使える為で、CMOS inverter回路特性から理解できる。

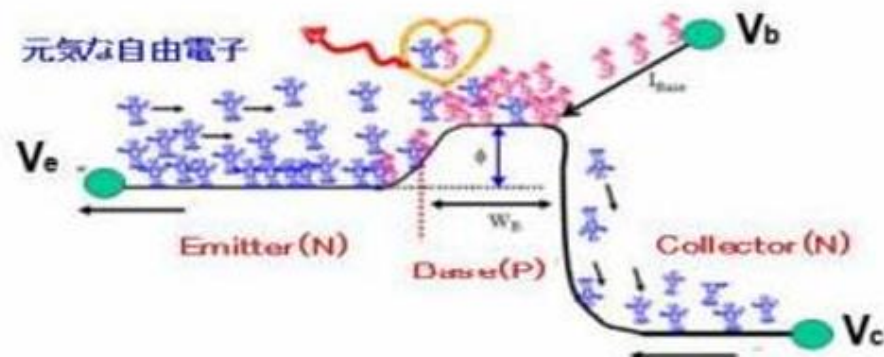
- CMOS inverter回路の入出力特性



- CMOS inverter回路の水門モデル

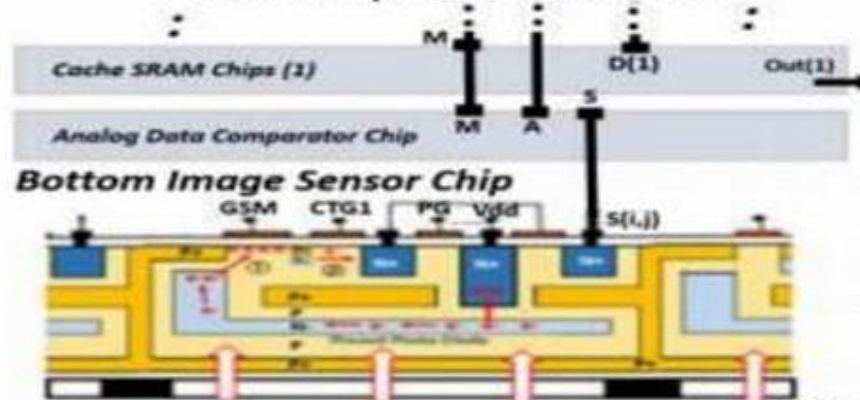


- NPN transistor の動作原理



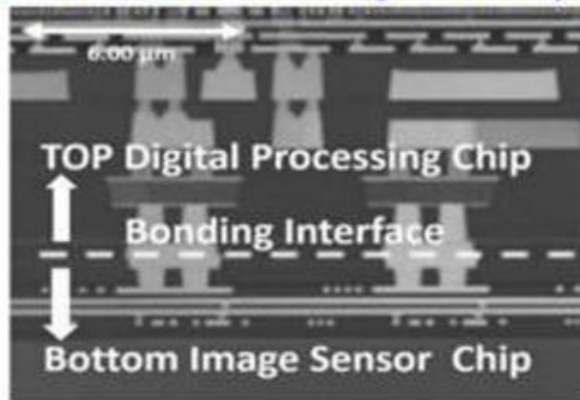
賢いイメージセンサーを支える技術は CMOS とBipolar の融合技術である。

2枚のchipを張り合わせる

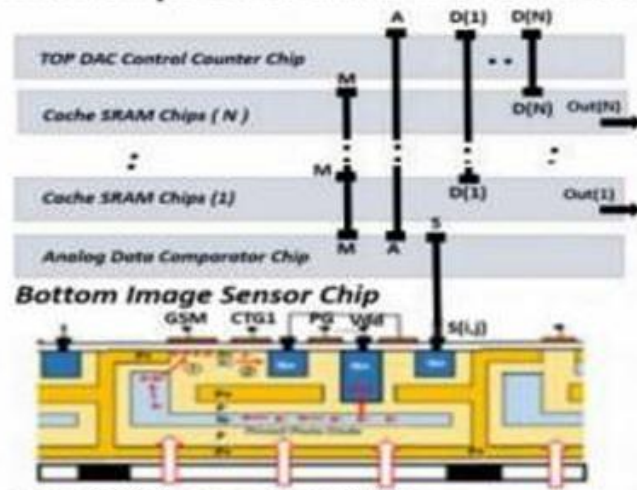


4. イメージセンサの動作原理

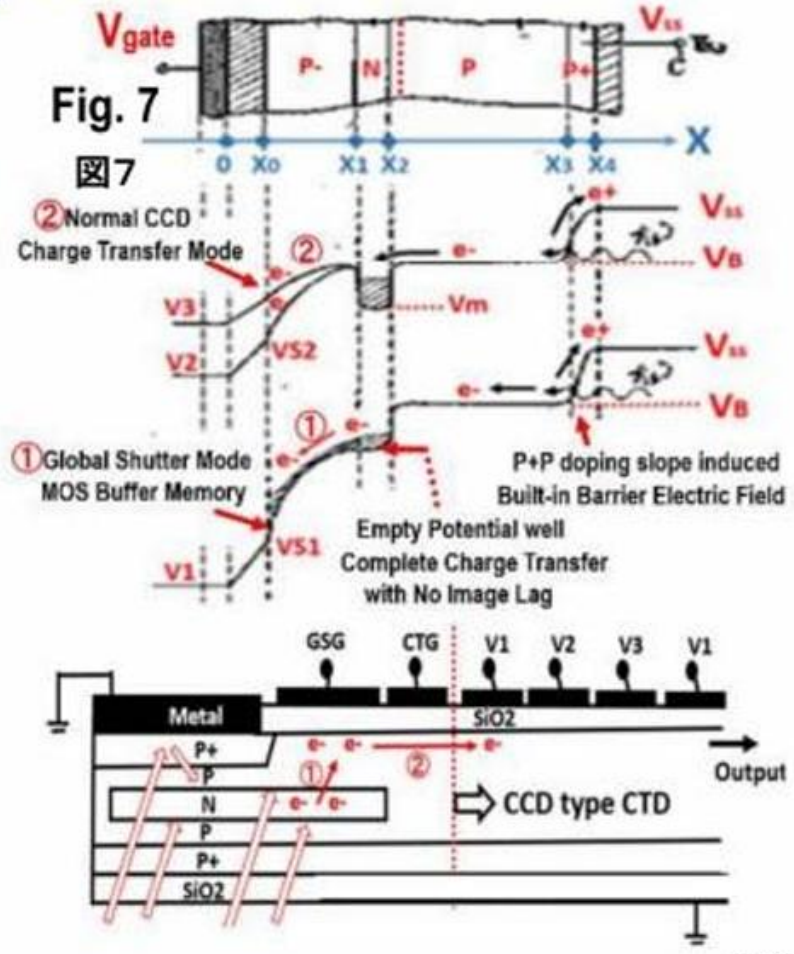
裏面照射型 CMOS Image Sensor (2020)



Multi-chips three dimensional LSI chip

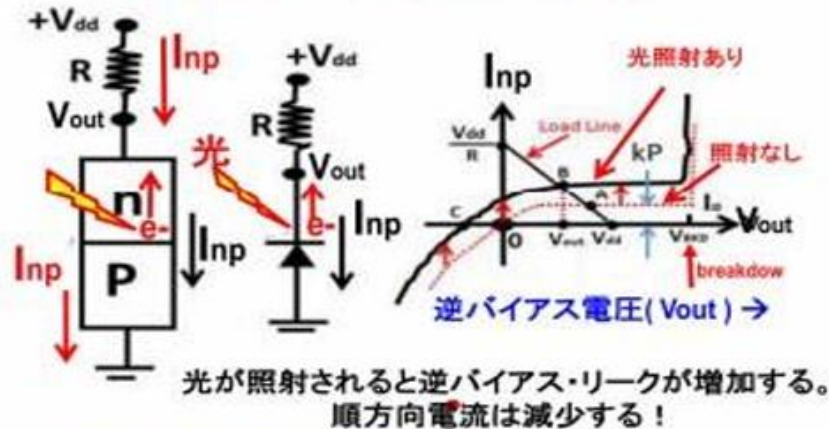


P+PNPP+接合型 Buried Pinned Photodiodeを採用した
裏面照射型 CCD Image Sensor (JAP 1975-127647)



4. イメージセンサの動作原理

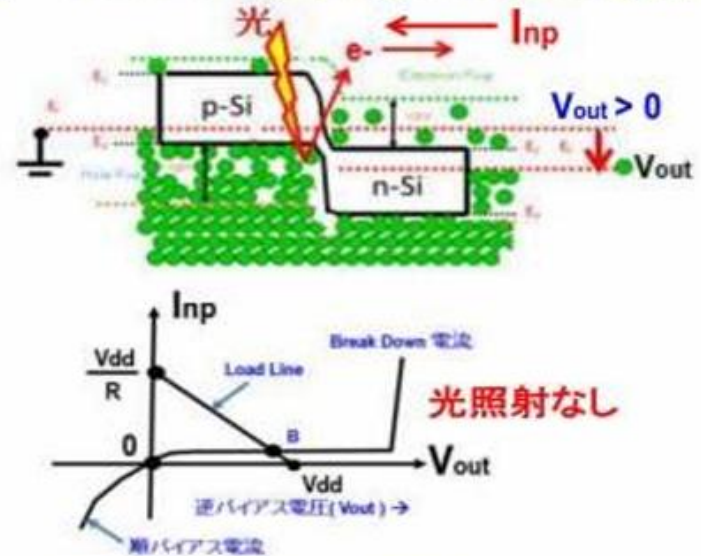
- イメージセンサーと太陽電池の動作原理は同じだが、
ただ受光絵素構造の個数と大きさが違う！



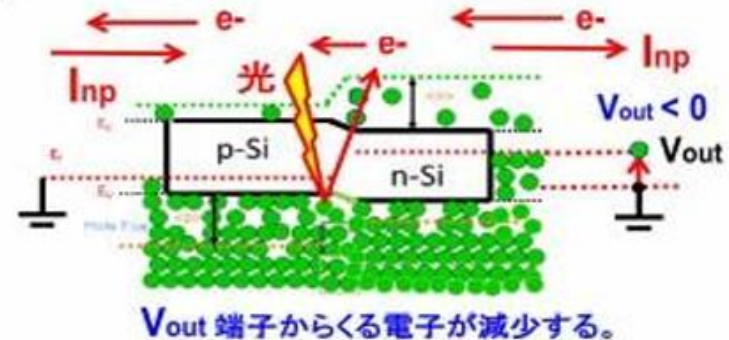
(1) NO バイアス mode の場合 太陽電池 mode



(3) $V_{dd} > 0$ 逆バイアス mode の場合

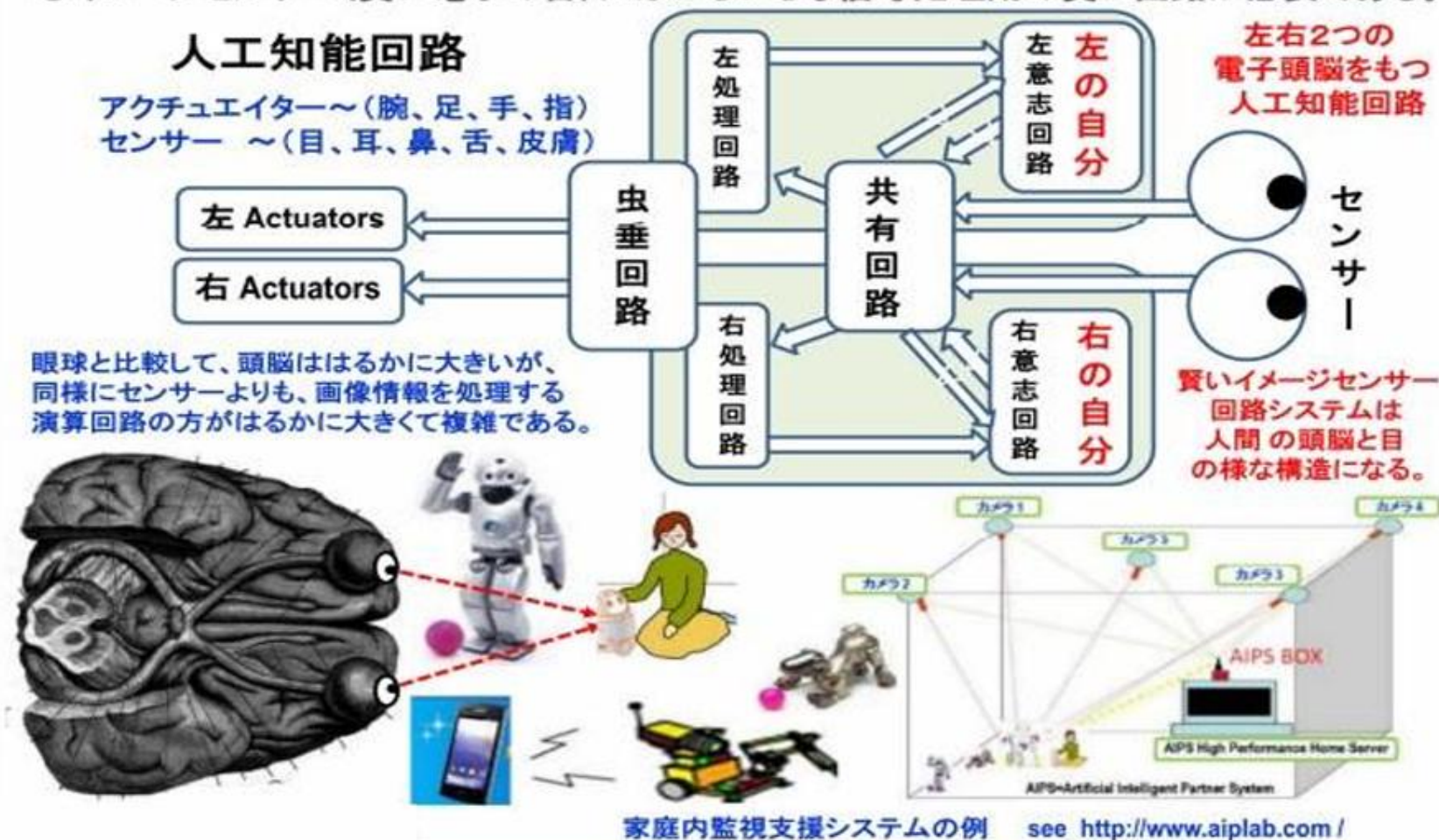


(2) $V_{dd} < 0$ 順バイアス mode の場合



5. 賢いイメージセンサーとは？

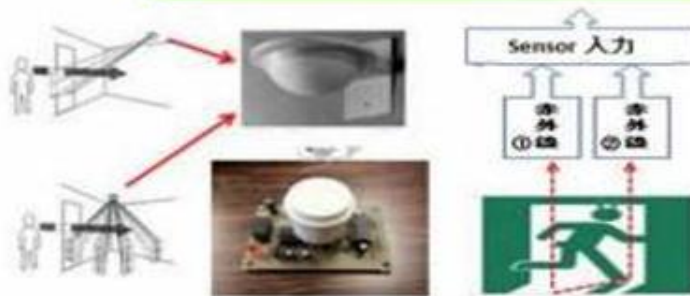
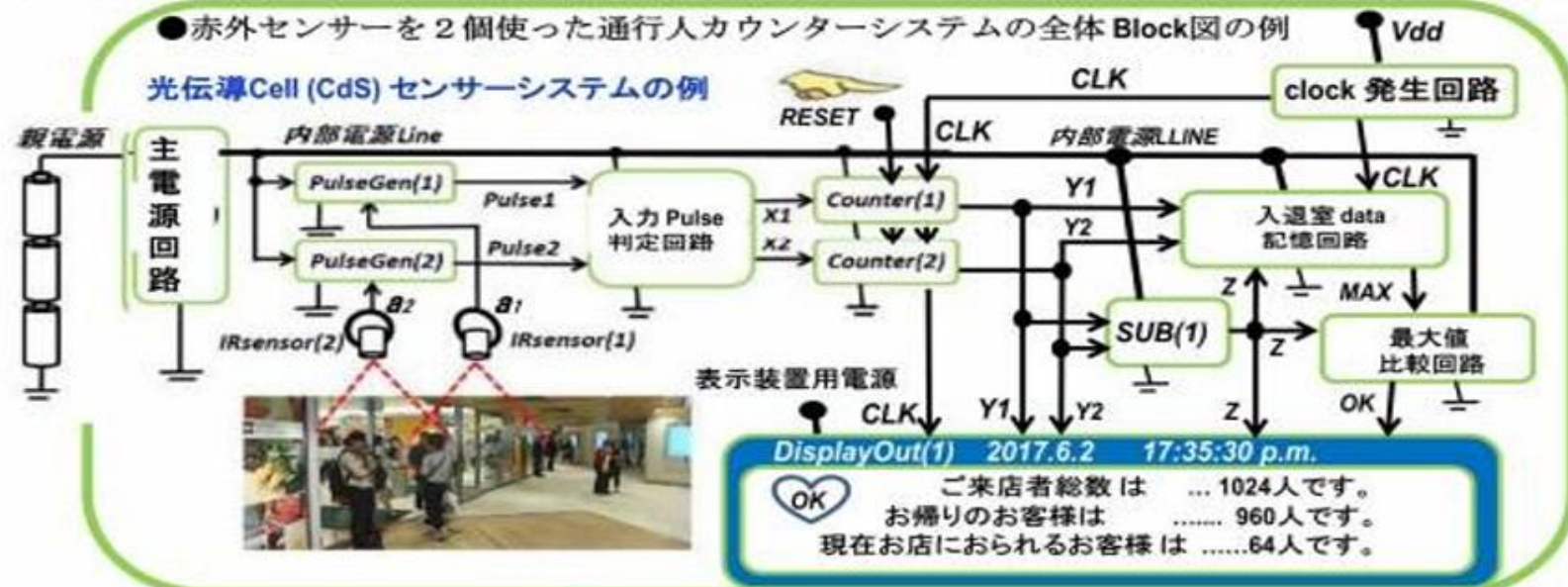
●イメージセンサー(賢い電子の目)にはいろいろな信号処理用の賢い回路が必要である。



5. 賢いイメージセンサーとは？

●イメージセンサー(賢い電子の目)にはいろいろな信号処理用の賢い回路が必要である。

●赤外センサーを2個使った通行人カウンターシステムの全体Block図の例



街中での通行人の映像



MOS カメラから CCDカメラへ、そして、CCDカメラからCMOSカメラへ

まとめ

Active in-Pixel MOS Image Sensor の1969年の発明は1970年のCCDの発明より早かったが、MOSの微細化技術の進歩を待つ必要があった。

開発実用化が初めて実現したのは1990年NHKの技研の技術者により実現した。その後CMOSデジタル回路の進化により絵素ごとにin-Pixel Amp回路だけでなく、CDS回路やADC回路がカラムごとに、組み込まれて、現在の省電力のCMOSデジタル出力処理回路が実現した。

理解度アップの基本復習問題

- 受光素子とは何か？
- 電荷転送装置 (CTD) とは？
- 感度 (Sensitivity) とは？
- CCD Image Sensor とは？
- CMOS Image Sensor とは？

参考技術書のご紹介

「イメージセンサーの本質と基礎」

黒田隆男 著
コロナ社 A5版 199頁
ISBN978-4-339-00845-6

「固体撮像素子の基礎」

安藤隆男・菰淵寛仁 共著
日本理工出版会 A5版 上製 246頁
ISBN4-89019-193-3

「CCD/CMOS イメージ・センサの基礎と応用」

米本和也 著
CQ出版社 A5版 271頁
ISBN4-7898-3626-6

「CCD/CMOS カメラの原理と実践」

安藤幸司 著
オーム社 A5版 214頁
ISBN978-4-274-06851-5

人工知能パートナーシステム(AIPS)を支える 「デジタル回路の世界」

萩原良昭 著
青山社 B5版 上製 475頁
ISBN978-4-88359-339-2

MOS カメラから CCDカメラへ、そして、CCDカメラからCMOSカメラへ

- 賢いイメージセンサーは、正確にすばやくまわりの動きを感じとる(感度)だけでなく、雑音や不要な情報を排除し(フィルター機能)、必要な情報だけを抽出加工し(情報認識)、人間支援のための知的処理を敏速に実行する。

賢いイメージセンサー実現のためのさらなる検討努力項目

●Dark Current (暗電流)の低減努力

- (1) 拡散電流
- (2) 発生電流
- (3) 表面リーク電流
- (4) トンネル電流

●量子効率の向上努力

- (1) 素子表面での入射光の反射
- (2) 小数キャリアの表面再結合
- (3) 光電変換領域以外での光吸収
- (4) 空乏層内でのキャリアの再結合

●雑音(ランダム)の低減努力

- (1) ショット雑音
- (2) 熱雑音
- (3) Avalanche過剰雑音
- (4) $1/f$ 雑音
- (5) reset雑音

●High Beam (overflow, blooming)抑制機能

●固定パターン雑音の低減努力

- (1) Clock雑音
- (2) Amp Offset 雑音
- (3) 画像欠陥(画素開口形状むら、Photo Diode 部暗電流むら、転送部暗電流むら)

●制御処理回路による性能改善努力

- (1) Correlated Double Sampling 回路
- (2) APS (Active Pixel Sensor) 回路
- (3) AMI (Amplified MOS Intelligent) 回路

●賢いイメージセンサー実現のためのその他の努力改善項目

- (1) PN 接合容量に光を照射する
- (2) MOS増幅回路処理、ガンマー補正処理
- (3) 出力信号の選択処理
- (3) A/D変換回路処理
- (4) 出力信号の伝達処理
- (5) 信号情報の記憶保存回路処理

MOS カメラから CCDカメラへ、そして、CCDカメラからCMOSカメラへ

Image Sensor の発明と開発背景に関する参考文献

Japanese Patent JPA 1977-126885 on Electrical Shutter Clocking Scheme invented by Y. Hagiwara, S. Ochi and T. Hashimoto in 1977.

公開特許公報 (A) 昭54-51318

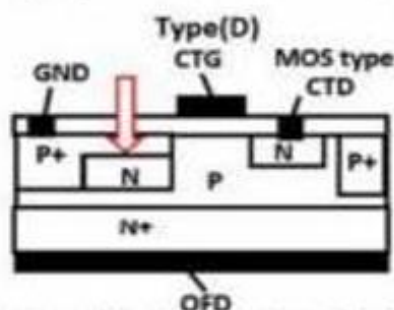
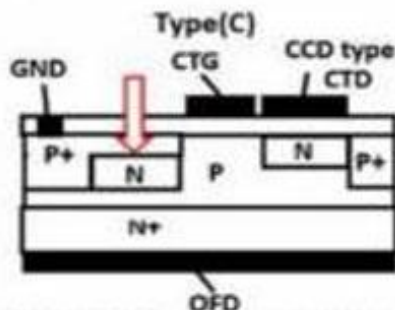
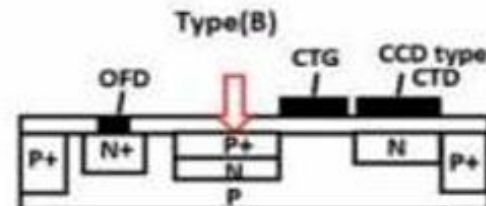
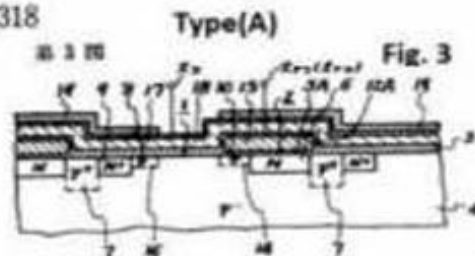
特 願 昭52-126685

出 願 昭52(1977) 9 月29日

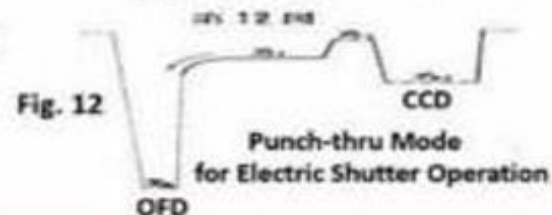
公開 昭和54年(1979) 4 月23日

発 明 者 萩原良昭

発 明 者 越智成之
同 橋本武夫



The electric shutter clocking scheme with the complete signal charge draining of no image lag can be achieved by the OFD punch-thru voltage control for any photodiodes, including not only the type (A) of the conventional CCD/MOS photo capacitor but also (B), (C) and (D) type Pinned Photodiodes.



MOS カメラから CCDカメラへ、そして、CCDカメラからCMOSカメラへ

Artificial Intelligence in Robot Vision



Mighty ATOM
/ ASTRO BOY © Osamu Tezuka



WALL-E © 2008 The Walt Disney Studios



理解度アップの基本復習問題

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- 感度 [Sensitivity] とは？
- CCD Image Sensor とは？
- CMOS Image Sensor とは？

hagiwara-yoshiaki@aiplab.com
<http://www.aiplab.com/>



人工知能パートナーシステム (AIPS) を支えるデジタル回路の世界 | 青山社

私がはじめてBipolar Transistorの構造と動作原理を学んだのは母校Caltechで大学2年生の時、Feynman の物理の授業でした。



人工知能パートナーシステム(AIPS)を支える デジタル回路の世界

IEEE Life Fellow, Ph.D.

萩原 良昭 著

ISBN978-4-88359-339-2 B5判 上製 475頁

定価(本体9,000円 + 税)

未来の人間社会には人工知能パートナーシステム(AIPS)とも言える人間にやさしい支援システムが出現すると期待している。AIPS搭載の自動走行車や老人介護システム、人間型歩行ロボットやロボット・ハウスなどである。そこで本書では、そのAIPSを支える「デジタル回路の世界」と題し、ハードとソフトの両面で、人とコンピュータをつなぐデジタル技術について紹介している。図や絵をたくさん用意して、基礎からやさしく解説している。

“Water and Solar Energy for all people on the earth.”

Yoshiaki Daimon Hagiwara, AIPS

Love is sharing ♥



2026年9月15日(火) 開催 DAFSユニバーシティ委員会主催

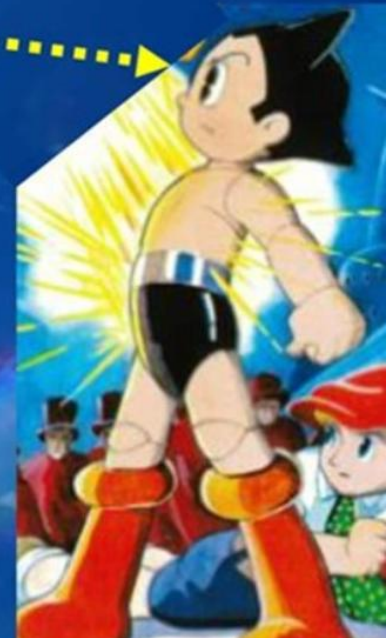
『AIロボティクスセミナー』

人工知能搭載AIロボットに不可欠な半導体部品の紹介

半導体産業人協会（SSIS）教育委員会委員 萩原良昭 講師

鉄腕アトムは半導体部品で構成され創られています。
鉄腕アトムの賢い電子の目は太陽の光を吸収して
光エネルギーを電気エネルギーに変換します。
鉄腕アトムの賢い電子の目は太陽電池でもあります。
賢い電子の目は半導体で造られます。

半導体とは？



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[2026_09_15_DAFSユニバーシティ_TEXT_SSIS_教育委員会_萩原良昭講師.pptx](#)