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**Past, Presence and Future Applications of Buried-channel Double-junction Sony Hole Accumulation Diode (HAD) type Image Sensors and Solar Cells with Pinned Surface and Empty Potential Well.**

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0-01 Thank you very much, Prof. Haruo Kobayashi.

0-02 This slide shows some of high lights of my talk.

0-03 This is the abstract of my talk.

0-04 And this slide shows the outline of my talk.

1-01 Now Introduction

1-02 This slide on the top shows a typical image sensor consisted of three parts. They are (1) Photodiode (2) Charge Transfer Device (CTD) and (3) Image Processor.

The first PNP double junction type buried-channel photodiode shown below was invented on June 9, 1975 by Philips. However, the surface p-region is connected only to the substrate ground level, and floating thru the high resistivity substrate with a large RC delay time, which is not perfect, not suited for high-frequency electronic shutter function nor suited for global-shutter function which is essential for CMOS image sensors.

1-03 This slide shows three types of pinned-surface and completely-majority-carrier-depleted buried-channel photodiodes without any image lag problem. The unit pixels, that is, image-sensor picture element cells, which have the electronic and global shutter function capabilities, which I invented in 1975, more than 50 years ago, at age 26 at Sony. The image sensors were hinted by Sony classical double and triple junction type bipolar transistor structures that Sony had developed and commercialized for Sony portable bipolar transistor radios in 1950s. My inventions would not have been possible without Sony Basic Bipolar Transistor Technology developed in 1950s.

2-01 Since my original inventions in 1975, after 50 years of R/D and business efforts, at Sony, young generations of Sony engineers have developed the advanced technology. And Sony is now enjoying the business of multi-chip 3DIC back-light illuminated CMOS image sensors.

2-02 This slide shows full schematics of one bit slice of a 128-bit high-frequency real-time data comparator unit element circuit block, that I would like to use and challenge to develop a new real-time AI robot vision chip. The simple NMOS silicon chip was originally designed and developed by Caltech students including myself in 1972 more than 50 years ago under the guidance of Prof. Carver Mead, which was then fabricated in Intel corporation. That was when I was a graduate student at Caltech in October 1971. Now I would like to apply this to realize AI robot real-time pattern recognition function capability, which can simply be implemented by a simple circuit block of one-bit input data line  $D[t]$  and one-bit key data line  $K[t]$  with one master data line  $M[t]$ .

2-03 By adding a few switching-pass and gating MOS transistors, this pinned-surface completely majority-carrier depleted P+PNPP+ double junction photodiode can be used also as a pinned-surface completely-depleted buried-N-channel P+PNPP+ double junction type solar cell.

2-04 In order to realize the high-frequency electronic shutter function, the surface of the PNP double junction buried-channel photodiode must be pinned and fixed directly by the surface grounded metal wire with no RC delay time. On the other hand, in order to realize the high-frequency global shutter function, we need an analog signal buffer memory capacitor, which can be simply made by a floating diffusion type N+P junction capacitor. However, this floating-surface N+P junction type capacitor has the serious image lag problem, or by the CCD type MOS capacitor invented by Bell lab in 1970 with the complete charge transfer capability and no image lag problem or the pinned-surface P+PNPP+ double junction capacitor which is my 1975 invention also with the complete charge transfer capability and no image lag problem.

2-05 This slide shows a circuit model of **(a)** the floating-surfacer N+NPP+ single-junction-type solar cell and **(b)** the proposed pinned-surface P+PNPP+ double-Junction solar cell in comparison. For the floating-surfacer N+NPP+ single-junction-type solar cell, all of the positively charged hole carriers generated by the photo-electron and hole generations by illuminated sun light must to pass thru the only high resistivity substrate while the proposed pinned-surface P+PNPP+ double-Junction solar cell has another surface P+P region for the positively charged hole carriers generated by the photo-electron and hole generations by illuminated sun light can be guided directly to the external grounded wire without any volage drop with no joule heat loss.

3-01 Now I would like to explain the difference of floating-surface single junction and pinned-surface double junction photodiodes.

3-02 This slide shows a band diagram of a floating-surface N+NPP+ single junction solar cell. For a low-concentration PN junction, we usually expect to have a large depletion width, which is needed for effective separations of photo electron and hole pairs. However, the extremely low concentration NP junction means a very high resistivity P substrate region and a very high resistivity floating-surface N region. Besides, in order to have the external metal-to-semiconductor ohmic contact formations, the heavily doped N+ is needed for the N region at the surface while the P+ region is needed for the low concentration high-resistivity P substrate region at the back side. However, the impurity atom doping variation P+P and N+N both induce the barrier potential drops. And we have undesired voltage drops in the N+N and P+P regions. And we do not expect much of potential drops inside the low concentration NP junction. Consequently, we have a flat NP junction potential with not much electric field inside the PN junction. We cannot expect any effective photo electron and hole pair separations inside the intrinsic semiconductors and the extremely low concentration NP junction.

3-03 This slide shows various types of solar cells.

3-04 Among them, for the simplicity and cost considerations, the simplest N+PP+ single junction type is now widely applied for solar cells. However, I am now proposing the P+PNPP+ double junction Sony classical bipolar transistor structure type solar cell for doubling the depletion width as an alternative device for higher photo to electron energy conversion efficiency. This new device structure is very similar and attractive cost-wise with the conventional N+PP+ single junction type solar cell. All we need now is to add two more ion implantation steps. They are, one step of the P+P surface low-energy ion-implantation and another step of the high-energy ion implantation to form the deep buried-channel low-concentration N region which must be always completely-depleted of majority-carrier electrons to provide a free underground long passage for photo-generated energetic new electrons to be directed swiftly to the small outlet N+ diffusion region. In this way the same receiving output circuits can be utilized for both single and double junction type devices.

3-05 Since I do not have much time left, I would like to skip the detailed explanations of device and physical aspects of this new device that have been introduced and published in other publications. And let me scan quickly my slides. The audience can read and study the details from the publications listed in the reference list. Specially please see my recent papers such as titled “Dynamic Photo Transistors for Image Sensors and Solar Cells “, reported and published on November 2024 at the *2024 International Symposium on Integrated Circuit Design and Integrated Systems (ICDIS2024)* in China.

9-02 And now let me explain some of the important points such as the one shown in this slide. This slide shows the percentage of the sunlight energy density penetrating into the silicon crystal for various different wave length as a parameter. For an extremely long wave sun-light, a silicon crystal looks like a completely transparent and the light just pass thru the silicon crystal. However, a very short-wave, the sun light is blocked and cannot penetrate the silicon crystal more than 0.4 micro meter in depth. Summing all components for all wave length, we get the total sunlight energy penetrating the silicon crystal.

10-02 By so doing, we finally get the percentage of the total sunlight energy penetrating into the silicon crystal as shown in this slide. For an N+PP+ single junction solar cell, the typical and effective width of the depletion region is about from the silicon depth of 0.3 micro meter to the silicon depth of 2.5 micro meter, which gives the theoretical upper limit value of 26.2 % for the solar cell energy conversion efficiency, which is confirmed in real productions. If we can collect all photons from the silicon surface up to the silicon depth 3.5 micro meter in depth, we expect to have  $(80.3-32.7) \% = 47.6\%$ , which is the expected theoretical value for my P+PNPP+ double junction type solar cell.

13-02 Now conclusion. The buried-channel type charge coupled device (CCD) is not the only charge transfer device (CTD) that can transfer one single photo electron in the buried-channel N region. The pinned-surface buried-channel P+PNPP+ double junction photodiode that I invented in 1975 can also transfer one single photo electron in the buried-channel N region, which is completely depleted of majority carrier electrons. My invention in 1975 is now widely used CMOS digital image sensors. My 1975 replaced CCD image sensors completely in the high-definition high-frequency modern digital TV era and still have new application for high efficiency solar cells.

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## 13. Summary and Conclusion

13-03

The double junction solar cell also has also a small-area outlet N+ drain region to connect the solar cell with the external load and the identical external maximum power tracking technology (MPTT) can be applied. Besides, the buried-channel N region, completely depleted of both majority carrier electrons and minority carrier holes, can transport even one single photo electron without recombination in the silicon chip for a long distance, directing photo electrons toward the small-area outlet N+ diffusion region, and very suited for high performance solar cell applications.

A new AI smart robot vision chip in the modern 3DIC CMOS image sensor technology is proposed, which is composed of an array of  $N \times N$  pinned-surface buried-channel P+PNPP+ double junction type photo diodes,  $N \times N$  analog-data steam mask-and-match comparators, and SRAM cache buffer CMOS memory units. All of them are integrated in a 3-D multichip system with the original 1972 basic architecture designed by Caltech EE graduate students.

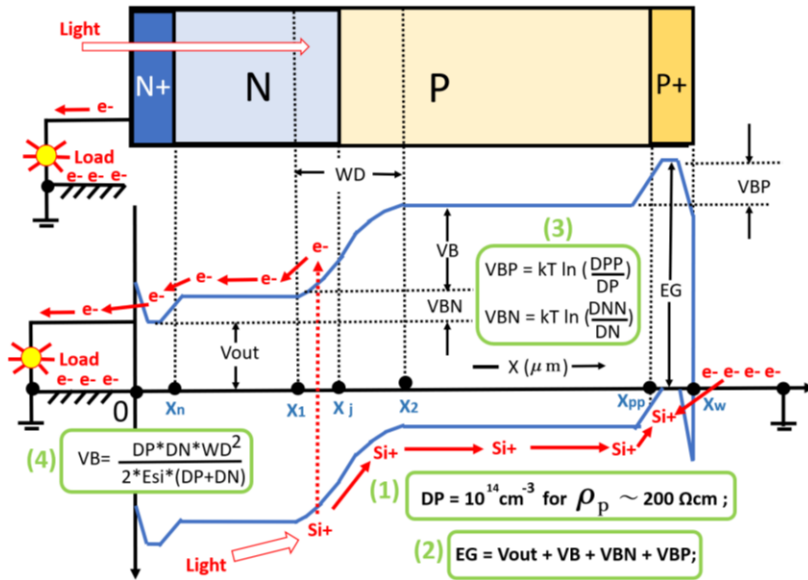
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### 13. Summary and Conclusion

In the external power-off mode, as an AI self-energy robot vision chip, the image sensor array of  $N \times N$  pinned-surface buried-channel P+PNPP+ double junction type photo diodes can also function as a solar cell energy source unit. By a clever device and circuit design scheme, this array of  $N \times N$  pinned-surface buried-channel P+PNPP+ double junction type photo diodes also function as a solar cell unit for the AI self-energy robot vision chip application. This real-time super performance solar cell in the AI smart robot vision chip is in this 3DIC multichip architecture with a unique high-performance unit of the built-in solar-cell and image-sensor combined SONY Hole Accumulation Diode (HAD) sensor type solar device structure, which is based on the Sony original 1950s semiconductor process of the P+PNPP+ double junction dynamic bipolar transistor technology with a charge transfer device unit which is based by the modern scaled CMOS 3DIC digital multichip process technology that Sony and many competing companies are developing.

The floating-surface single-junction N+NPP+ junction type photodiode with a typical depletion width  $W_d = [X1, X2] = [0.2, 2.0]$  gives the efficiency of about  $66.8 - 40.0 = 26.8\%$ . However, in case of the P+P pinned-surface completely-depleted buried-channel Sony Hole-Accumulation Diode (HAD) sensor type solar cell, utilizing the high-energy ion implantation technology, if we achieve the depletion depth of  $X2 = 3.0 \mu\text{m}$ , then, the solar cell efficiency of  $80.4 - 34.7 = 45.7\%$  is expected. This expectation must be urgently examined and tested by fabricating a real silicon chip.

For N+NPP+ Single Junction Solar Cel,  
Maximum Depletion Width  $WD=2.22 \mu m$  ;



\*\*\*\*\*  
 $EG=1.11 \text{ eV}$ ;  $kT=0.0259 \text{ eV}$ ;  $E_{si}=648 \text{ e}/(\text{V} \cdot \mu \text{ m})$  ;  
 $NC=10400000 \text{ e}/(\mu \text{ m})^{**3}$ ;  $NV=28000000 \text{ e}/(\mu \text{ m})^{**3}$  ;

\*\*\*\*\*

Demand {  $V_{out}= 0.3 \text{ V}$  ;  $DP=130$  :  $DN > DP$  : } , |

(1)  $V_{BPP}=(EG+kT \cdot \ln(NV/NC))/2=0.567826 \text{ eV}$  ;

(2)  $V_{BNN}=(EG+kT \cdot \ln(NC/NV))/2=0.542174 \text{ eV}$  ;

(3)  $DP=NV \cdot \exp(-V_{BP}/kT) - NC \cdot \exp((V_{BP}-EG)/kT)$  ;

(4)  $DN=NC \cdot \exp(-V_{BN}/kT) - NV \cdot \exp((V_{BN}-EG)/kT)$  ;

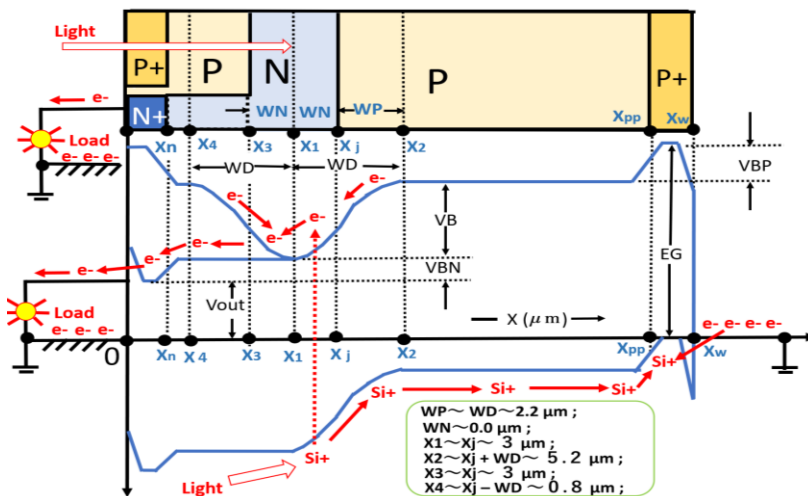
(5)  $DPN = (DP + DN) / (DP \cdot DN)$  ;

(6)  $V_B = EG - V_{out} - V_{BP} - V_{BN}$  ;

(7)  $WD = \text{sqrt}(2 \cdot E_{si} \cdot V_B / DPN)$  ;

\*\*\*\*\*

For P+PNPP+ Double Junction Solar Cell,  
Photo Electron Generation Width= $5.2 \mu m$  ;



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Output

\*\*\*\*\*

$V_{BN}=0.005422$   $V_{BP}=0.317982$

$DN=8435694.814368$   $DP=130.373502$

$V_B=0.486596$  for  $WD=2.199355$

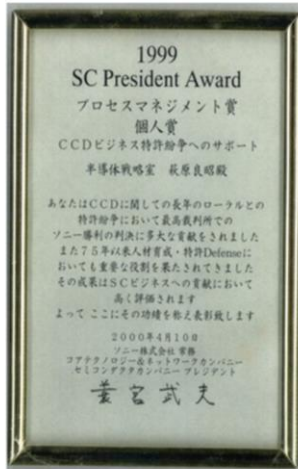
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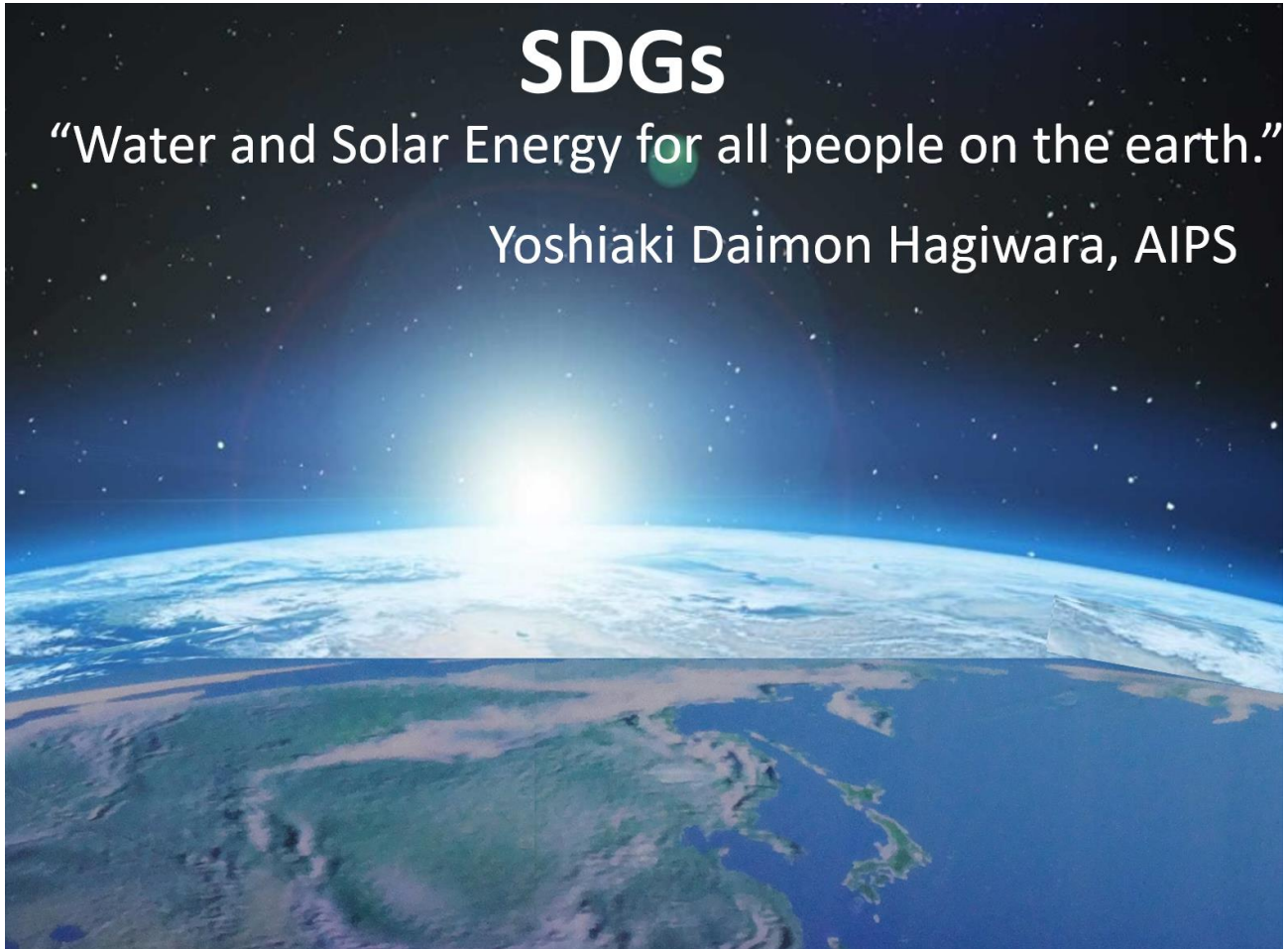
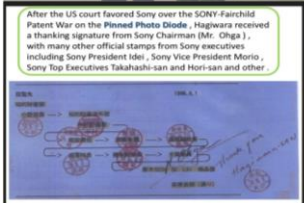
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Semiconductor Company President Award 1999



Newspaper describing Sony Victory on Sony-Fairchild Patent War July 18, 1996



# Thank you very much!