

萩原 aips 研究所が創る人工知能 (A I) 搭載のロボットは、人間にやさしい、自然にやさしい、人間を助けるパートナーとして、いろいろな目的での活躍が期待されるシステム・ロボットです。太陽光をエネルギー源とし、その超光感度の電子の目はそのままでも光電変換効率の高い太陽電池として機能します。自然にやさしい地球にやさしい、SDGs に貢献する、賢い超光感度の電子の目を持つ自己発電型・人工知能 (A I) 搭載ロボットです。

鉄腕アトムは半導体部品で構成され創られています。  
鉄腕アトムの賢い電子の目は太陽の光を吸収して  
光エネルギーを電気エネルギーに変換します。  
鉄腕アトムの賢い電子の目は太陽電池でもあります。  
賢い電子の目は半導体で造られます。

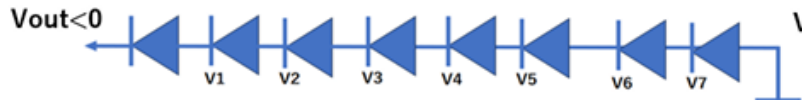
## 半導体とは？



# TANDEM型多重接合太陽電池

# Face-to-Face型多重接合太陽電池

Conventional Multi-junction Solar Cell Structure



Many Large Floating-Diffusion N+ Area ( V1, V2~V7 ) causing Serious Recombination Loss

Hagiwara Multi-junction Solar Cell Structure



Small Outlet Floating N+ Diffusion Area with Very Small Recombination Loss

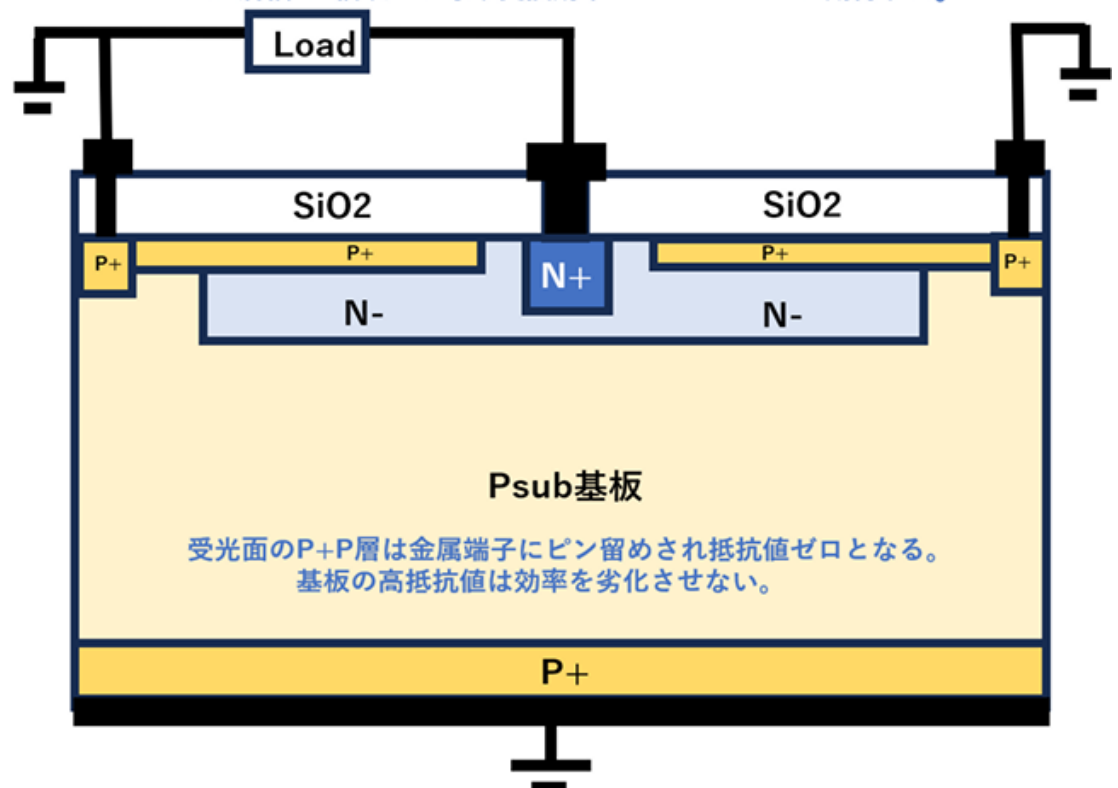
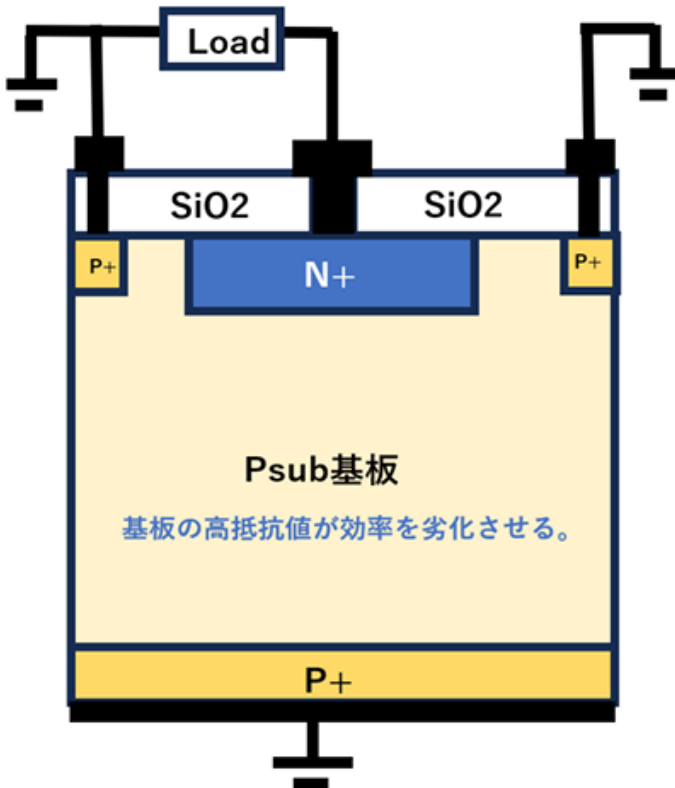
## 従来のN+Pシングル接合型太陽電池

熱拡散法のみで製造しコストに有利だが、  
変換効率は20%程度が限界である。

## 2020年8月1日出願のP+PNPP+ダブル接合型太陽電池

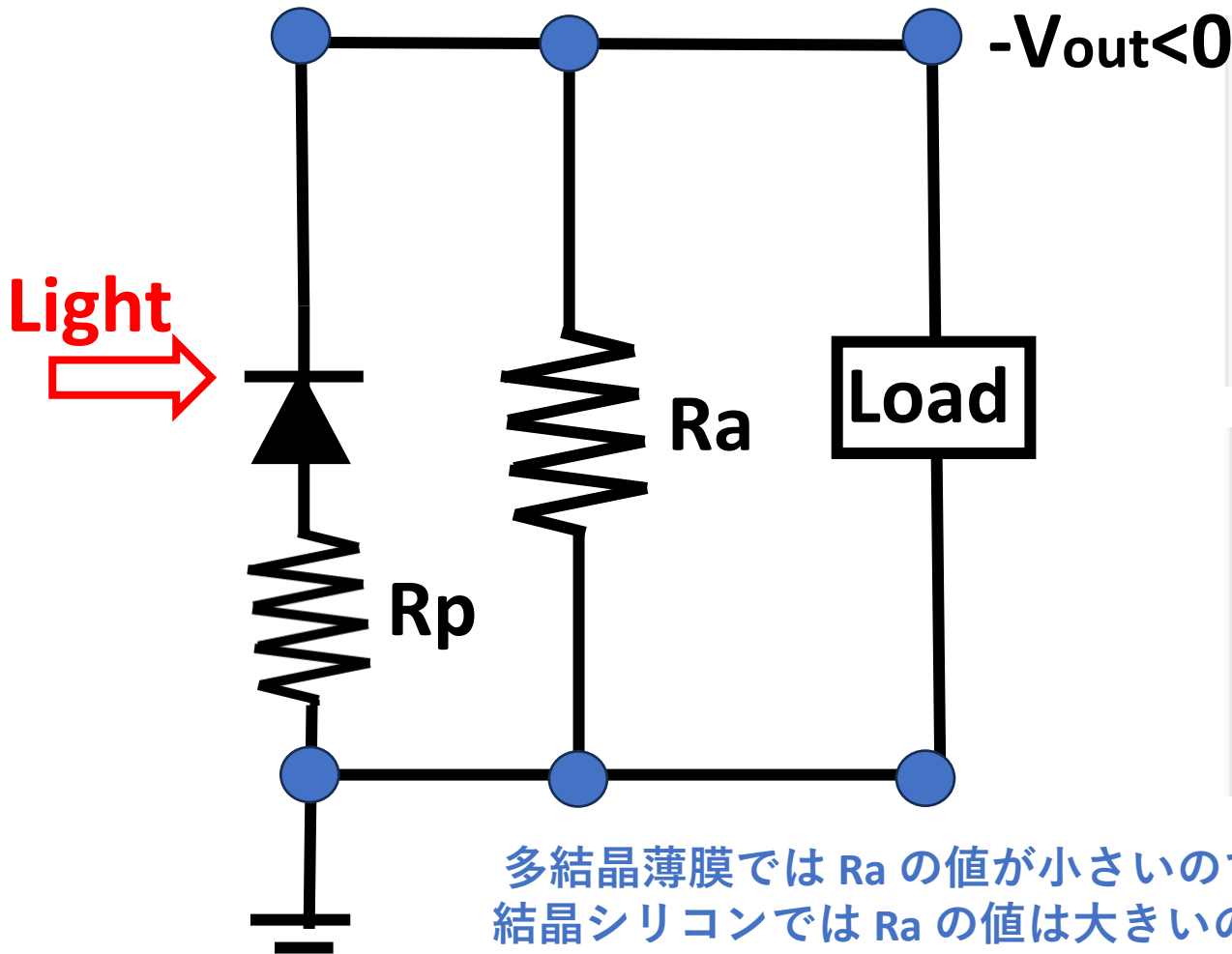
JPA2020-131313

N+埋め込み層形成の為に高エネルギーイオン打ち込み装置が不可欠。  
空乏層幅が2倍以上になり変換効率は40~60%を期待する。



多結晶シリコンでは  $\text{¥}2399/6\text{W}=\text{¥}400/\text{W}$ ;  
 薄膜 アモーフアス・シリコンでは  $\text{¥}2409/\text{W}$ ;

Intrinsic 型ペロブスカイト膜を使った P-I-N型太陽電池が有望視されている。



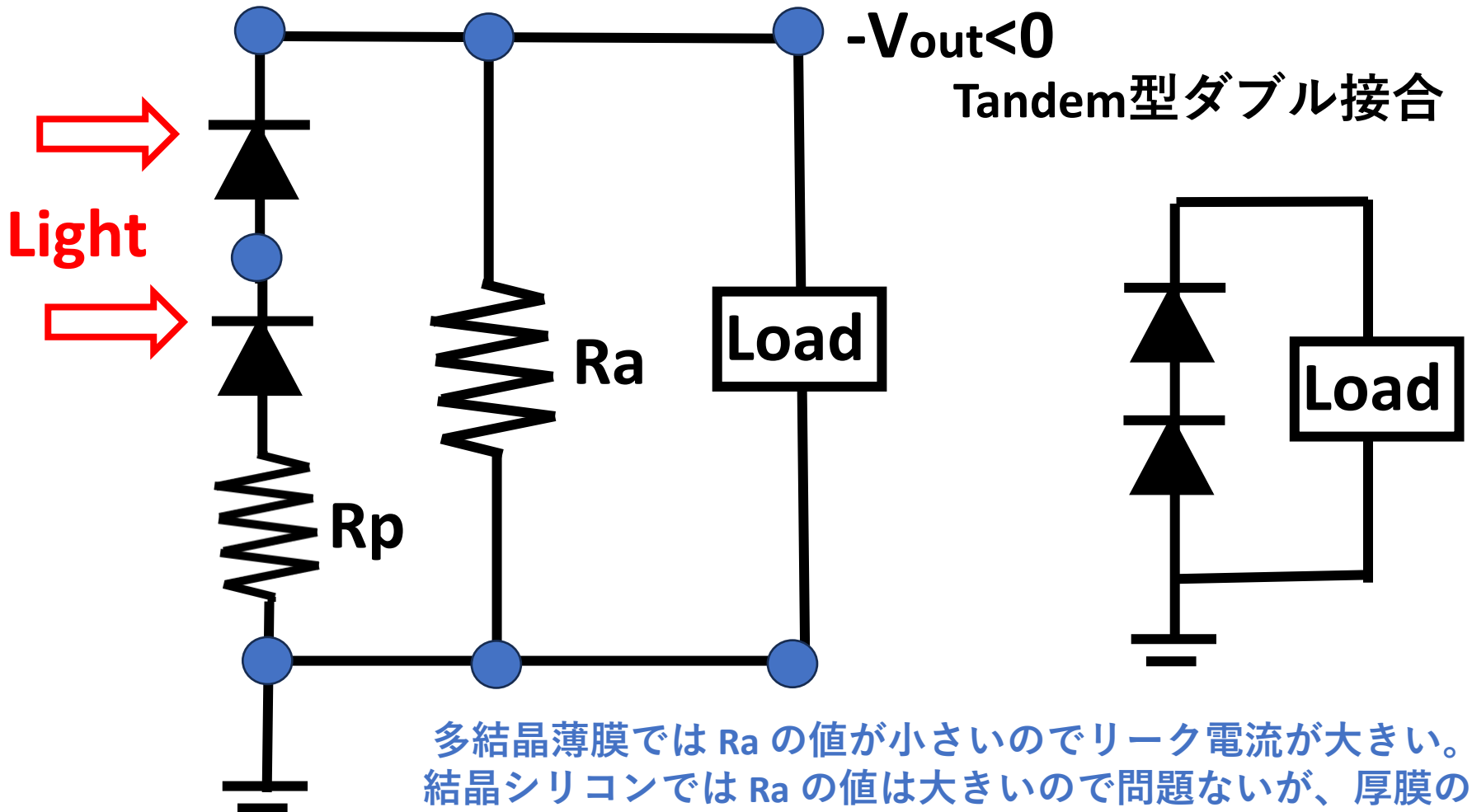
 <p>Aicosineg ミニソーラ ーパネルソーラーパ ネル 単結晶シリコン</p> <p><b>¥783</b></p>	 <p>FlexSolar ソーラーパ ネル 6W 5V 高性能単 結晶 usb超薄携帯型</p> <p><b>¥2,399</b></p>
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 <p>Galori アモルファス シリコンソーラーパネ ル,1W6Vフレキシブル</p> <p><b>¥2,690</b></p>	 <p>1W 6V フレキシブル ソーラーパネル小型薄 型アモルファスシリコ</p> <p><b>¥2,409</b></p>
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多結晶薄膜では  $R_a$  の値が小さいのでリーク電流が大きい。  
 結晶シリコンでは  $R_a$  の値は大きいので問題ないが、厚膜の  
 結晶シリコンでは基板抵抗  $R_p$  の値が大きく、電力ロスが生じる。

多結晶シリコンでは ¥2399/6W=¥400/W;  
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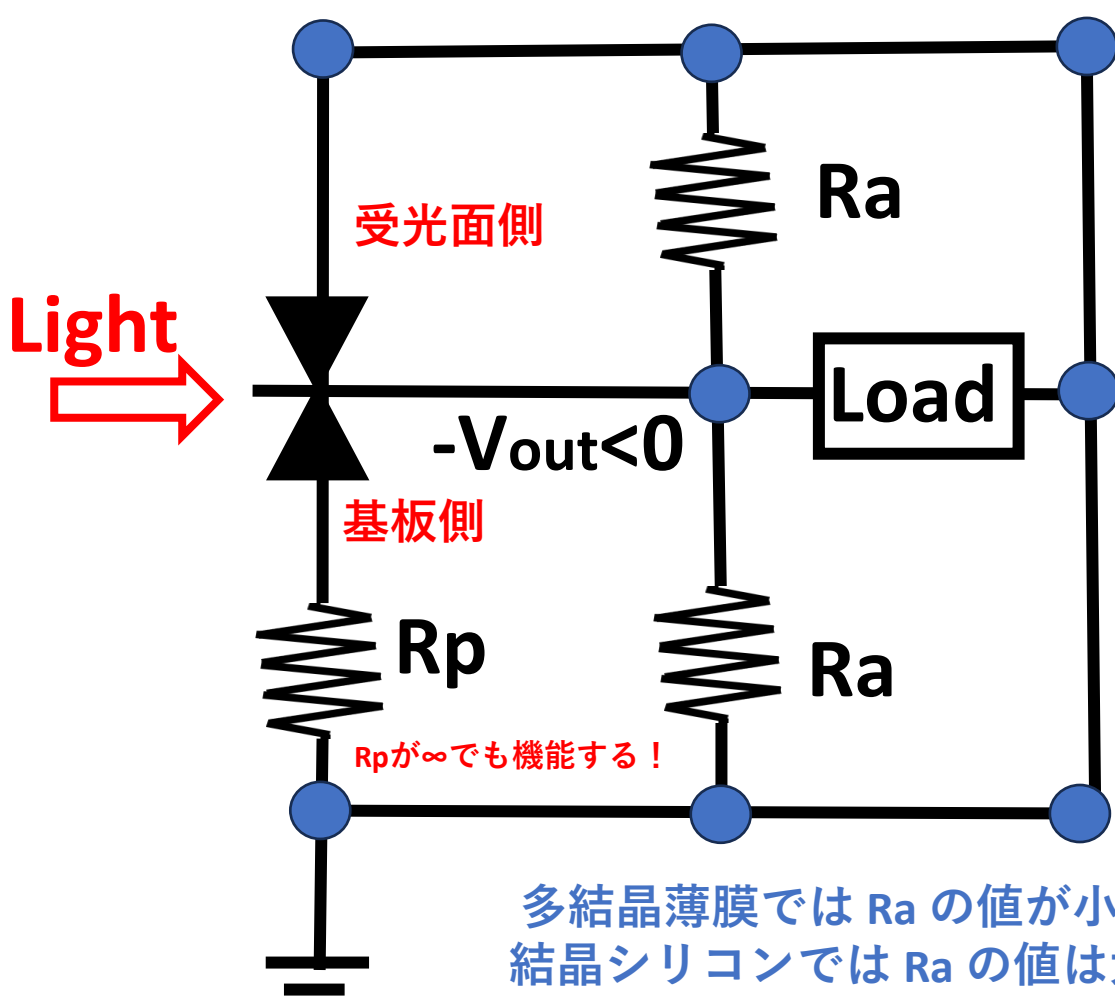


Tandem型ダブル接合

多結晶薄膜では  $R_a$  の値が小さいのでリーク電流が大きい。  
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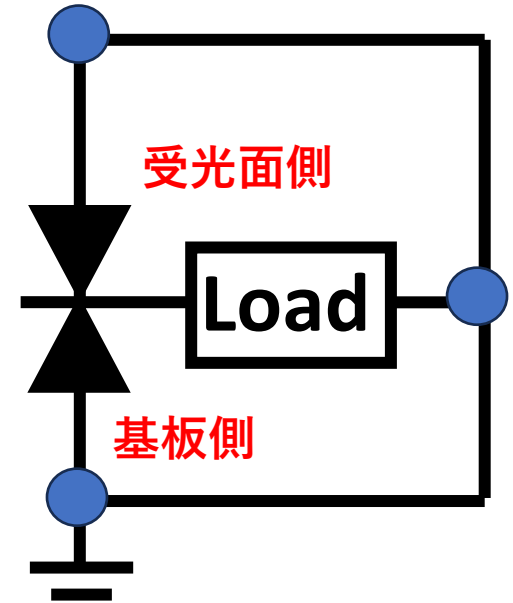
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Intrinsic 型ペロブスカイト膜を使った P-I-N型太陽電池が有望視されている。



$R_p$ が $\infty$ でも機能する!

Face-to-Face型ダブル接合



受光面で金属端子に直接接続された、もう1つDiodeがある為に、基板の  $R_p$  が大きくても問題にならない。

多結晶薄膜では  $R_a$  の値が小さいのでリーク電流が大きい。  
 結晶シリコンでは  $R_a$  の値は大きいので問題ないが、厚膜の  
 結晶シリコンでは基板抵抗  $R_p$  の値が大きく、電力ロスが生じる。



今年2025年は、私が26歳の時にPinned Photodiodeを発明して丁度50年になります。いろいろ通り道をした屈曲の人生でした。

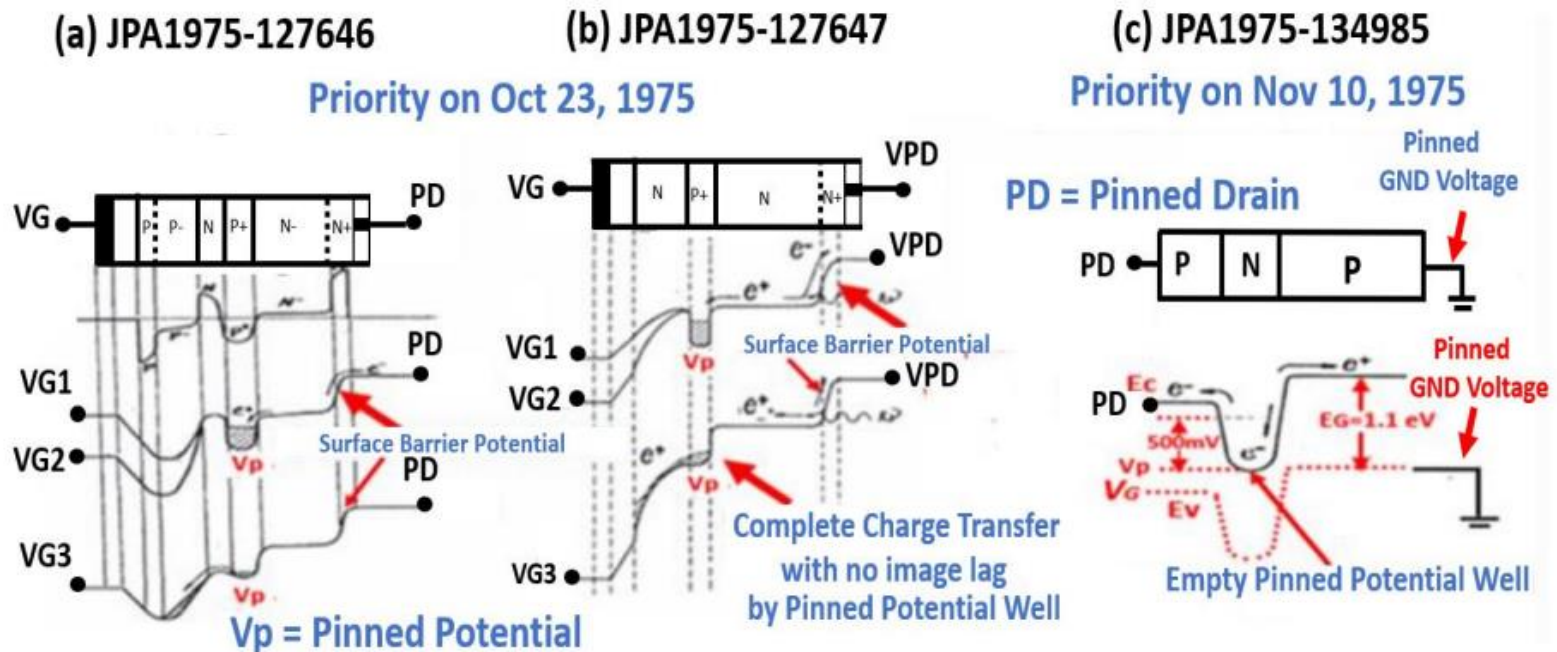


Figure 2. Pinned-surface and completely-depleted charge-collecting buried-storage photodiodes [13]

[13] Yoshiaki Daimon Hagiwara, "Chronology of silicon-based image sensor development", IEEE Electron Device Society (EDS) Newsletter pp.18-21. Jan 2023.

[https://eds.ieee.org/images/files/newsletters/Newsletter\\_Jan23.pdf](https://eds.ieee.org/images/files/newsletters/Newsletter_Jan23.pdf)

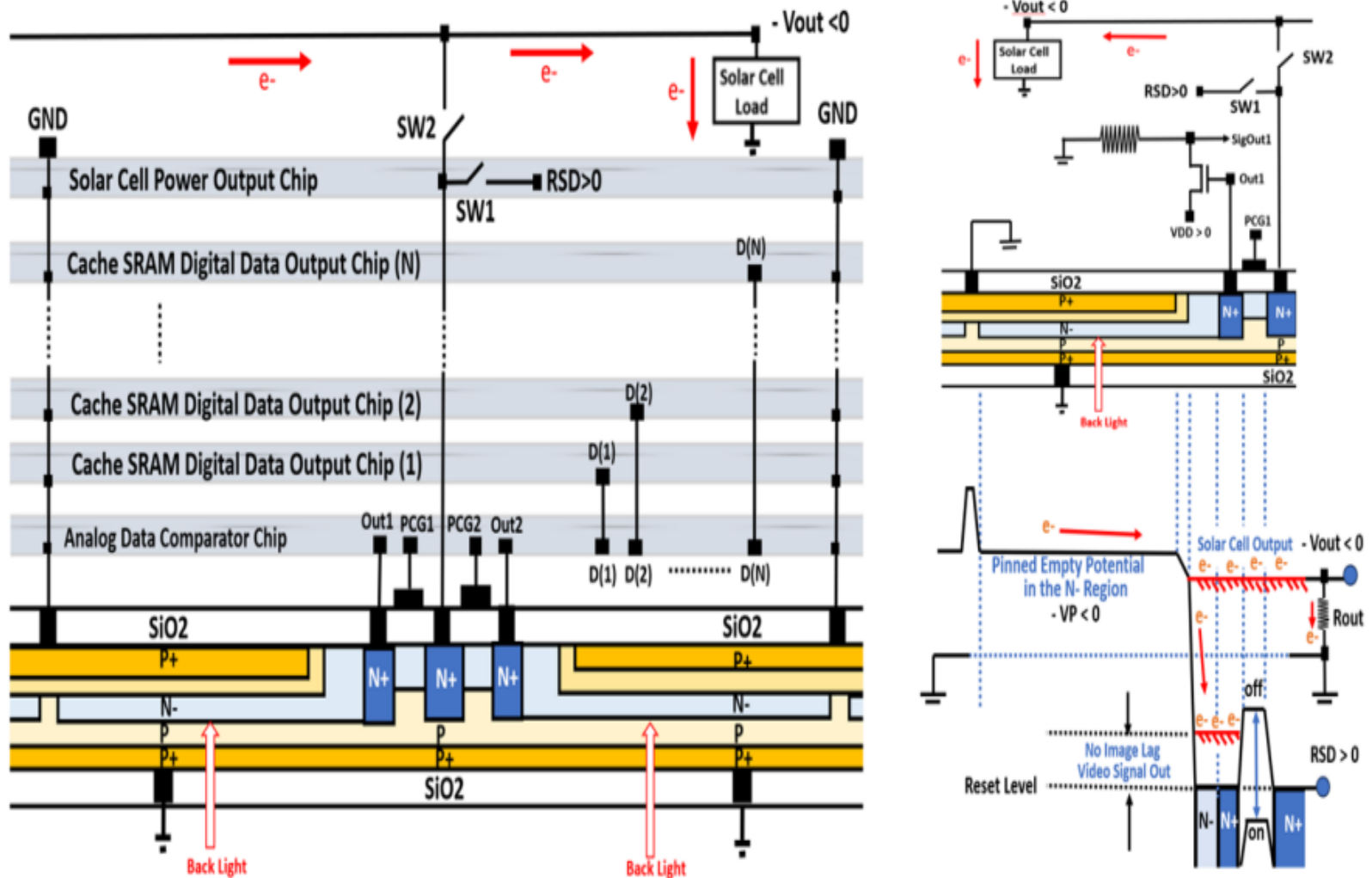
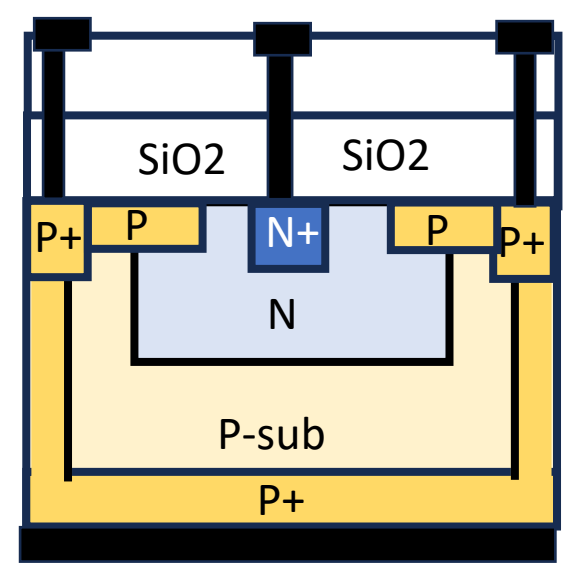
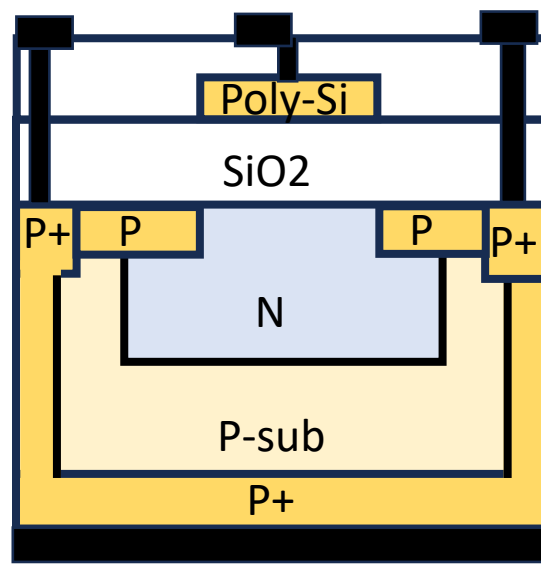
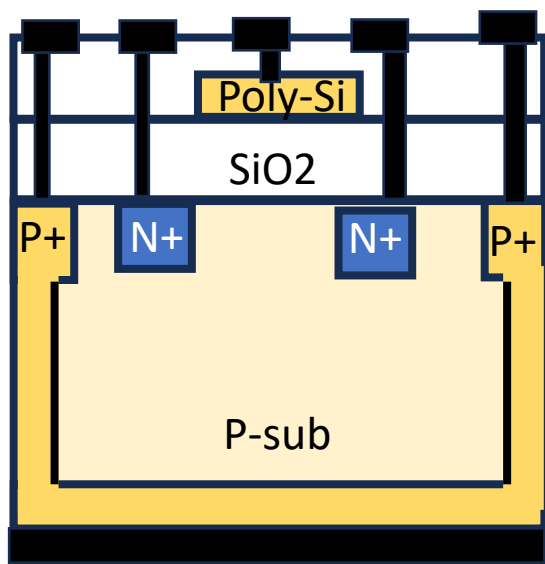


Figure 4. A cross-sectional view of our new AI Robot Vision chip in 3DIC multichip architecture



**(1) Intel 1968**  
**Bob Bower, Caltech**

**Self-Aligned Gate  
 MOS Transistor Process**

with

**High N+ Dose Low-Energy  
 Ion Implantation Technology  
 for Source/Drain Formation**

**(2) Sony 1978**

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**Pinned-Surface Virtual Gate  
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 for Buried Channel  
 N-region Formation**

**(3) AIPS 2020**

**Yoshiaki Hagiwara, AIPS**

**Pinned-Surface Virtual Gate  
 PNP Double Junction  
 Photodiode Type  
 New High QE Solar Cell**

with

**High-Dose Low-Energy  
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 for Buried Channel  
 N-region Formation**



●合同会社 locomtec.jp/萩原aips研究所 所長

<https://locomtec.jp/%E8%90%A9%E5%8E%9Faips%E7%A0%94%E7%A9%B6%E6%89%80>

# 合同会社ロコムテック

萩原*AIPS*研究所目的

この研究所は、人工知能を備えた鉄腕アトム  
のようなロボットを  
つくることを目的としている

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## 手段

目的を達成するために

萩原良昭研究所所長が所有する新素子、変換効率 80% の太陽光発電素子を製造する技術確立してその財源とする。

● 19.6%の太陽光エネルギー成分は、長波長赤外線光（波長 $\lambda > 1.1\mu\text{m}$ ）による。長波長は、シリコン結晶はガラス板のように透明となる。したがって、光は透過してしまい、光電変換にまったく寄与しない。19.6%の太陽光のエネルギー成分は、無駄になる。熱にもならない。残りの80.4%に期待をかける。しかし、水の分子にも低温の液体状態と高温の気体状態がある。

エネルギーが大きな「気体電子」と低エネルギーの「液体電子」が電子にもある。太陽電池が抽出する電子は「液体電子」である。

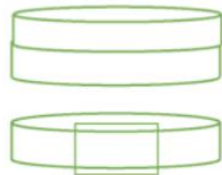
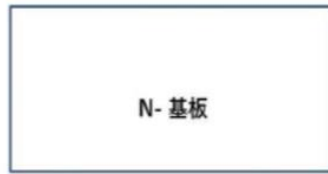
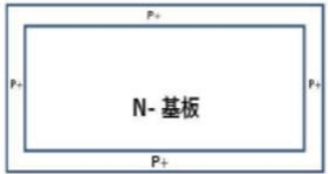
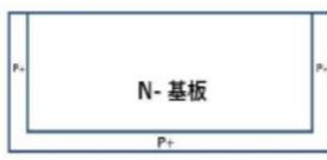
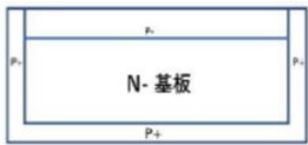
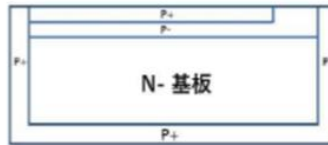
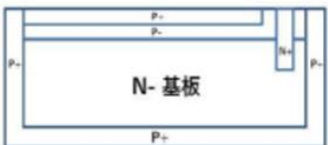


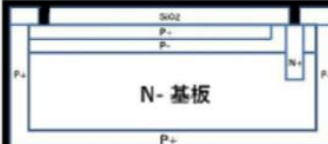

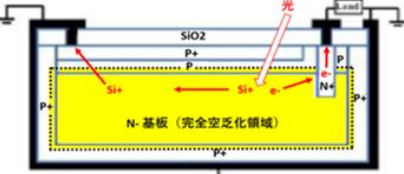
一方の、Diodeの順方向電流やTransistorのswitch-onで流れる電流は高エネルギーの「気体電体」である。

## あつぎSDGsパートナー登録申請書

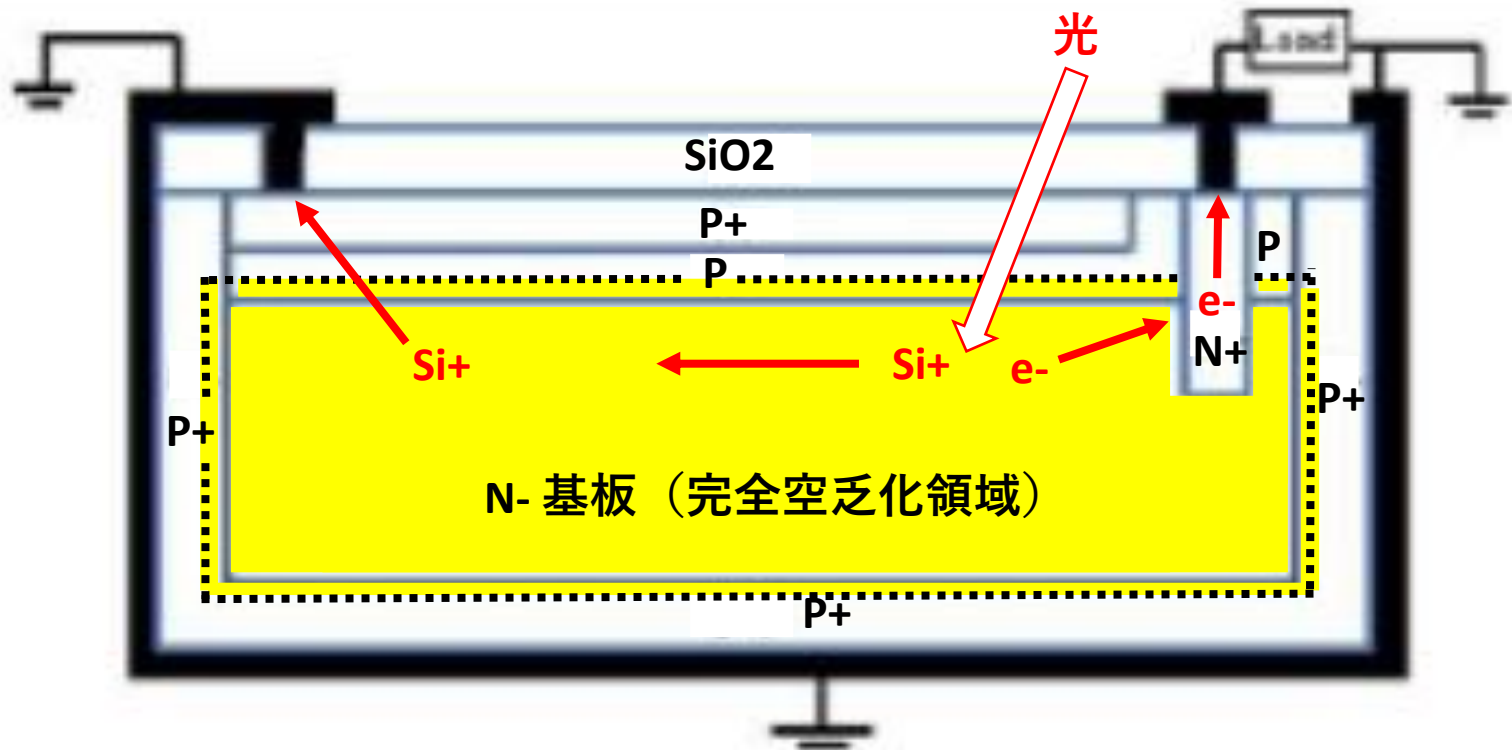
申請者概要等	
(ふりがな) 企業・団体名等	ごうどうがいしゃろこむてつく はぎわらえーあいぴーえすけんきゅうじよ 合同会社ロコムテック 萩原 AIPS 研究所
区分	企業(業種:研究・試作・製造)、団体、大学、NPO、その他( )
企業・団体等の 事業概要	この研究所は、人工知能を備えた鉄腕アトムのようなロボットを作ることを目的としているが、目的を達成するために萩原良昭研究所長が特許を所有する新素子、変換効率80%の太陽光発電素子を製造する技術を確立してその財源にする。
代表者役職	代表社員
(ふりがな) 代表者氏名	いわさき まさあき 岩崎 正昭
所在地	神奈川県厚木市みはる野2-3-8
担当者氏名	岩崎 正昭
電話番号	090-7630-9582
メールアドレス	mk@locomtec.jp

SDGsの取り組み																																					
SDGs関連事業の概要	再生可能エネルギーの新素子(特許 6818208 号)の研究、試作、製造技術を確立して、安価で無尽蔵な太陽光エネルギーを永続して供給できる仕組みを構築する。 その財源を用いて、ロボットを大量、安価に供給して、教育や生活に潤いをもたらす。																																				
SDGs達成のための 目標①	目 標	炭素系エネルギー生成を削減する。																																			
	概 要	2025 年度に新素子(特許 6818208 号)の製造試作機完成。 高エネルギーイオン打ち込み装置を入手 2026 年度に試作機の変換効率30%を目標に改良を行う。 2027 年度に変換効率 50%の量産試作機を考案。 2028 年度に量産機を完成し量産開始する。																																			
	関連する ゴール	<table border="1"> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> <td><input checked="" type="checkbox"/></td> <td><input checked="" type="checkbox"/></td> <td><input checked="" type="checkbox"/></td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td><input type="checkbox"/></td> <td><input checked="" type="checkbox"/></td> <td><input checked="" type="checkbox"/></td> <td><input checked="" type="checkbox"/></td> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> <td><input checked="" type="checkbox"/></td> <td><input type="checkbox"/></td> </tr> </table>										<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>										<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
																																					
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## 新素子製造方法

 <p>0. N 型 Silicon 基板</p>	 <p>1. 非常に結晶性の良い高抵抗の N-基板を使う</p>	 <p>2. 熱拡散で回りに P+ 領域を形成し。N-層を完全な埋め込み層にする。</p>	 <p>3. 表面を Koh 液で部分エッチングを行う</p>
 <p>4. 表面に P- 領域を全面形成する</p>	 <p>5. 表面に P+ 領域を部分形成する</p>	 <p>6. 表面に N+ 領域を部分形成する</p>	 <p>7. 表面に酸化膜を形成する</p>
 <p>8. 表面の酸化膜に金属コンタクト用の窓開けを形成する</p>	 <p>9. 全面を金属膜でカバーする</p>	 <p>10. GND 金属端子と出力金属端子に分離する</p>	 <p>11. 完成図</p> <p><math>(Si) + (光) \rightarrow (Si+) + (e-)</math></p> <p><small>N-基板の厚さと濃度を薄く調整して、完全空乏化領域 (PN 接合の境界領域) が広がり、有効光電変換領域も広がり、効率向上する。</small></p>

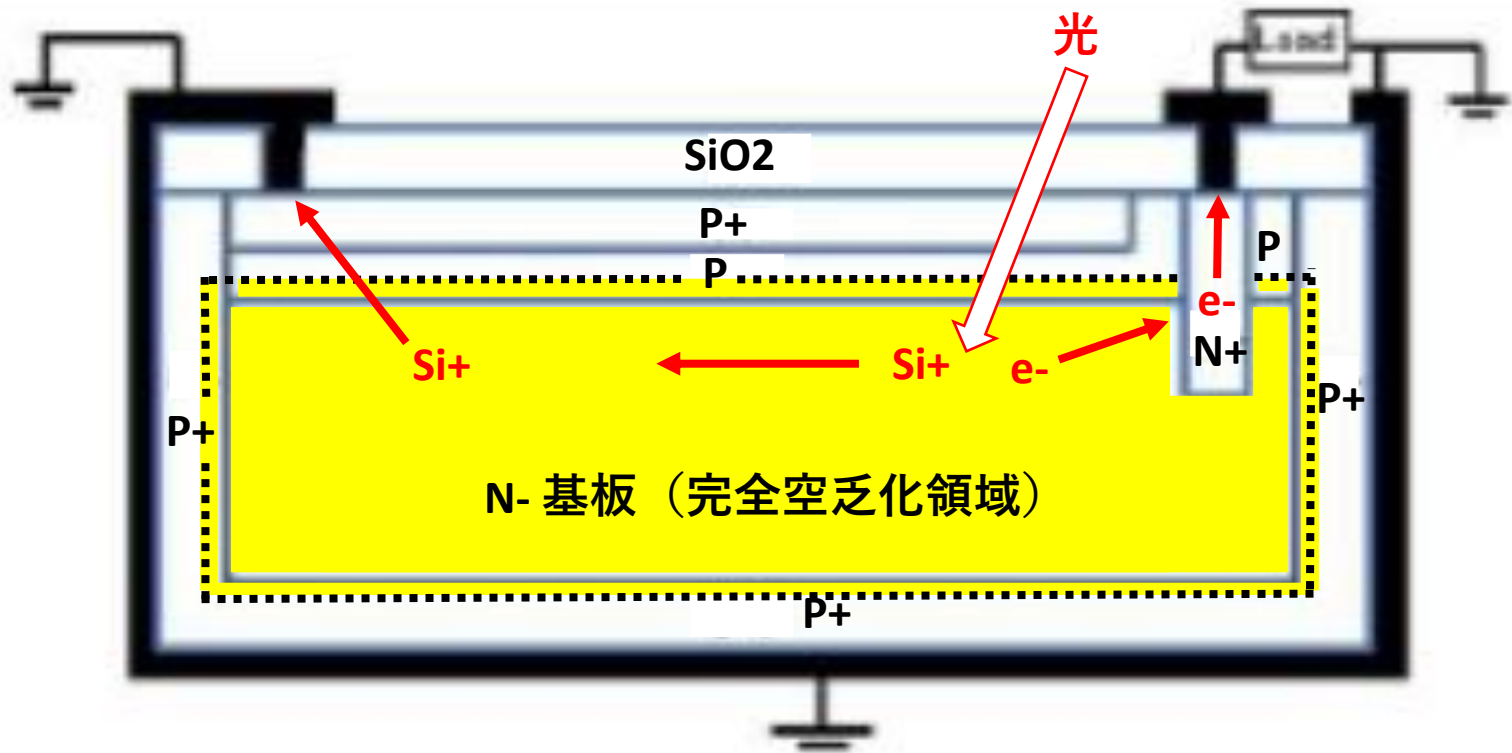




# 1 1. 完成図

N-基板の厚さと濃度を薄く調整して、完全空乏化領域（PN接合の境界領域）が広がり、有効光電変換領域も広がり、効率が向上する。





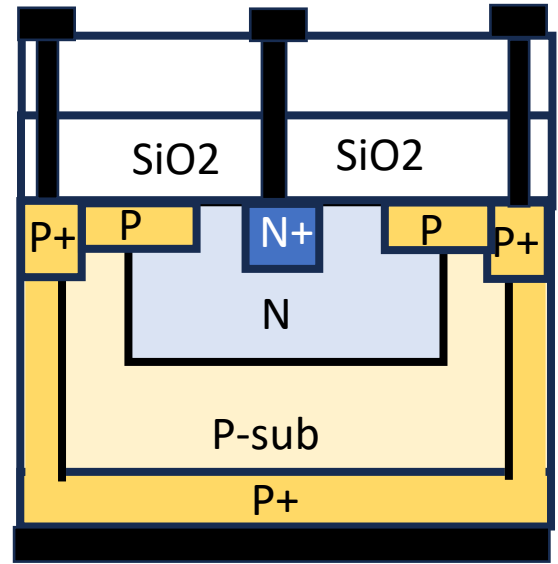
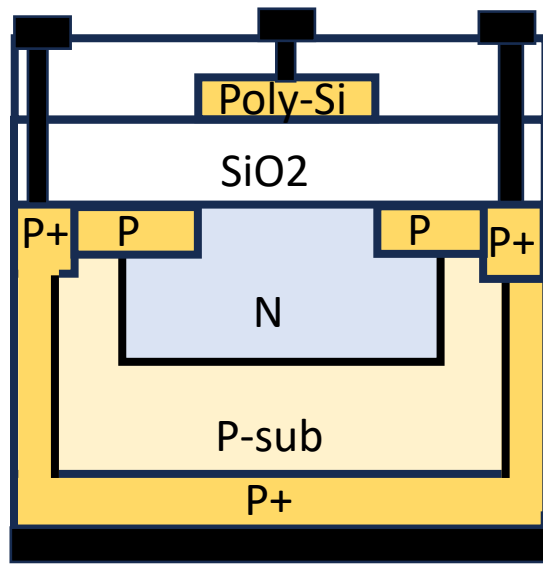
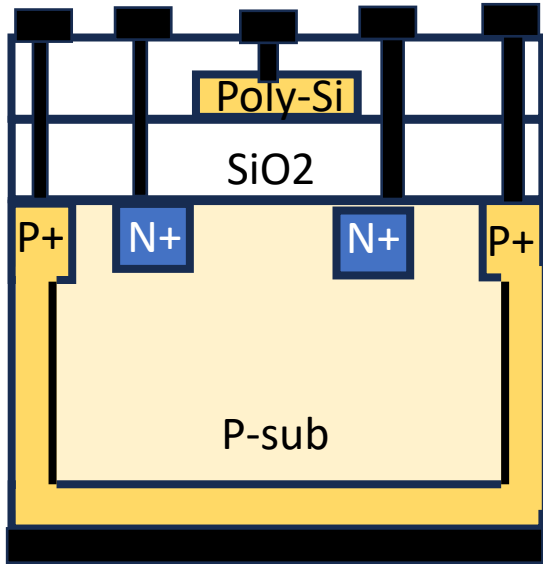
## 1 1. 完成図

N-基板の濃度と厚さを薄くすると  
完全空乏化領域とする事が可能



### 完全空乏化とは？

<https://detail-infomation.com/diode-depletion-layer/>



**(1) Intel 1968**  
**Bob Bower, Caltech**

**Self-Aligned Gate  
 MOS Transistor Process**

**with**

**High N+ Dose Low-Energy  
 Ion Implantation Technology  
 for Source/Drain Formation**

**(2) Sony 1978**

**Yoshiaki Hagiwara, Caltech/Sony**

**Pinned-Surface Virtual Gate  
 PNP Double Junction  
 Photodiode Type**

**Buried Channel CCD Imager**

**with**

**High-Dose Low-Energy  
 Ion Implantation Technology  
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 and Low-Dope High-Energy  
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 N-region Formation**

**(3) AIPS 2020**

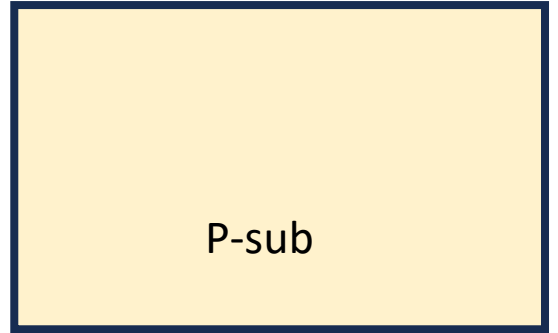
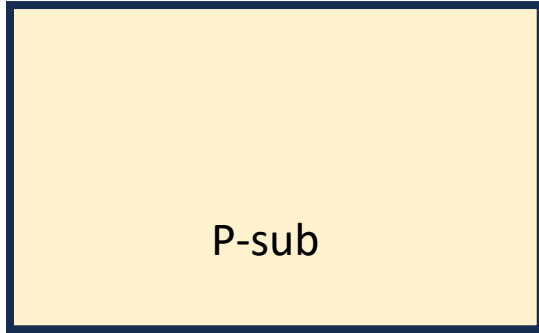
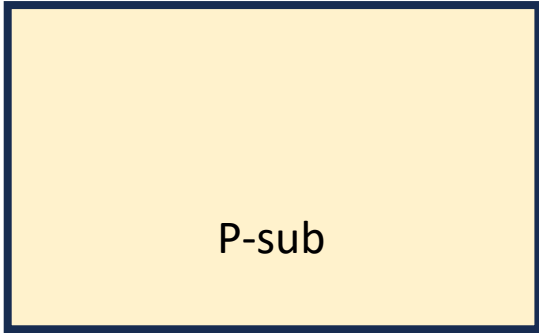
**Yoshiaki Hagiwara, AIPS**

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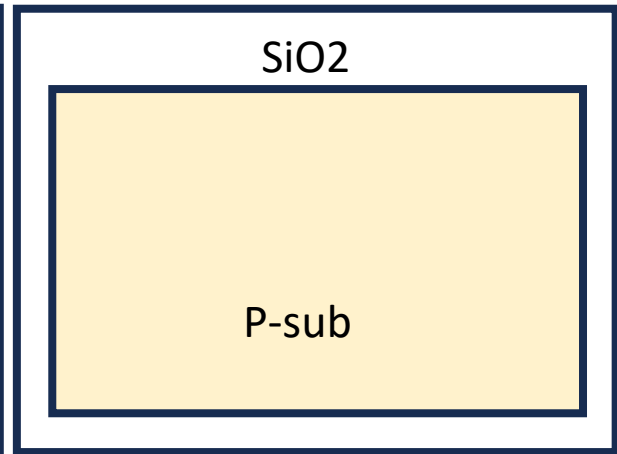
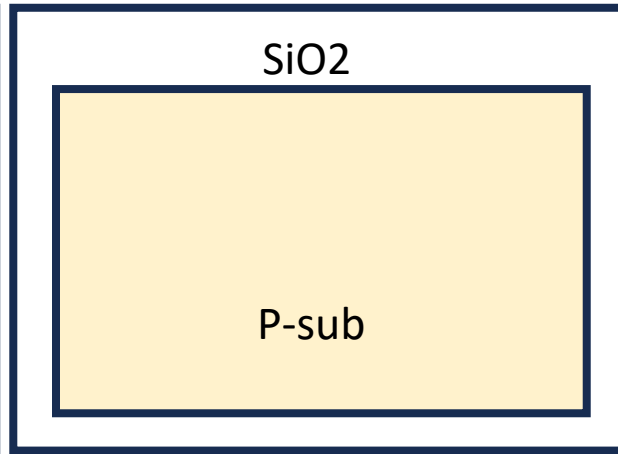
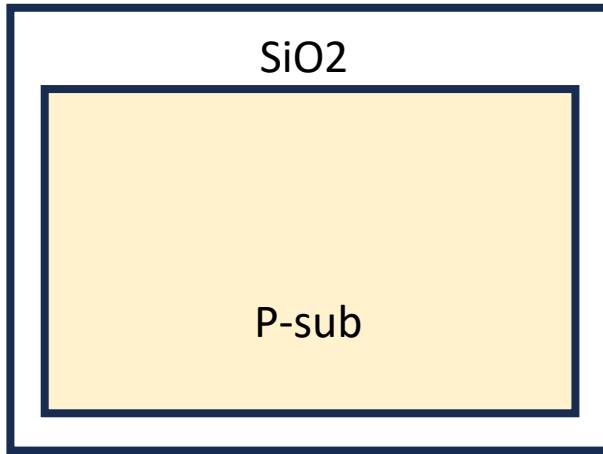
**(3) AIPS 2020**

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**Pinned-Surface Virtual Gate  
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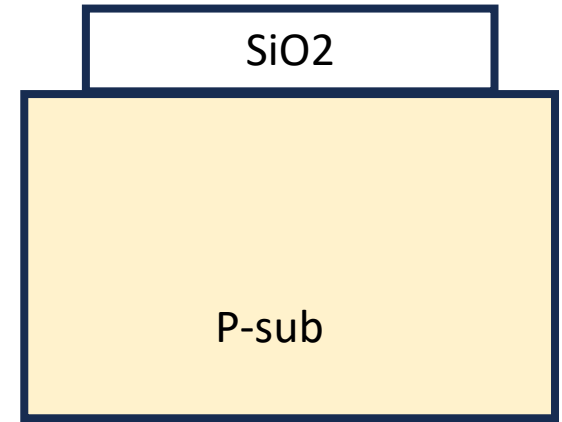
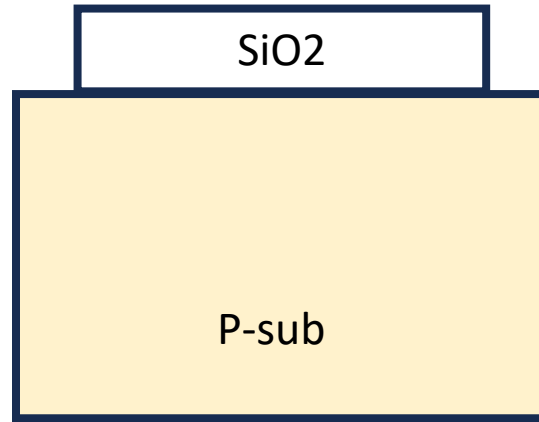
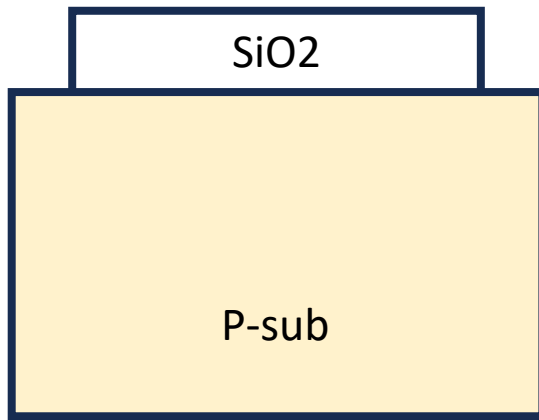
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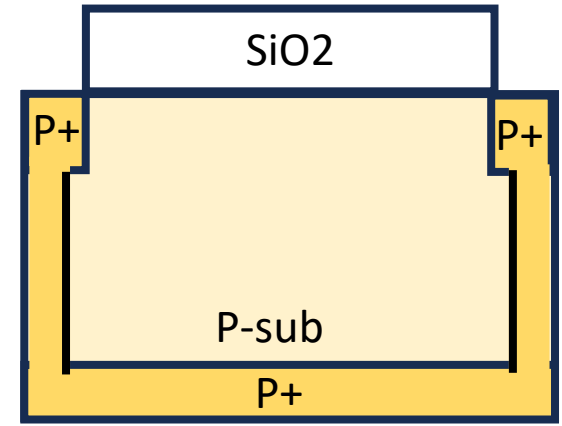
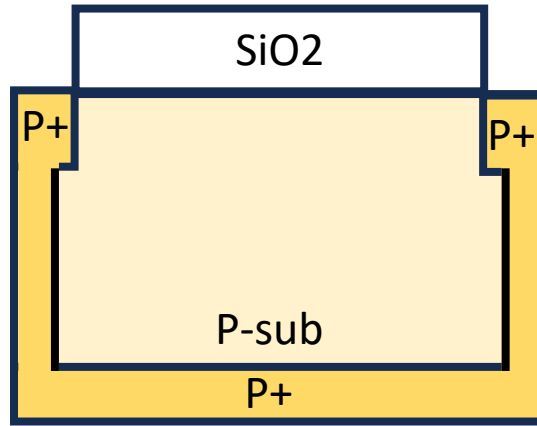
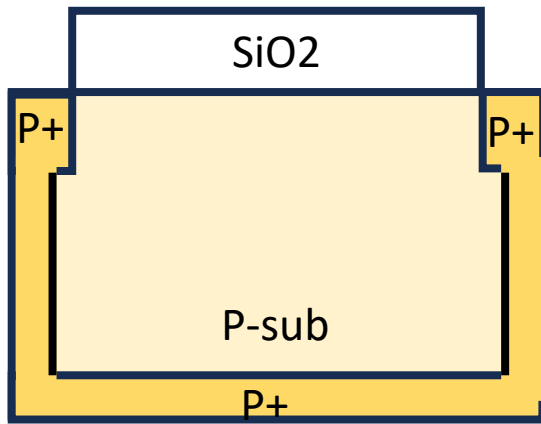
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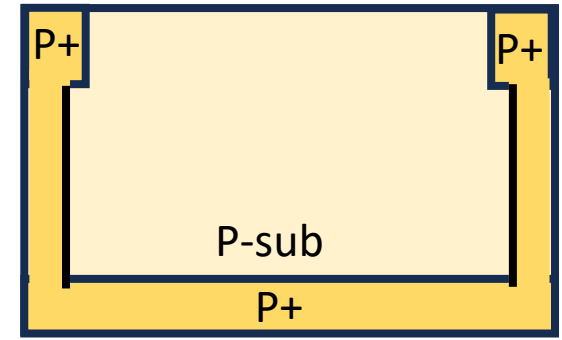
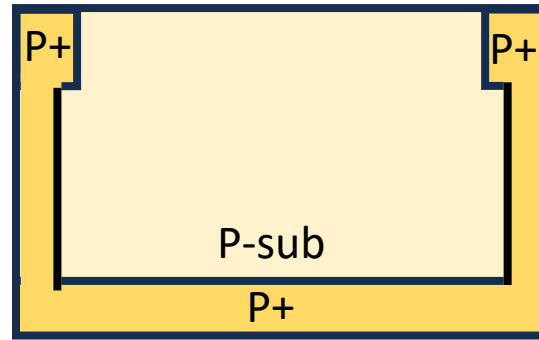
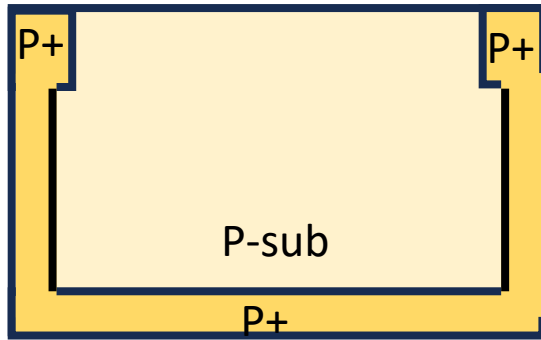
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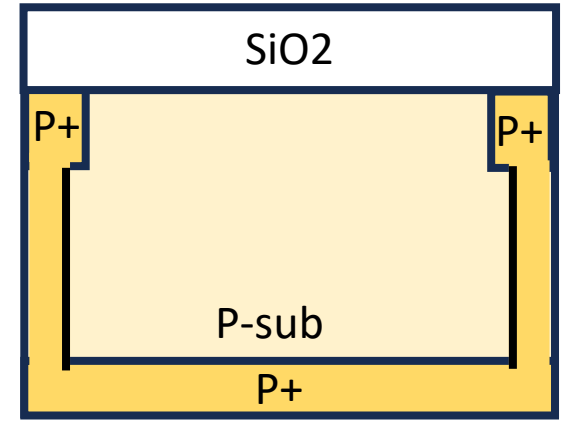
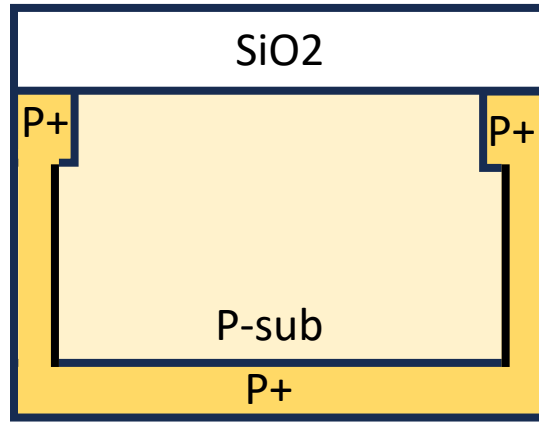
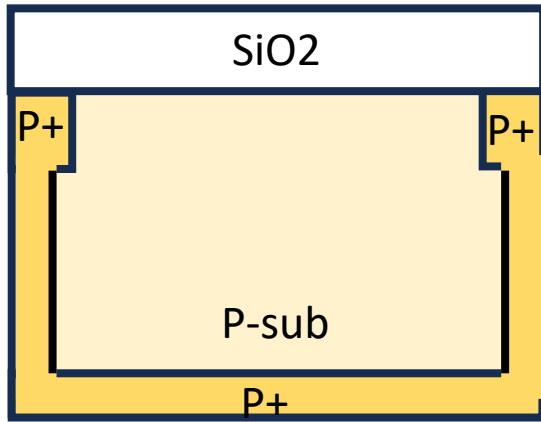
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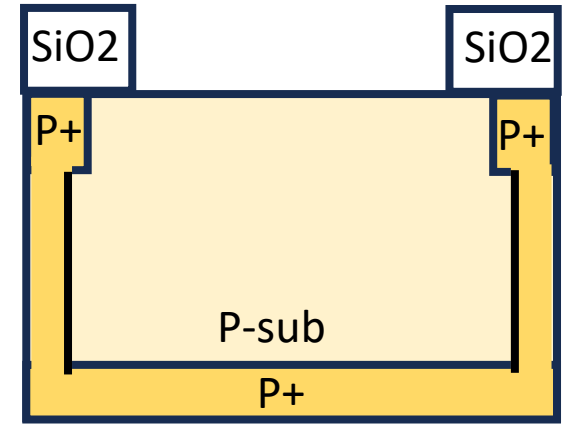
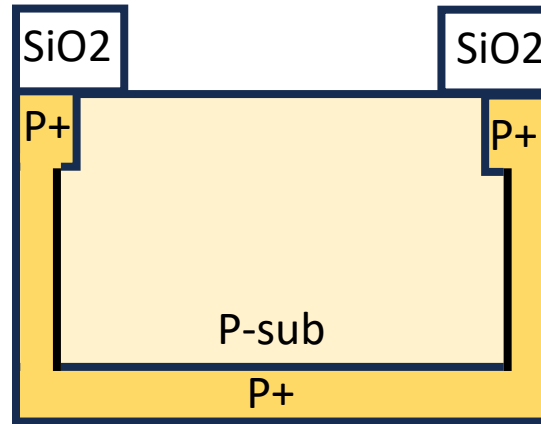
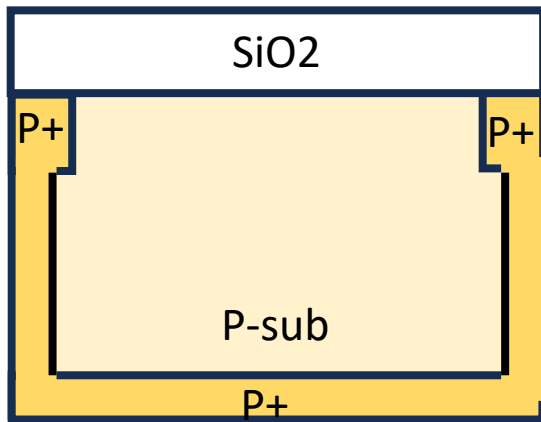
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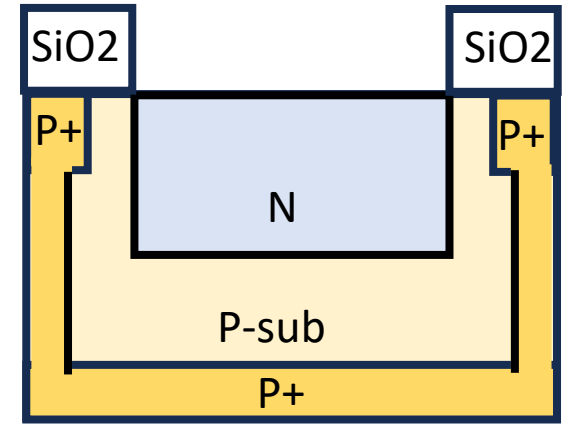
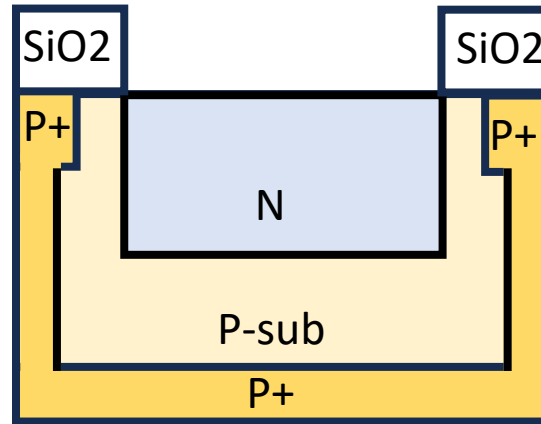
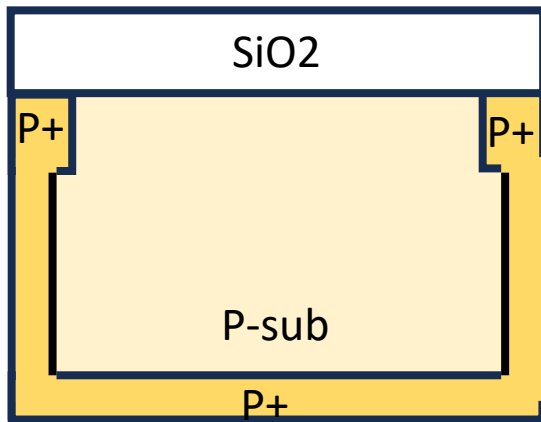
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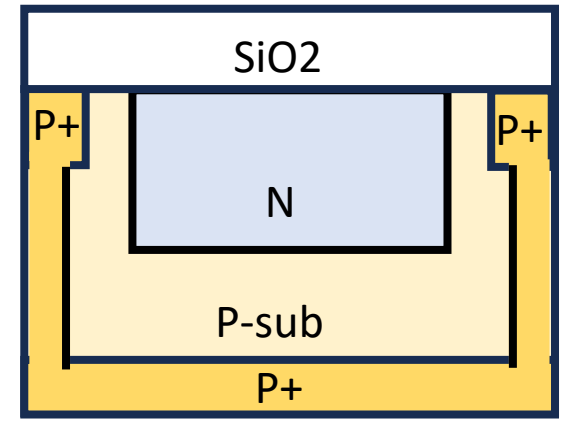
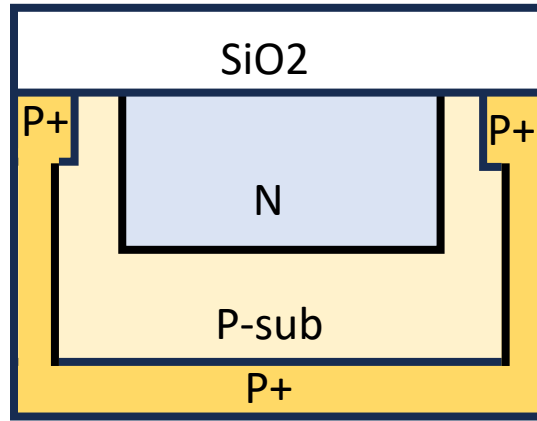
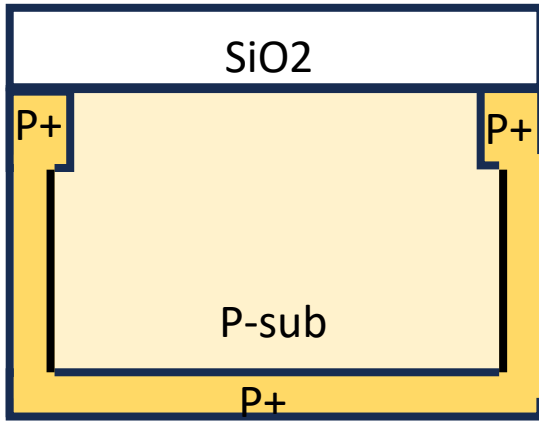
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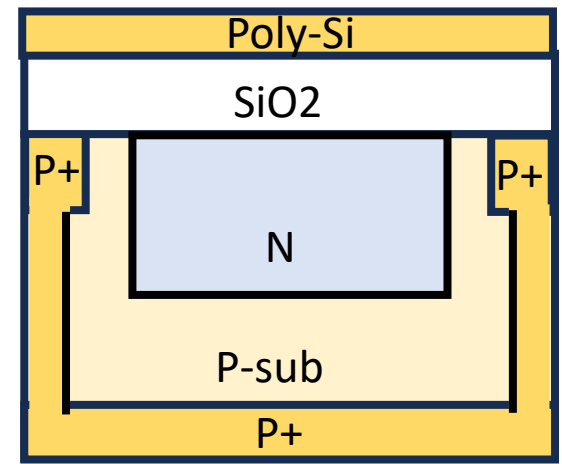
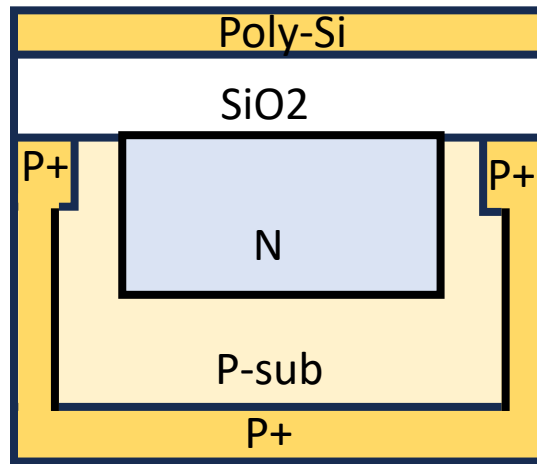
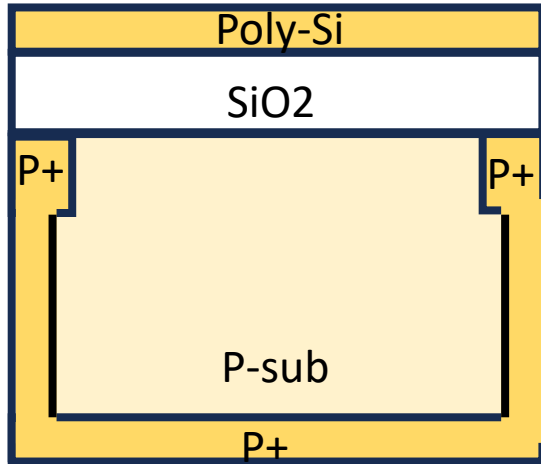
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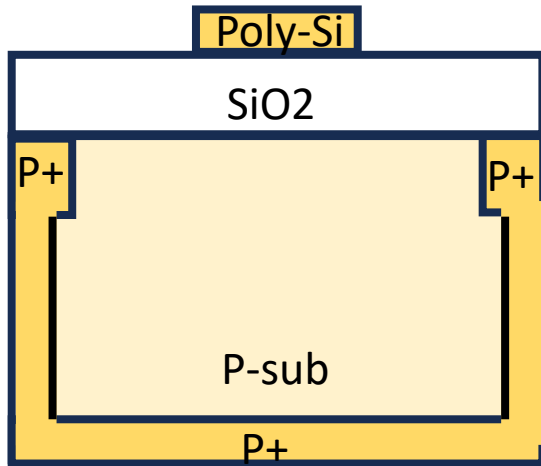
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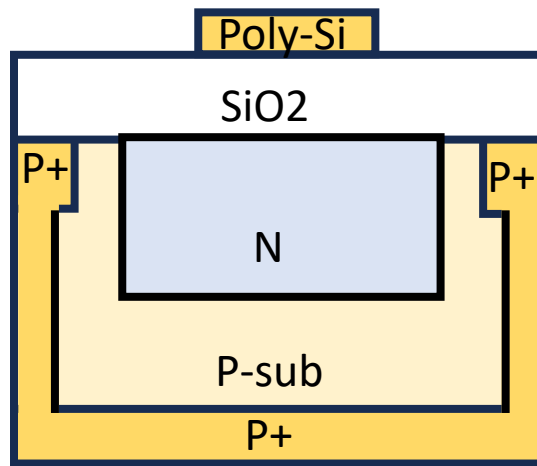
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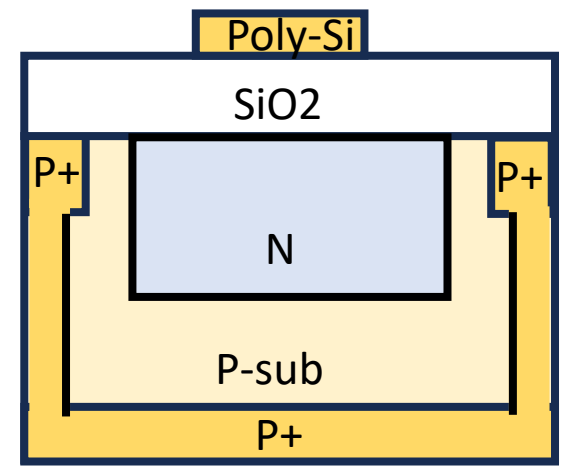
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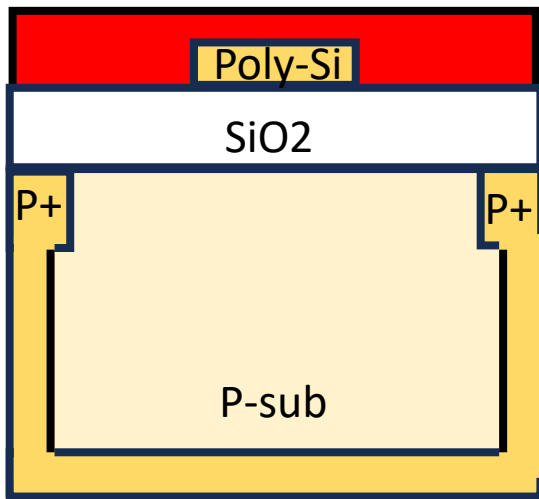
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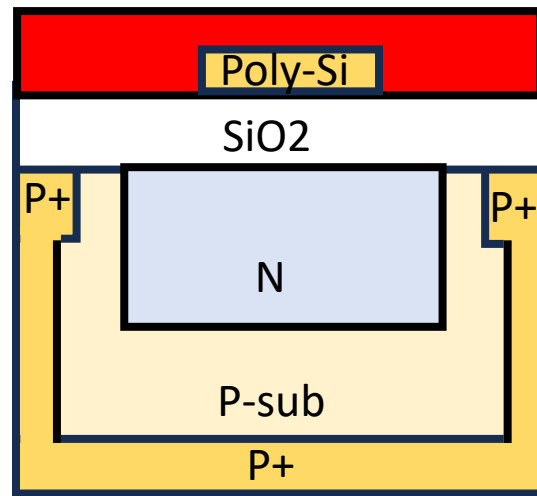
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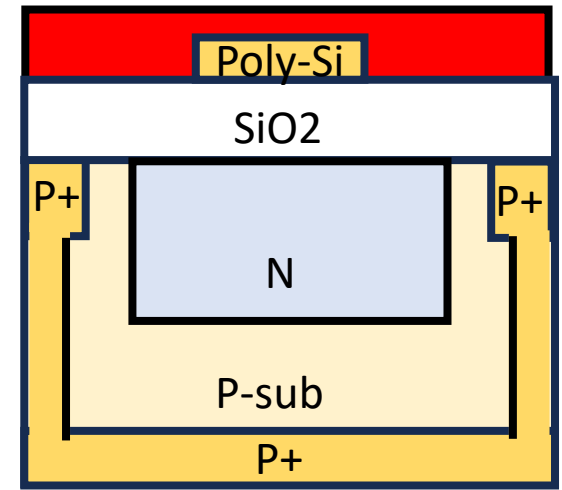
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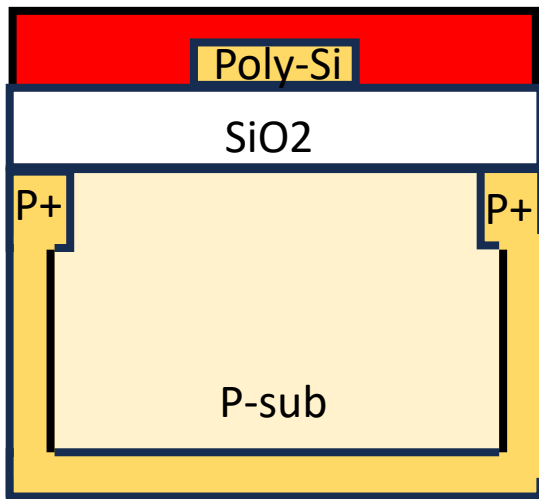


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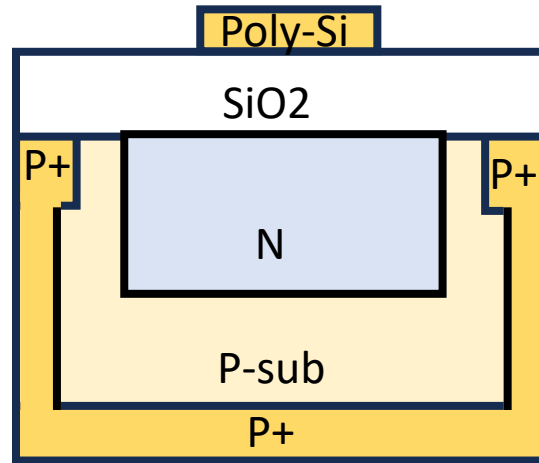




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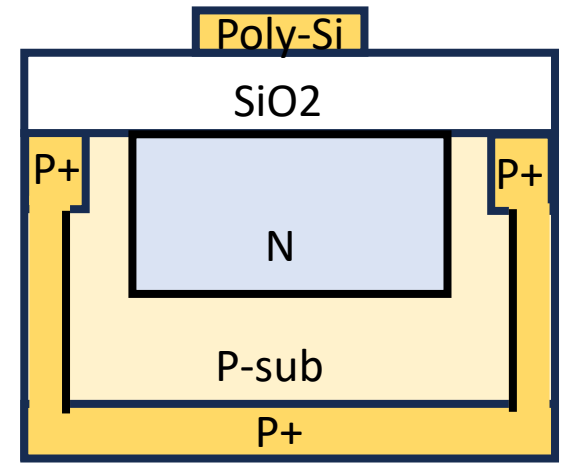
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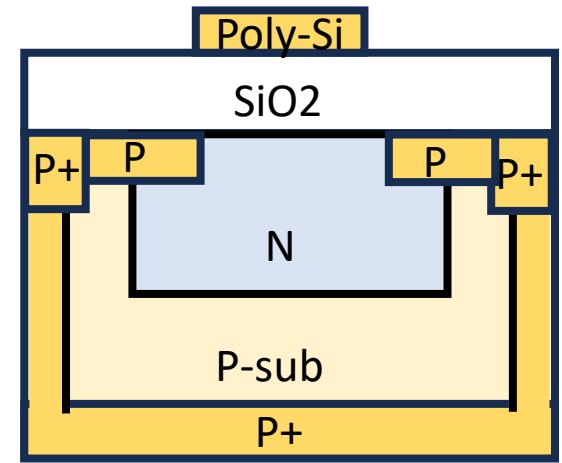
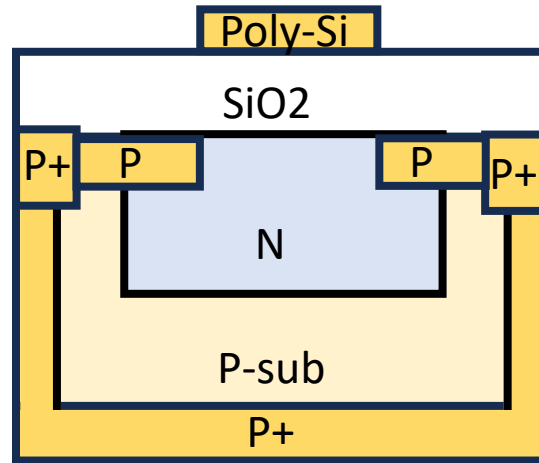
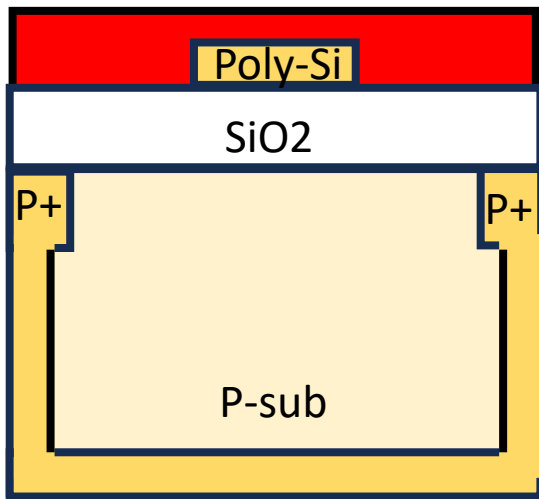
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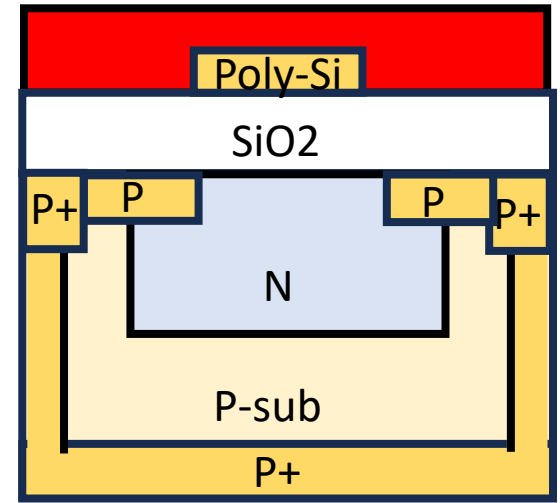
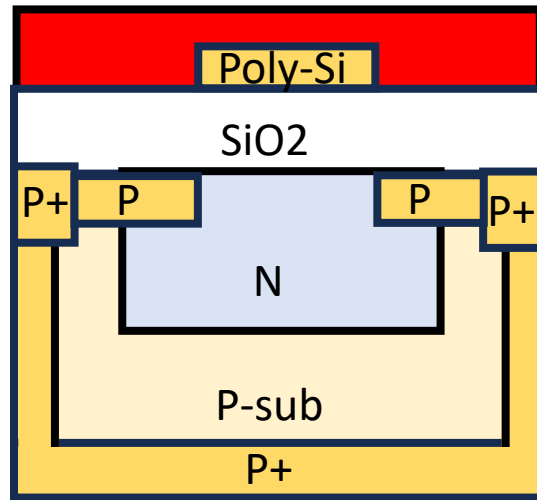
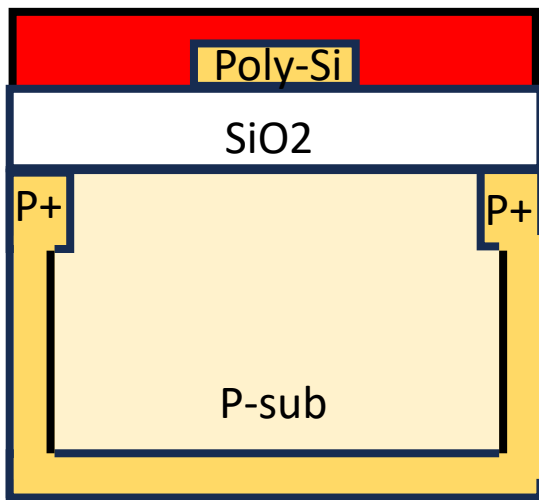
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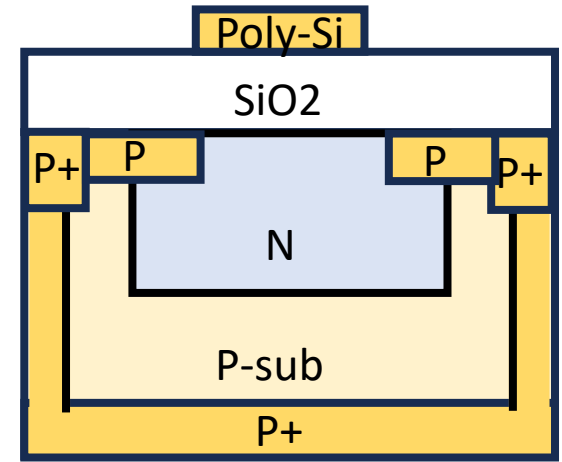
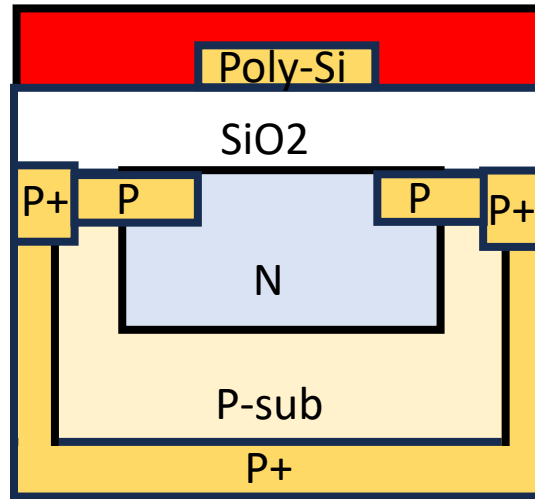
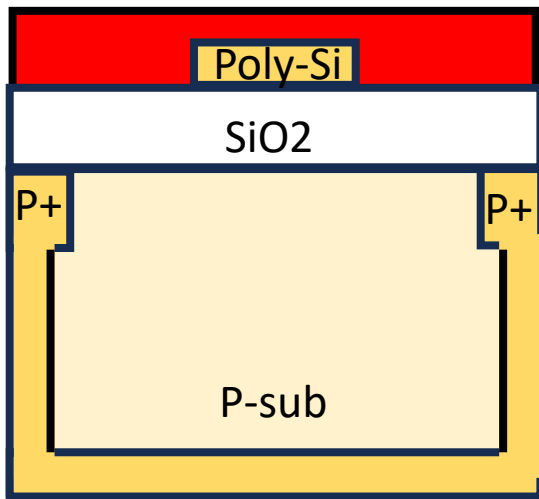
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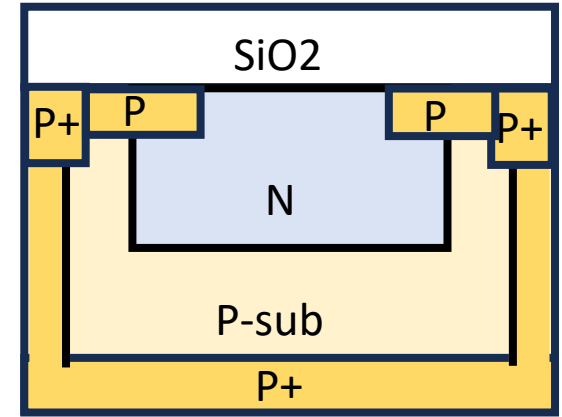
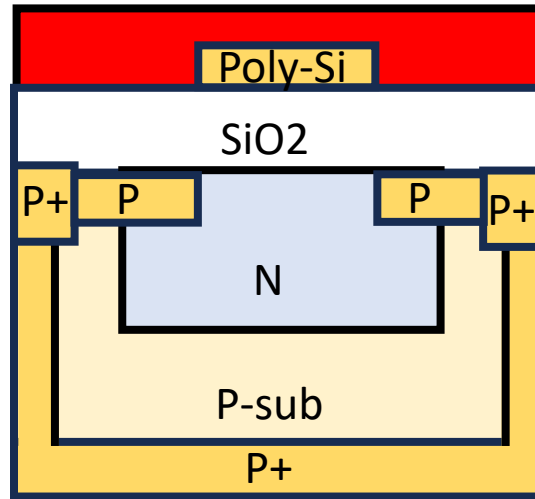
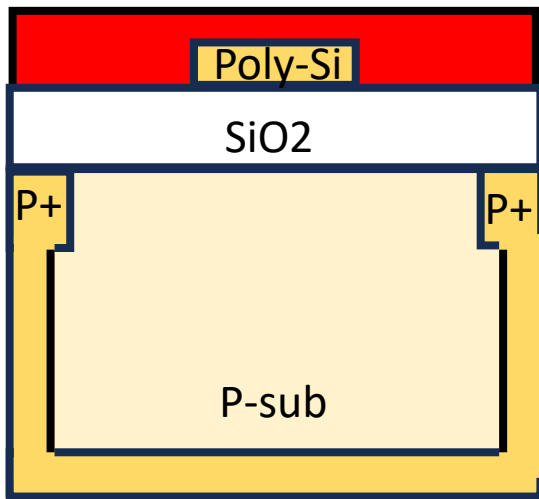
Yoshiaki Hagiwara, AIPS

Pinned-Surface Virtual Gate  
PNP Double Junction  
Photodiode Type

New High QE Solar Cell  
with

High-Dose Low-Energy  
Ion Implantation Technology  
for Surface P-region Formation  
and Low-Dope High-Energy  
Ion Implantation Technology  
for Buried Channel  
N-region Formation

**MASK 05**



**(1) Intel 1968**  
**Bob Bower, Caltech**

**Self-Aligned Gate  
 MOS Transistor Process**

with

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**(2) Sony 1978**

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**(3) AIPS 2020**

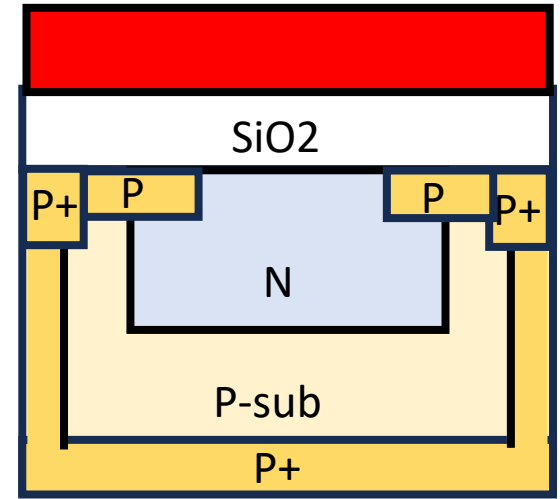
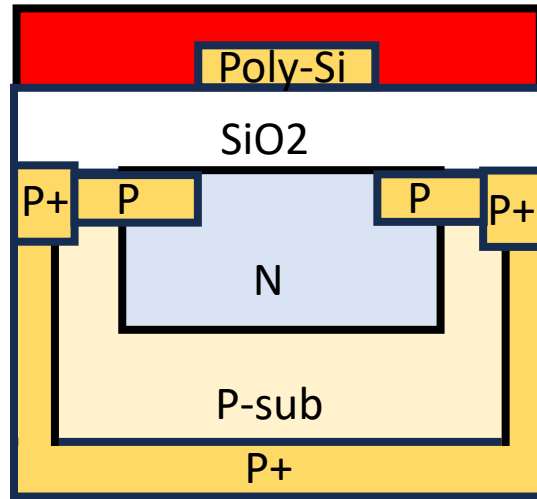
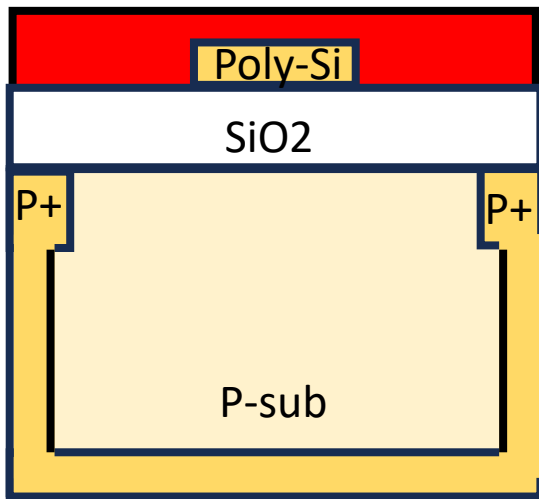
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**(3) AIPS 2020**

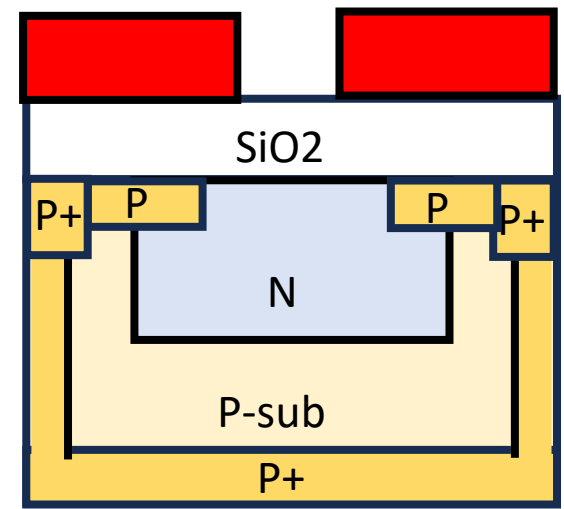
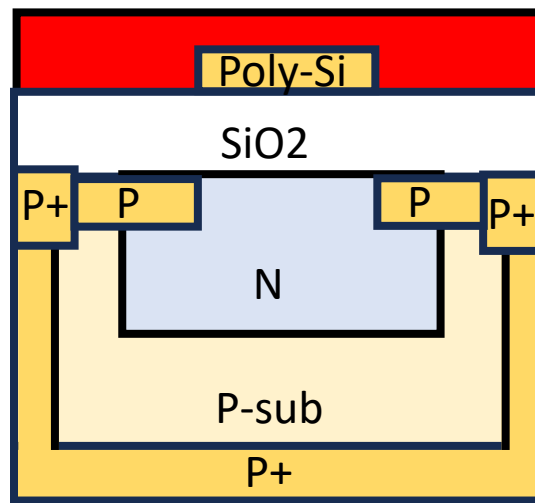
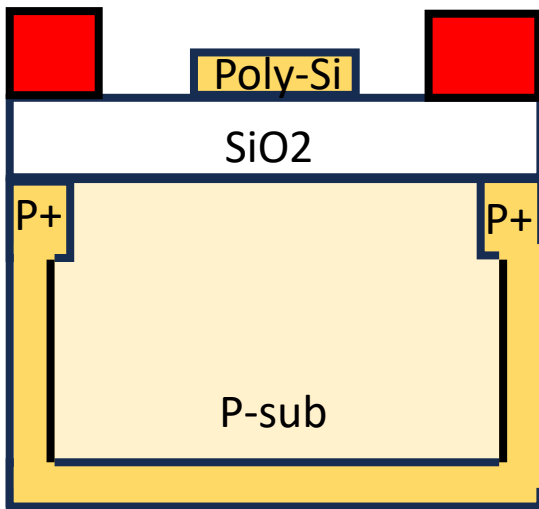
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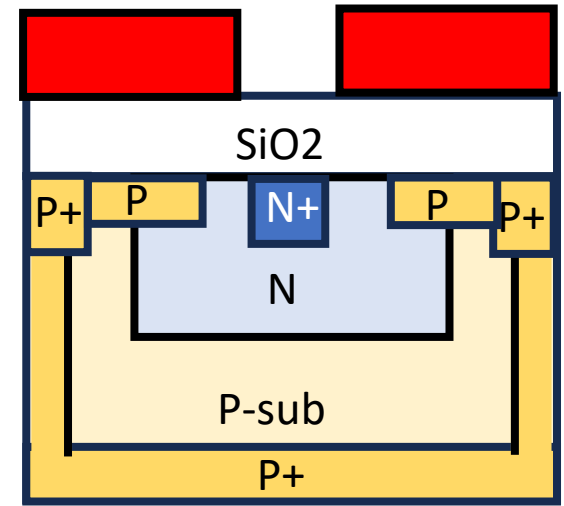
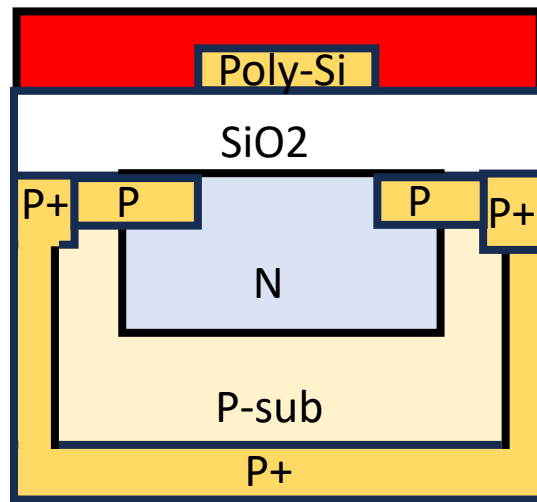
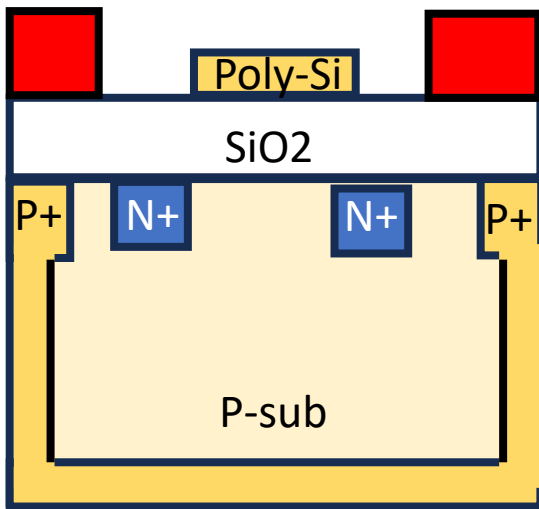
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**MASK 06**





(1) Intel 1968  
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(3) AIPS 2020

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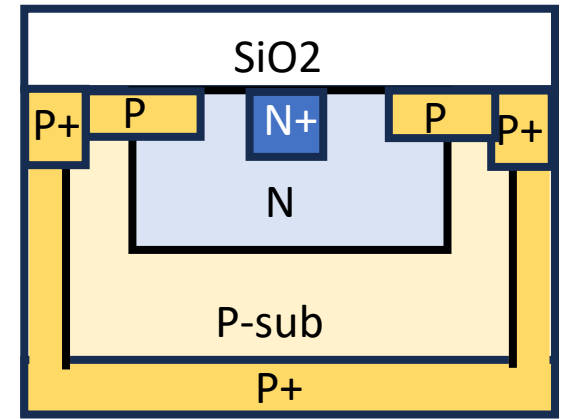
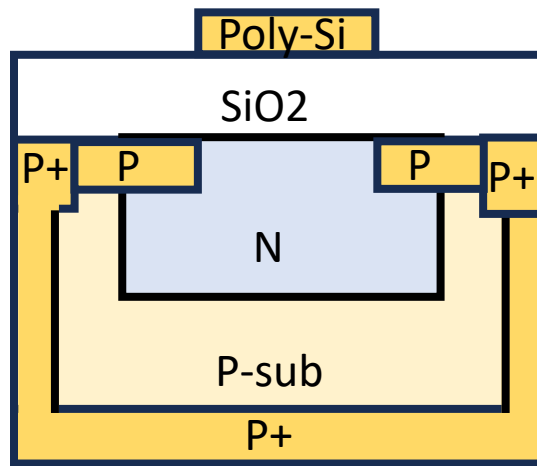
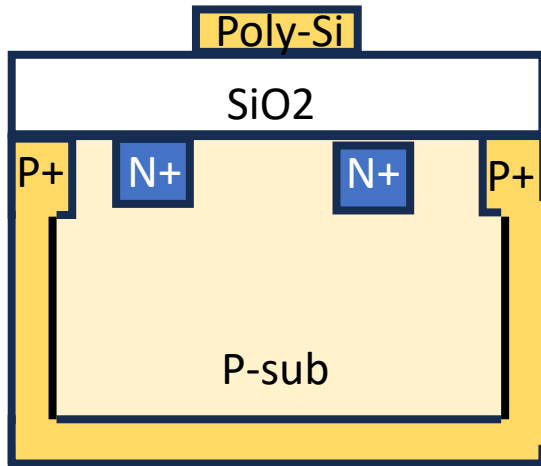
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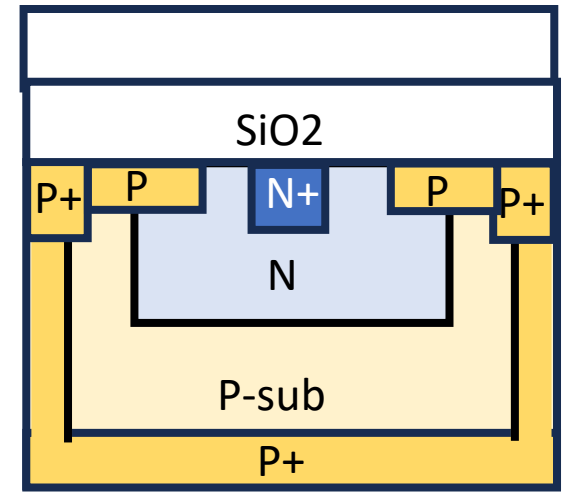
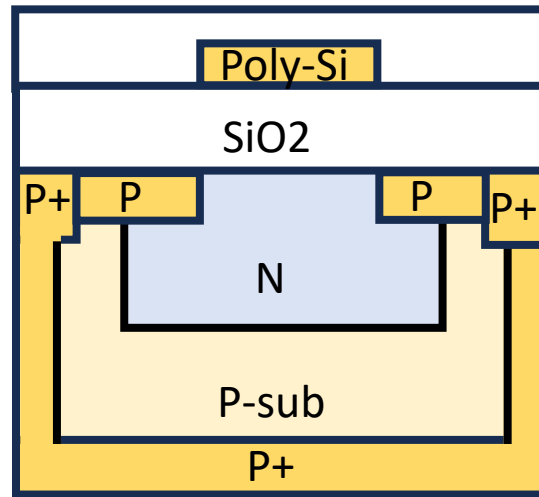
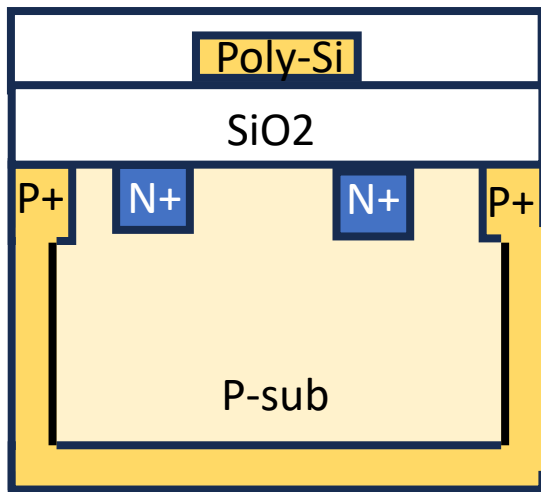
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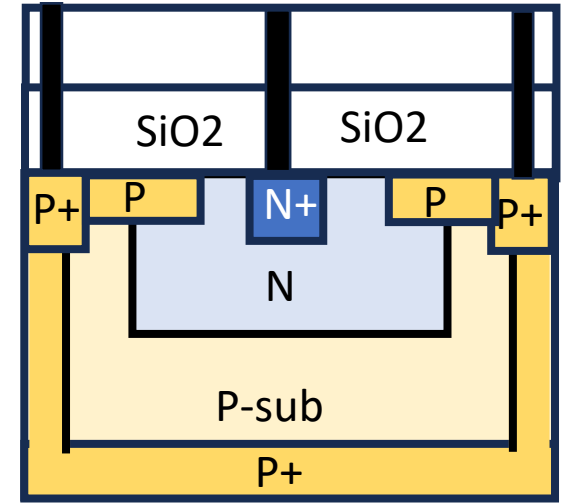
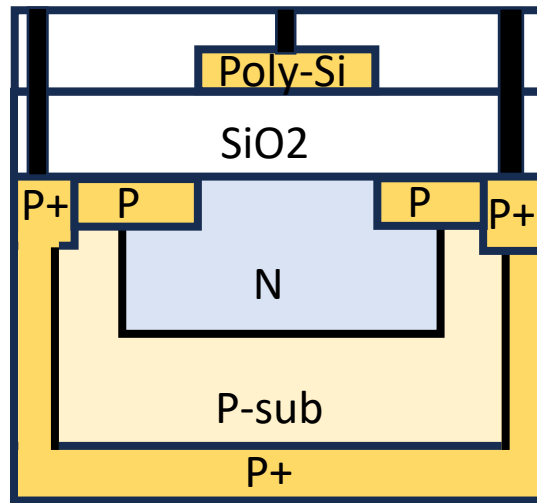
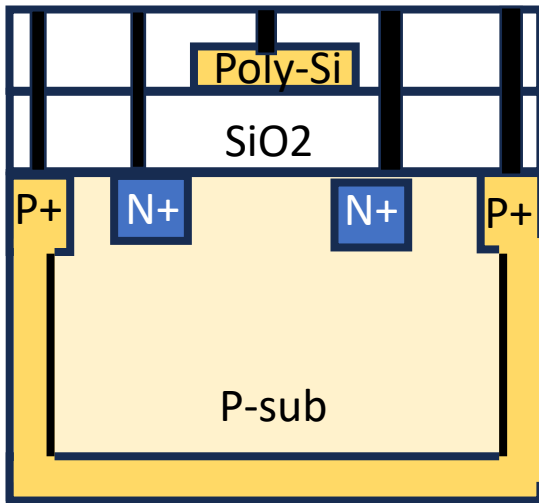
**(3) AIPS 2020**

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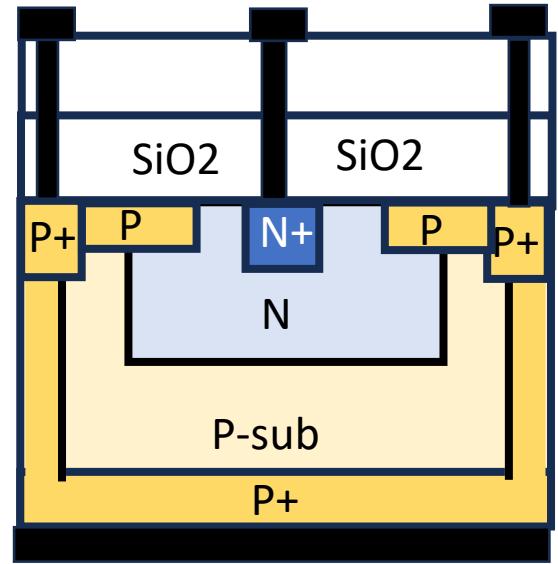
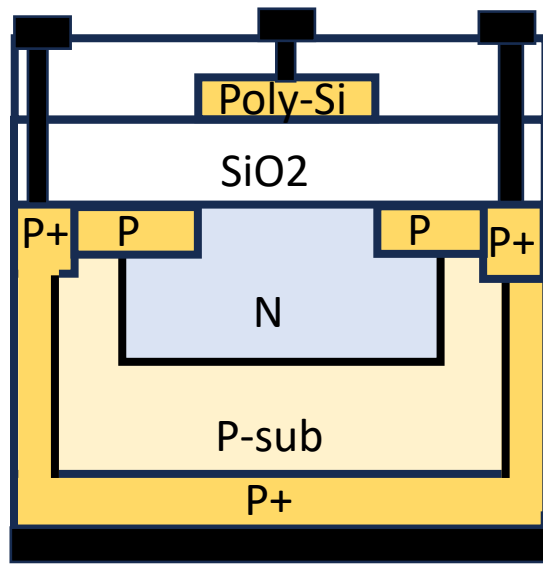
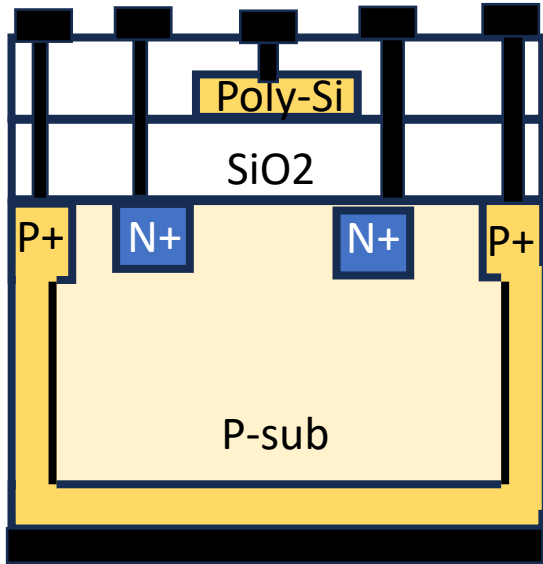
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**MASK 07**



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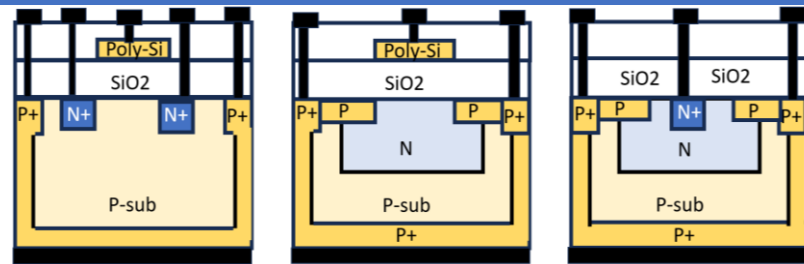
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# 半導体とは？



(1) Intel 1968  
Bob Bower, Caltech

(2) Sony 1978  
Yoshiaki Hagiwara, Caltech/Sony

(3) AIPS 2020  
Yoshiaki Hagiwara, AIPS

