Virtual Gate type Solar Cell Process

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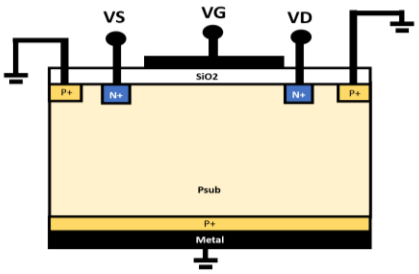
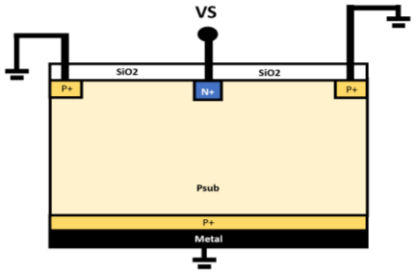
(a) Conventional Process

to form the NMOS transistor
with Four-Mask Basic Process



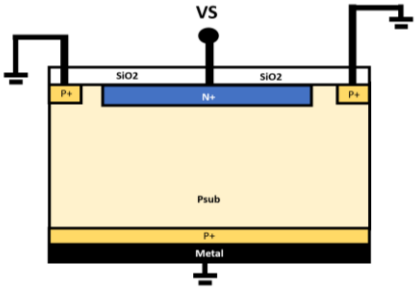
(b) Conventional Process

to form the small N+ diffusion
with Four-Mask Basic Process



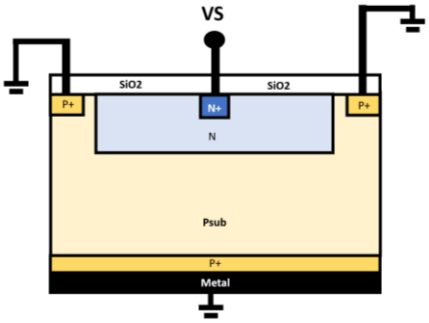
(c) Conventional Process

to form the large N+ diffusion
with Four-Mask Basic Process



(d) Floating-Surface Solar Cell

with One More Mask for
High Energy Ion Implantation
to form the deep N region



(e) Virtual_Gate_type_Solar_Cell

with Another More Mask for
Low Energy Ion Implantation
to form the surface P+ region