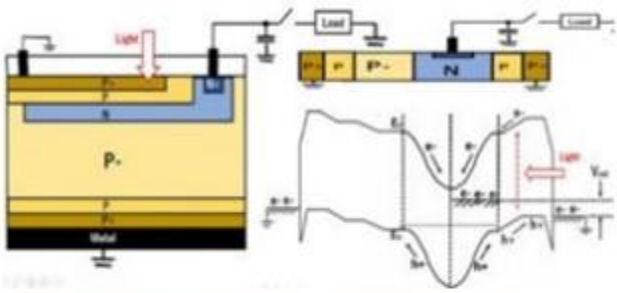

Fig.22 Pinned Buried Photodiode type Solar Cell and its band diagram

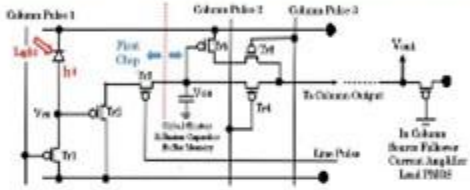

Fig. 23 Active In-Pixel1 Sensor for 3D APS by Hagiwara in 2000

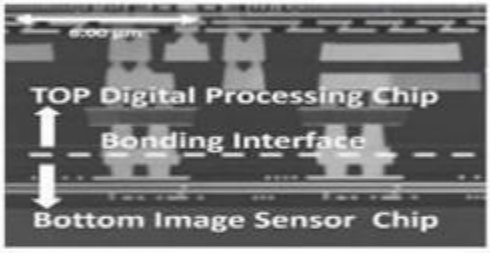

Fig. 24 Sony Two-chip Stacked Back-Lit CMOS Imager

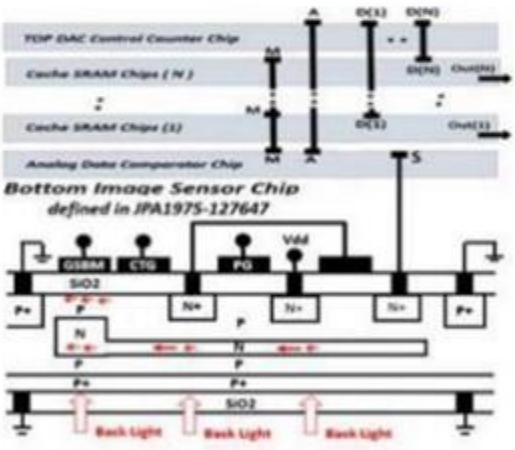

Fig. 25 Active In-Pixel Current AMP 1C6T Circuit (Hagiwara 2020)

Fig. 26 VAR was used in the FIFA at the 2022 World Cup in Qatar.

There is no room and no time for recombination of photo eletron and hole pairs not only at the visinity of the silicon surface but also in the the bulk silicon of the completely depleted buried N- region. By the presense of the strong electric field inside of the empty potential well of the completely depleted buried N storage region and also by creating the surface-barrier electric field generated by the surface conduction band bending created by a careful surface P+P doping engineerings of the surface P+P region, the excellent short-wave blue light sensitivity and also the very low surface dark current can be realized in the double junction Pinned Buried Photodiode type solar cell. See Fig.22.

VIII. Artificial Intelligent Partner System (AIPS)

One very important task of AIPS is the real-time fast compare-and-match operations for the pattern-recognition with big-data. Hardware elements and software elements are both important to realize AIPS. Clever decision making software algorithm must be incorporated the smart robot vision real time system of AIPS.A 128 bit data-stream real-time fast comparator chip was designed by Caltech graduate students in 1972 under the guidance of Prof. C. A. Mead at Caltech and fabricated at Intel in 1973 [26]. This simple 128-bit data-stream comparator was the first attempt to realize the real-time fast big-data compare-and-match operation and the pattern recognition for AIPS.

In order to realize the real-time big-data compare-and-match operations for pattern-recognition and big-data compare-and judge-operations, fast-access-time cache-SRAM chips are also needed for very fast real-time corrections, enhancements and image recognition processing units in AIPS. A fast Cache 4 Mega Bit SRAM with the 25 nanosecond access time world-fastest SRAM was developed by Sony in 1989, with the dynamic bit line load refresh and sense amp circuits invented by Miyaji at Sony, and was used as the very fast digital data buffer memory [27]. Fig. 24 shows the cross sectional view of the two chip stacked back-illuminated CMOS image sensor using the unique cupper technology developed by Sony in 2019 [28]. This was the first development effort to open future image sensor world of 3-D multichip smart-intelligent AIPS robot-vision system [29-35] . Fig.25 shows the concept of the 3D multichip smart real-time vision sensor system (AIPS) with unique in-pixel analog comparator control circuits to generate the match digital output signal (M) from the reference analog voltage (A) and the image sensor analog signal (S).

FIFA's use of VAR at the 2022 World Cup in Qatar was different from the Premier League's use with the addition of a semi-automatic offside system. The new element uses 12 dedicated cameras that tracks the ball and all players to calculate their exact position on the pitch. Each camera, installed under the roof of the stadium, receive 50 data points per second. See Fig.26. They focus on 29 data points, including every limb of every player and the limbs needed for offside. The match ball will also provide a key element. The future of real-time computing will include massive assemblies of parallel processors over mesh-connected wireless networks to execute the vast amounts of computation with vast number of sensors of all types in order to assist the way humans and computers interact in order to meet our human needs.