

(a) J. M. Early 1973 VOD (b) Y. D. Hagiwara 1975 VOD

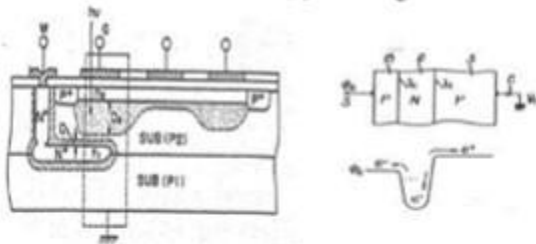


Fig.16 (a) The in-pixel CCD/MOS capacitor type Vertical Overflow Drain (VOD) invented on Dec 3, 1973 in USP3896485 by James M. Early at Fairchild Instrument, USA and (b) the in-pixel double junction type Pinned Photodiode type Vertical Overflow Drain (VOD) invented by Yoshiaki Daimon Hagiwara at Sony on November 10, 1975 in JPA1975-134985.

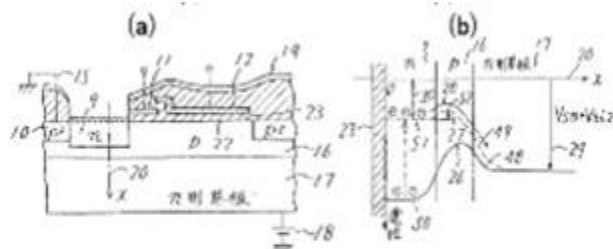
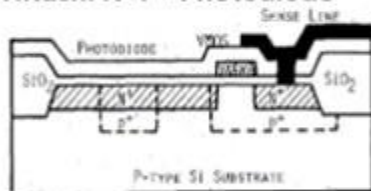
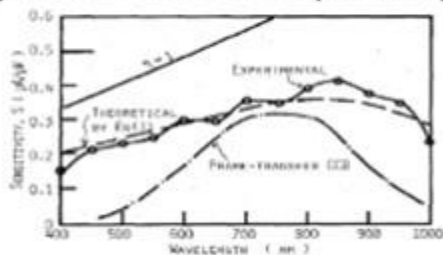


Fig.17 (a) NPN double junction photodiode with floating surface N charge storage and vertical overflow drain (VOD) with punch-thru action and (b) its potential profile defined by Toshiba in JPA1978.-1971 patent application [23].

(a) Hitachi N+P+ Photodiode



(b) Hitachi N+P+ Photodiode Spectral Response



(c) Hitachi P+N+P+ Photodiode JPA1977-837

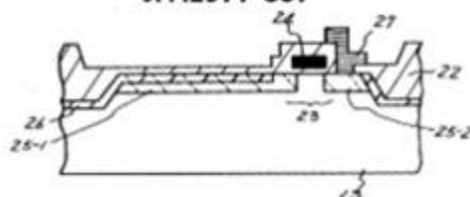


Fig.18 Hitachi N+P+ single junction photodiodes with (a) fully-oxide-exposed floating-surface (b) its spectral response and with (c) partially-oxide-exposed floating-surface and partially-covered by the pinned P+ surface region which is connected to the LOCOS P+ channel stop [24].

Both the heavily doped surface P+ region and the heavily doped P+ channel stops are not enough conditions. They both must be pinned one way or another. Even if the P+ surface of the photodiode is directly connected to the adjacent heavily doped P+ channel stop region, if the P+ channel stop itself is not perfectly pinned, the P+ surface of the photodiode may be floating with some small RC delay time. In this case, the P+ surface of the photodiode is not pinned.

#### IV. DIFFERENCE OF FAIRCHILD VOD AND SONY VOD

Fig.16a shows an in-pixel overflow drain (VOD), built-in with the MOS/CCD type photo capacitor, used in ILT CCD image sensors, and invented on Dec 3, 1973 by James M. Early at Fairchild Instrument [22]. The oxide surface of the MOS/CCD photo capacitor is fixed, pinned and controlled by externally metallic electrode. This photodiode is by definition a pinned surface photodiode and has the complete charge transfer capability and the no image lag. Fig.16b shows an in-pixel double junction type Pinned Buried Photodiode type with in-pixel vertical overflow drain (VOD), invented by Yoshiaki Daimon Hagiwara at Sony on November 13, 1975 [10]. Both sides of the PNP junction photodiode is pinned by the direct metallic contacts. This photodiode is also a pinned surface photodiode and has the complete charge transfer capability and the no image lag problem.

As explained in Fig. 3 before, soon after CCD was invented, in early 1970s, a simple MOS capacitor type Four-Phase CCD delay line with an in-pixel anti-blooming vertical overflow drain (VOD) of the substrate drain type was developed and used widely for frame transfer (FT) type CCD area image sensors. Nothing is new about the concept of in-pixel anti-blooming and vertical overflow drain (VOD) by 1973. However, there is a big difference in types of vertical overflow drain (VOD) between the Fairchild 1973 in-pixel VOD [22] shown in Fig.16a and the Sony 1975 in-pixel VOD [10] shown Fig.16b. The Fairchild 1973 VOD has the unique connection directed upward to the silicon surface while the SONY 1975 VOD has the connection downward to the VOD substrate, opposite to the silicon surface. This is a big difference and they are not the same structure.

#### V. DIFFERENCE OF FLOATING SURFACE PHOTODIODES AND PINNED BURIED PHOTODIODES WITH PINNED SURFACE

Fig.17 shows a NPN double junction photodiode proposed by Toshiba in 1978 with the in-pixel VOD with a floating surface N type photo charge storage region [23]. This photodiode has the serious image lag problem and not Pinned Buried Photodiode by definition. Fig.18a shows a conventional floating-surface N+P+ single junction photodiode developed by Hitachi which has uniquely an adjacent P+ channel stop region formed under the LOCOS isolation region. Fig.18b shows its spectral response with the short-wave blue light range is reported. Fig.18c shows a unique single junction type photodiode with the surface P+ layer by Hitachi [24]. Partially covering the N+ charge storage region, it increases the photo charge storage capacity. The surface P+ layer is directly connected to the adjacent P+ channel stop, formed under LOCOS isolation. But the N storage region is partially exposed to the silicon surface, being floating, again causing the serious image lag problem. This is not Pinned Buried Photodiode.