

Fig.13 Sony 1987 Pinned Buried Photodiode with P+ channel stop formed by high energy ion impalntation and unique lamp anneal method invented by Sony

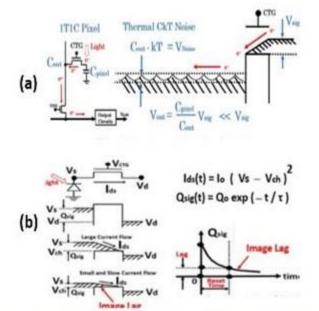


Fig.14 (a) Classical MOS image sensor with a large read-out capacitance C inducing undesired large CkT noise and (b) a large RC delay time constant causing the undesired image lag at the short reset time when the reset-channel resistance R gets larger as the photo charge is drained out thru the transer gate,

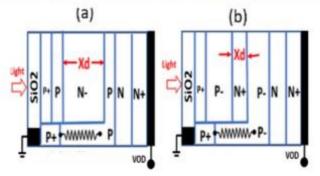


Fig. 15 (a) Lightly-doped N- Buried Storag type P+PN-PN+ triple junction Pinned Photodiode and (b) Heavily-doped N+ Buried Storag type P+P-N+ P-N+ triple junction Pinned Photodiode. Both (a) and (b) type Pinned Photodiode have Veritical Overflow Drain (VOD) applicable for the electronic shutter function. Using Pinned Buried Photodiode originally invented by

The IEDM1982 NEC Buried Photodiode, shown in Fig.10, does not have any adjacent P+ channel stop for pinning the very thin surface P+ photosensor layer [18]. However, the very thin surface P+ photosensor layer itself can be considered to serve as the P+ pinned power ground line instead of any adjacent P+ channel stops. However, the very thin surface P+ region itself may have a very large ohmic resistance since the thin surface P+ region is formed in real productions as a stripe of about 5–10 mm length, determined by the vertical size of the optical lens system, and with a width which is less than the width of one pixel of the photosensor. Consequently, the thin P+ surface photosensor region is a high-R resistive stripe being very thin in depth, very long in vertical direction and very short in horizontal direction.

The adjacent P+ channel stop must be perfectly pinned directly by the surface metal-wire contact one way or another. Only by connecting the adjacent P+ channel stop to the substrate is not enough. Philips [7] and NEC Buried Photodiodes [17-18] have a floating surface with some RC delay time constant to the substrate voltage level. Philips and NEC Buried Photodiodes do not have the surface direct metal-wire contact. They do not have the ideal zero RC time delay with no pinned surface P+ regions.

Ishikawa team at Sony developed and commercialized portable video cameras in 1987 with the perfectly mechanical-parts free electronic shutter capability [20-21], See Fig.13. Sony 1987 Pinned Surface Triple junction type Pinned Buried Photodiode does not have the serious image lag problem.

The adjacent very heavily doped metal-like P+ channel stop is now considered a must to pin the surface P+ photosensor region to achieve the complete charge transfer capability and the no image lag feature, which is also a must to realize the electronic shutter function which becomes possible only by the triple junction type Pinned Buried Photodiode with Clocked Substrate Vertical Overflow Drain (VOD) for electronic shutter function invented by Sony originally in 1975 and developed in 1987.

III. DIFFERENCE OF FLOATIING SURFACE BURIED PHOTODIODE AND PINNED-SURFACE BURIED PHOTODIODE

A conventional 1T1C type claccical MOS image sensor, before CCD image sensors were invented in 1969, has a floatingsurface N charge-collecting storage and suffers the undesired thermal noise CkT due to the large capacitance C of the output line. The device also suffers the undesired image lag because of the short reset time and the channel resistance R of the transfer gate get larger and larger as the photo charge is drained out. See Fig.14. The large output data line capacitance C was the cause of the large CKT noise. It does not matter whether the charge storage N region is buried or not buried. As long as the charge storage N region is floating, the photodiode suffers the serious image lag. The buried N region must be pinned at both sides one way or another. The surface P+ layer side and the other side of the P type region in the bulk substrate both must be pinned one way or another. If the storage N region is floating one way or another, whether it is buried or not, the photodiode suffers the serious image lag.

However, as shown in Fig. 15, for the triple junction type P+P-NPNN+ junction Pinned Buried Photodiode, the surface pinning voltage is not necessarily the same value as the substrate voltage.