Artificial Intelligent Partner System (AIPS) with Pinned Buried Photodiode used for Robot Vision and Solar Cell Panel

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***Abstract*— The future of real-time computing will include massive assemblies of parallel processors over mesh-connected wireless networks to execute the vast amounts of computation with vast number of sensors of all types in order to change the way humans and computers interact in order to meet our human needs. This paper explains the details of the artificial intelligent partner system (AIPS) which was originally introduced in 2008 by Sony, using Play Station III Cell Processor and the intelligent image sensor real-time system, using the Sony Original Pinned Buried Photodiode for future robot vision and solar cell panels with the excellent short-wave blue light sensitivity and the electronic and global shutter function capabilities for fast action pictures.**

Keywords*— *Cell Processor, Pinned Photodiode, Real Time, Robot Vision, Solar Panel, Play Station III, Electronic Shutter

I. INTRODUCTION

The concept of the video assistant referee (VAR), now applied and used worldwide, is very similar to the original concept of the Artificial Intelligent Partner System (AIPS) introduced by Hagiwara in 2008 [1-2]. The first AIPS used Play Station III Cell Processors together with a large number of video cameras to realize a real-time fast-action friendly assistant and care system, supported by the wire-less real-time communication network. Many semiconductor device elements are needed. See Fig.1.

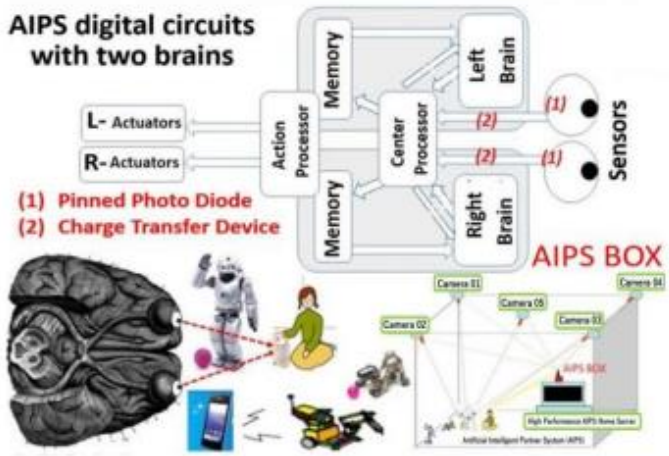

Fig.1 Artificial Intelligent Partner System (AIPS) introduced in 2008

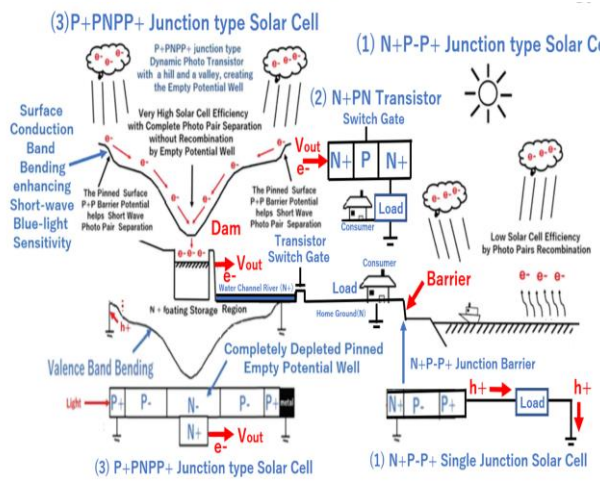

Fig.2 Water Barrier, Water Gate and Water Dam Analogy of Semiconductor.

In the January 2023 issue of IEEE EDS Newsletter [3], an article was published that explained important semiconductor device aspects, focused on "chronology of silicon-based image sensor development" [4]. The details of development efforts of different types of the pinned photodiodes, now widely used in consumer video cameras, smart phones and real time robot vision system (AIPS) were described in details. Steps towards achieving the excellent short-wave blue-light sensitivity are emphasized. These steps were followed by many successful realizations of the Pinned Buried Photodiodes and their applications in different image sensors and equipment. It concluded that the excellent short-wave blue light sensitivity is the most important feature of Pinned Buried Photodiode.

Fig.2 shows analogy in behaviors of water molecules and charge carriers (electron and hole pairs) in semiconductor devices. It explains the concepts of the N+P-P+ single junction diode as Water Barrier, the P+PN+ double junction bipolar transistor as Water Gate, the P+PN-PP+ double junction Pinned Buried Photodiode as Water Dam and the N+ diffuion buffer capacitor used as Underground Water Storage. The silicon-based P+PNP double junction type solar cell structure, by careful engineerings of the silicon surface P+P impurity doping profile, is expected to have a good quantum efficiency.

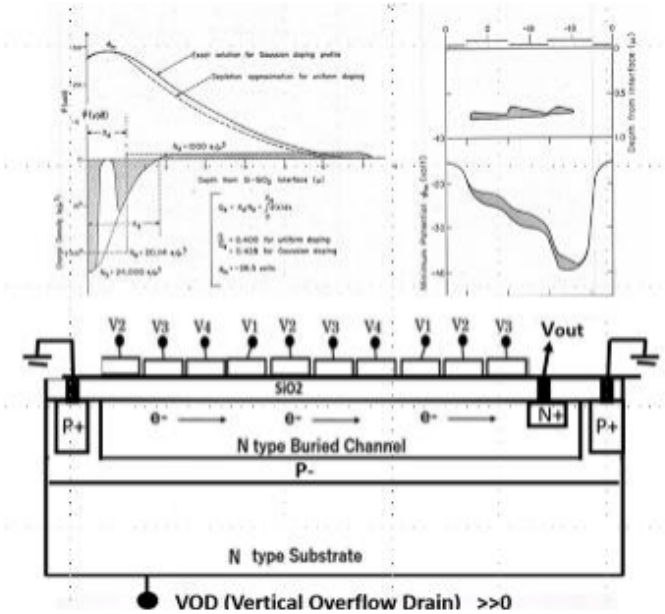

Fig. 3 Simple MOS capacitor type Four-Phase Buried Channel CCD delay line with the substrate type VOD, widely applied in frame transfer (FT) CCD image sensors in early 1970s and the results of its numerical computations reported at the ISSCC1974 conference as PhD student paper by Hagiwara [5-6] in Feb 1974.

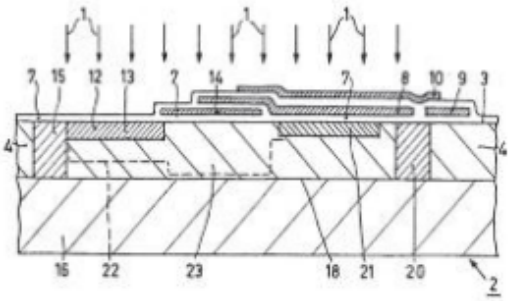

Fig. 4 Philips Buried Photodiode invented on June 9, 1975

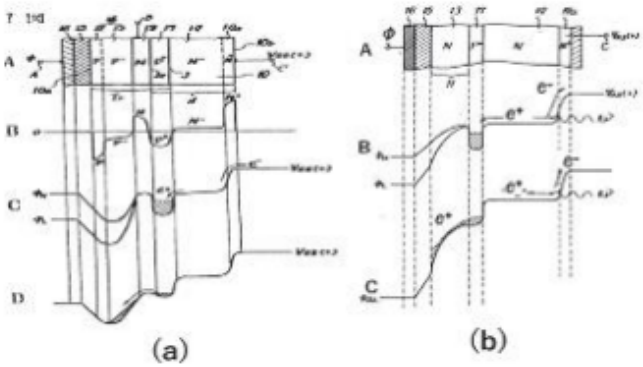

Fig. 5 Sony Pinned Buried Photodiode invented on October 23, 1975

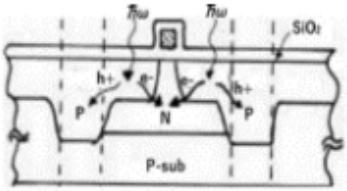

Fig. 6 PNP junction Pinned Phtodiode used by Sony in FTCCD imager in 1978.

In the 2023 January issue of IEEE EDS Newsletter, the author focused on works done by teams from Sony, including double junction-, triple junction-type PPDs, FT PPDs, ILT PPDs, HADs, to name a few. The main author's message is that (i) the short-wave blue light sensitivity is the most important advantage of the double- and multi-junction Pinned Buried Photodiodes, and (ii) Pinned Buried Photodiodes enabled implementation of the electronic shutter in the image sensors and realize the completely mechanical-parts free and light-sensitive video cameras in the HD digital TV era.

Furthermore, in this paper it is added that (iii) Pinned Buried Photodiode is a important semiconductor device element widely used in real-time robot vision future systems including AIPS and VAR and that (iv) the excellent short-wave blue-light sensitive PNP double junction type Pinned Buried Photodiode has another potential future application to realize a high quantum efficiency (QM) solar cells to solve the problem of our future energy crisis.

In this paper, more technical sides of inventions, research and development efforts made by NEC, Kodak, Hitachi and Toshiba are focused and explained. The difference between floating-surface photodiodes and pinned-surface type photodiodes is discussed. And the difference of the floating-surface type and the pinned-surface type Buried Photodiodes are also discussed.

II. Difference of Surace-floating Buried Photodiode and Pinned-surface Pinned Buried Phtodiode

The first charge coupled device (CCD) was invented in 1969, but it was a surface channel type CCD. It had only the 99.9 % or less charge transfer efficiency, which was useless for image sensor and also for DRAM applications because of its power issue. Then, Buried Channel type CCD was invented, which had the 99.999% charge transfer efficiency.

Fig.3 shows a typical Buried Channel Frame Transfer (FT) type CCD image sensor with the back light illumination and the substrate anti-blooming vertical overflow drain (VOD) scheme. By applying a strong substrate voltage, the excess photo charge in high light is drained to the substate VOD.

The complete charge transfer flow of Buried Channel CCD was studied [5] and the results obtained by the computer t-x-y three dimensional numerical calculation were reported at the ISSCC1974 conference in February 1974 in the form of a computer graphics (CG) moving picture by Hagiwara as a PhD student paper [6]. See Fig.3.

Philips invented on June 9 1975 for the first time in the world a double junction type Buried Photodiode [7] and explained the complete charge transfer capability and the no image lag feature by showing an empty potential profile in the charge collecting region in the patent figure. However, the surface layer of Philips Buried Photodiode is connected to the high resistivity substrate and this photosensor may have a serious RC delay time constant problem. Being exposed to the surface oxide, a good light sensitivity is expected. See Fig. 4

Fig. 5 shows the triple and double junction type Pinned Buried Photodiodes invented by Sony on October 23 1975 for the first time in the world [8-10]. Fig. 6 shows the PNP double junction type Pinned Buried Photodiode Sony developed [11-13].

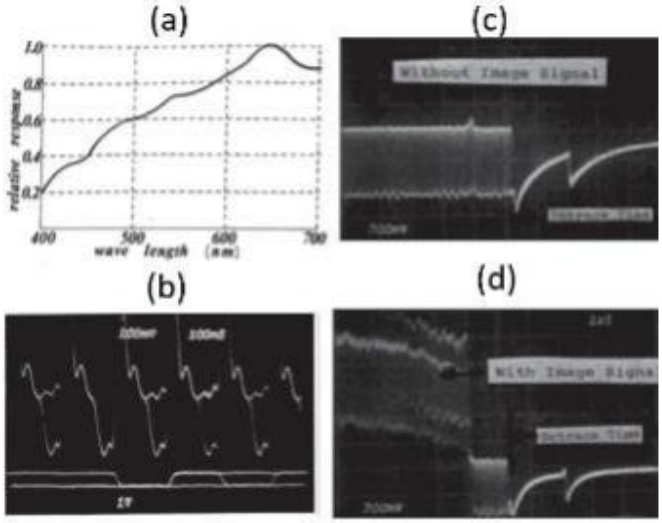

Fig. 7 Spectral Response (a) and output waves showing complete charge transfer of no image lag feature (b) and the very low surface dark current characteristics with out illumination(c) and with illuminaion(d).

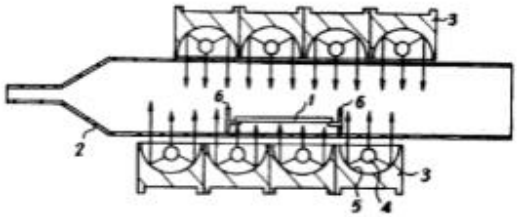

Fig. 8 Unique Lamp Anneal method invented by Nisiyama at Sony in 1981

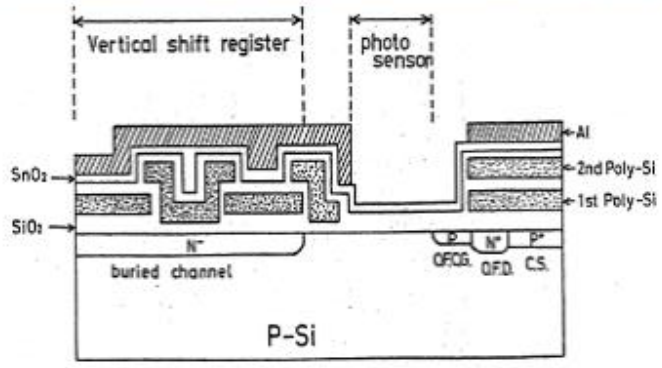

Fig. 9 ILT CCD image sensor with CCD/MOS photo capacitor

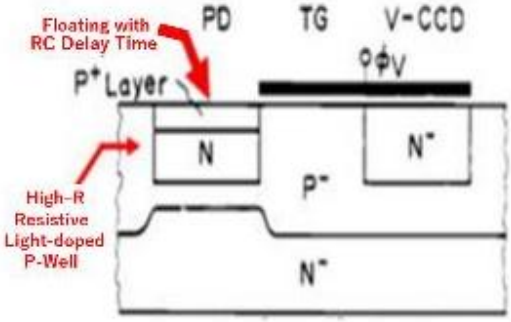

Fig.10 NEC IEDM1982 Buried Photodiode with RC delay

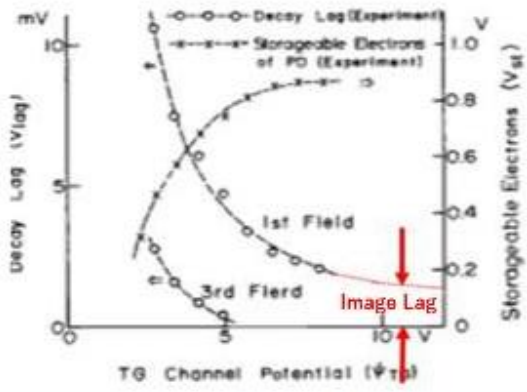

Fig.11 Image Lag reportd by NEC in IEDM1982 Buried Photodiode Paper

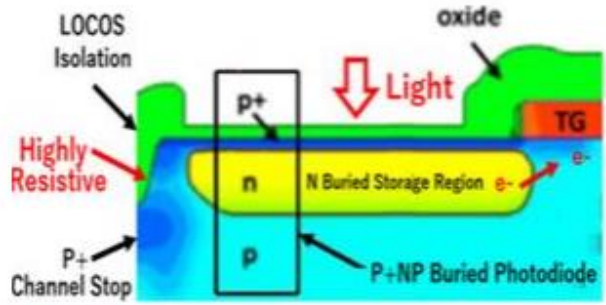

Fig.12 Kodak 1984 Pinned Buried Photodiode with LOCOS P+ channel stop

Sony developed PNP double junction type Pinned Buried Photodiode for the first time in the world in 1977 and 1978, and reported at the SSDM1977 and the SSDM1978 conferences at Tokyo. Complete charge transfer capability of the no image lag and the very low surface dark current were reported. See Fig. 7.

A unique lamp anneal method was invented and developed by Kazuo Nishiyama at Sony [14] and was used in the formation of the perfectly pinned P+ adjacent channel stop with the ideal zero RC delay time constant. Only high energy ion implantation was used in Sony process, without LOCOS isolation nor Shallow Trench isolation. See Fig. 8. Sony also developed Interline Transfer (ILT) CCD image sensor with a thin-polysilicon gate CCD/MOS photo capacitor [15] with the no image lag feature and the clocked OFD electronic shutter scheme [16]. See Fig. 9.

In 1982, NEC developed Buried Photodiode and reported in the IEDM1982 conference [17-18] with image-lag data. NEC used Buried Photodiode in ILT CCD image sensor for the first time in the world. See Fig.10. However, in the NEC Buried Photodiode, serious image lag was observed. See Fig.11. Both Philips and NEC Buried Photodiode are similar. But they both were not Pinned Buried Photodiodes since the surface P+ has a RC time delay and become floating in high frequency operations.

At the IEDM1984 conference, KODAK used P+NP double junction type Pinned Buried Photodiode for the first time in ILT CCD image sensor. KODAK Pinned Buried Photodiode has the P+ surface region connected directly, within some distance in depth, to the adjacent P+ channel stop formed under LOCOS isolation [19]. See Fig.12. KODAK named the device as Pinned Photodiode. NEC reported the serious image lag data while KODAK reported the no image lag feature.

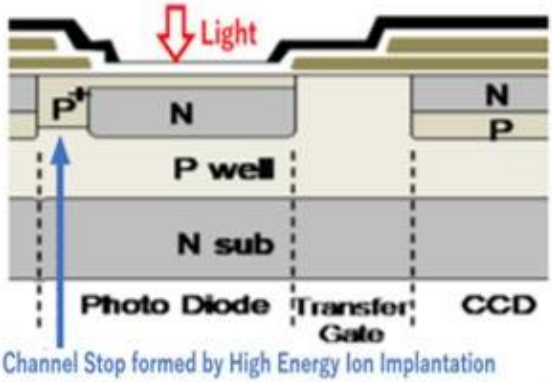

Fig.13 Sony 1987 Pinned Buried Photodiode with P+ channel stop formed by high energy ion impalntation and unique lamp anneal method invented by Sony

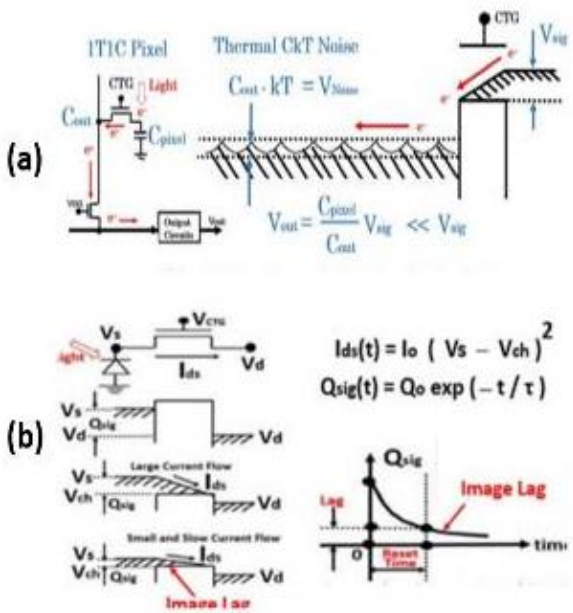

Fig.14 (a) Classical MOS image sensor with a large read-out capacitance C inducing undesired large CkT noise and (b) a large RC delay time constant causing the undesired image lag at the short reset time when the reset-channel resistance R gets larger as the photo charge is drained out thru the tranfer gate,

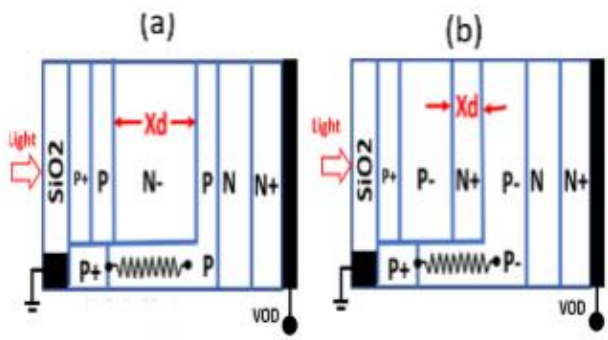

Fig.15 (a) Lightly-doped N- Buried Storag type P+PN-PN+ triple junction Pinned Photodiode and (b) Heavily-doped N+ Buried Storag type P+P-N+ P-N+ triple junction Pinned Photodiode. Both (a) and (b) type Pinned Photodiode have Veritical Overflow Drain (VOD) applicable for the electronic shutter function.

Using Pinned Buried Photodiode originally invented by

The IEDM1982 NEC Buried Photodiode, shown in Fig.10, does not have any adjacent P+ channel stop for pinning the very thin surface P+ photosensor layer [18]. However, the very thin surface P+ photosensor layer itself can be considered to serve as the P+ pinned power ground line instead of any adjacent P+ channel stops. However, the very thin surface P+ region itself may have a very large ohmic resistance since the thin surface P+ region is formed in real productions as a stripe of about 5~10 mm length, determined by the vertical size of the optical lens system, and with a width which is less than the width of one pixel of the photosensor. Consequently, the thin P+ surface photosensor region is a high-R resistive stripe being very thin in depth, very long in vertical direction and very short in horizontal direction.

The adjacent P+ channel stop must be perfectly pinned directly by the surface metal-wire contact one way or another. Only by connecting the adjacent P+ channel stop to the substrate is not enough. Philips [7] and NEC Buried Photodiodes [17-18] have a floating surface with some RC delay time constant to the substrate voltage level. Philips and NEC Buried Photodiodes do not have the surface direct metal-wire contact. They do not have the ideal zero RC time delay with no pinned surface P+ regions.

Ishikawa team at Sony developed and commercialized portable video cameras in 1987 with the perfectly mechanical-parts free electronic shutter capability [20-21], See Fig.13. Sony 1987 Pinned Surface Triple junction type Pinned Buried Photodiode does not have the serious image lag problem.

The adjacent very heavily doped metal-like P+ channel stop is now considered a must to pin the surface P+ photosensor region to achieve the complete charge transfer capability and the no image lag feature, which is also a must to realize the electronic shutter function which becomes possible only by the triple junction type Pinned Buried Photodiode with Clocked Substrate Vertical Overflow Drain (VOD) for electronic shutter function invented by Sony originally in 1975 and developed in 1987.

III. Difference of Floatiing Surface Buried Photodiode and Pinned-Surface Buried Photodiode

A conventional 1T1C type claccical MOS image sensor, before CCD image sensors were invented in 1969, has a floating-surface N charge-collecting storage and suffers the undesired thermal noise CkT due to the large capacitance C of the output line. The device also suffers the undesired image lag because of the short reset time and the channel resistance R of the transfer gate get larger and larger as the photo charge is drained out. See Fig.14. The large output data line capacitance C was the cause of the large CKT noise. It does not matter whether the charge storage N region is buried or not buried. As long as the charge storage N region is floating, the photodiode suffers the serious image lag. The buried N region must be pinned at both sides one way or another. The surface P+ layer side and the other side of the P type region in the bulk substrate both must be pinned one way or another. If the storage N region is floating one way or another, whether it is buried or not, the photodiode suffers the serious image lag .

However, as shown in Fig. 15, for the triple junction type P+P-NPNN+ junction Pinned Buried Photodiode, the surface pinning voltage is not necessarily the same value as the substrate voltage.

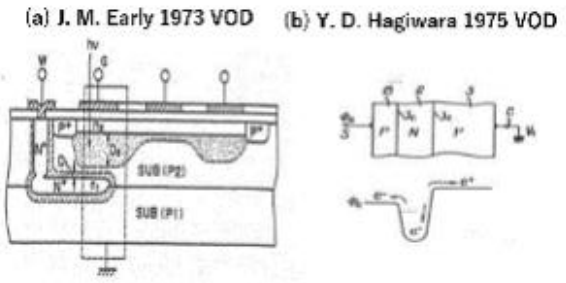

Fig.16 (a) The in-pixel CCD/MOS capacitor type Vertical Overflow Drain (VOD) invented on Dec 3, 1973 in USP3896485 by James M. Early at Fairchild Instrument, USA and (b) the in-pixel double junction type Pinned Photodiode type Vertical Overflow Drain (VOD) invented by Yoshiaki Daimon Hagiwara at Sony.on November 10, 1975 in JPA1975-134985.

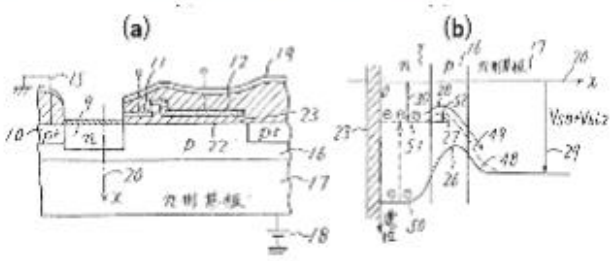

Fig.17 (a) NPN double junction photodiode with floating surface N charge storage and vertical over flow drain (VOD) with punch-thru action and (b) its potential profile defined by Toshiba.in JPA1978.-1971 patent application [23].

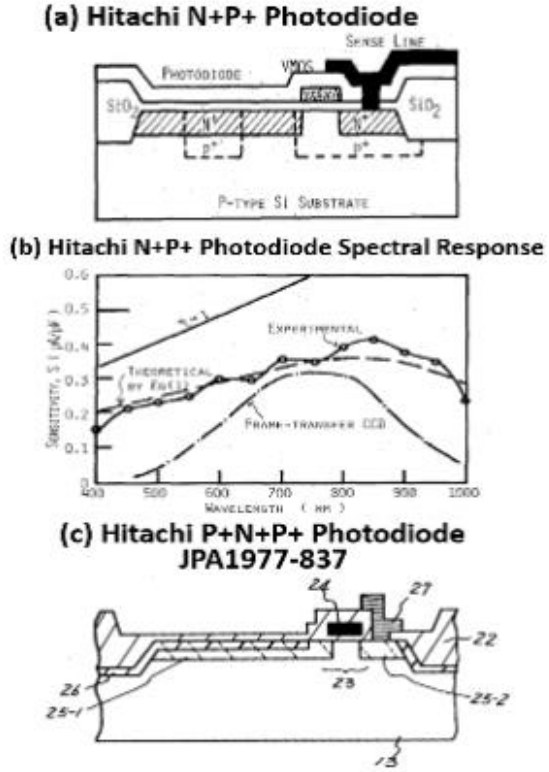

Fig.18 Hitachi N+P+ single junction photodiodes with (a) fully-oxide-exposed floating-surface (b) its spectral response and with (c) partially-oxide-exposed floating-surface and partially-coveed by the pinned P+ surface region which is connected to the LOCOS P+ channel stop [24].

Both the heavily doped surface P+ region and the heavily doped P+ channel stops are not enough conditions. They both must be pinned one way or another. Even if the P+ surface of the photodiode is directly connected to the adjacent heavily doped P+ channel stop region, if the P+ channel stop itself is not perfectly pinned, the P+ surface of the photodiode may be floating with some small RC delay time. In this case, the P+ surface of the photodiode is not pinned.

IV. Difference of Fairchild VOD and Sony VOD

Fig.16a shows an in-pixel overflow drain (VOD), built-in with the MOS/CCD type photo capacitor, used in ILT CCD image sensors, and invented on Dec 3, 1973 by James M. Early at Fairchild Instrument [22]. The oxide surface of the MOS/CCD photo capacitor is fixed, pinned and controlled by externally metalic electrode.This photodiode is by definition a pinned surface photodiode and has the complete charge transfer capability and the no image lag. Fig.16b shows an in-pixel double junction type Pinned Buried Photodiode type with in-pixel vertical overflow drain (VOD), invented by Yoshiaki Daimon Hagiwara at Sony.on November 13, 1975 [10]. Both sides of the PNP junction photodiode is pinned by the direct metallic contacts. This photodiode is also a pinned surface photodiode and has the complete charge transfer capability and the no image lag problem.

As explained in Fig. 3 before, soon after CCD was invented, in early 1970s, a simple MOS capacitor type Four-Phase CCD delay line with an in-pixel anti-blooming vertical overflow drain (VOD) of the substrate drain type was developed and used widely for frame transfer (FT) type CCD area image sensors. Nothing is new about the concept of in-pixel anti-blooming and vertical overflow drain (VOD) by 1973. However, there is a big difference in types of verical overflow drain (VOD) between the Farichild 1973 in-pixel VOD [22] shown in Fig.16a and the Sony 1975 in-pixel VOD [10] shown Fig.16b. The Fairchild 1973 VOD has the unique connection directed upward to the silicon surface while the SONY 1975 VOD has the conection downward to the VOD subtrate, opposite to the silicon surface. This is a big difference and they are not the same strucuture.

V. Difference of Flaoting Surface Photodiodes and Pinned Buried Photodiodes with Pinned Surface

Fig.17 shows a NPN double junction photodiode propsed by Toshiba in 1978 with the in-pixel VOD with a floating surface N type photo charge storage region [23]. This photodiode has the serious image lag problem and not Pinned Buried Photodiode by definition. Fig.18a shows a conventional floating-surface N+P+ single junction photodiode developed by Hitachi which has uniquely an adjacent P+ channel stop region formed under the LOCOS isolation region. Fig.18b shows its spectral response with the short-wave blue light range is reported. Fig.18c shows a unique single junction type photodiode with the surface P+ layer by Hitachi [24]. Partially covering the N+ charge storage region, it increases the photo charge storage capacity. The surface P+ layer is directly connected to the adjacent P+ channel stop, formed under LOCOS isolation. But the N storage region is partially exposed to the silicon surface, being floating, again causing the serious image lag problem. This is not Pinned Buried Photodiode.

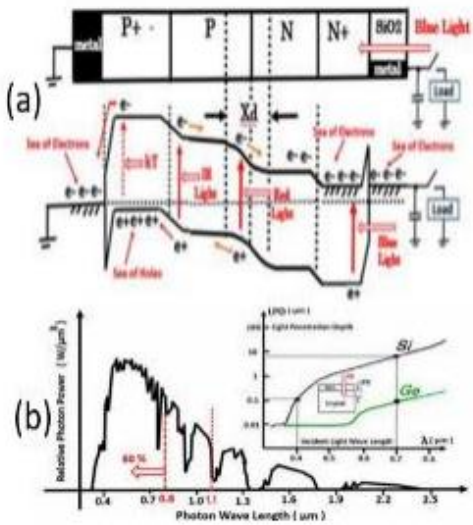

Fig. 19 (a) Single Junction type Solar Cell and (b) Sun Light Spectrum

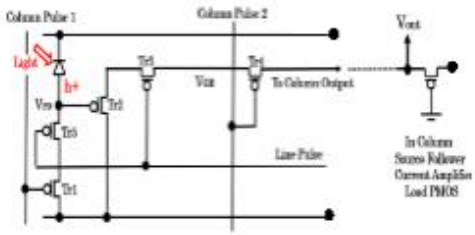

Fig. 20 Active In-pixel source-follower type (APS) PMOS imager invented by Peter Noble in 1968. PMOS transistors were too laerge in early 1970s, now small enough, thanks to the modern advancement of CMOS process scalings.

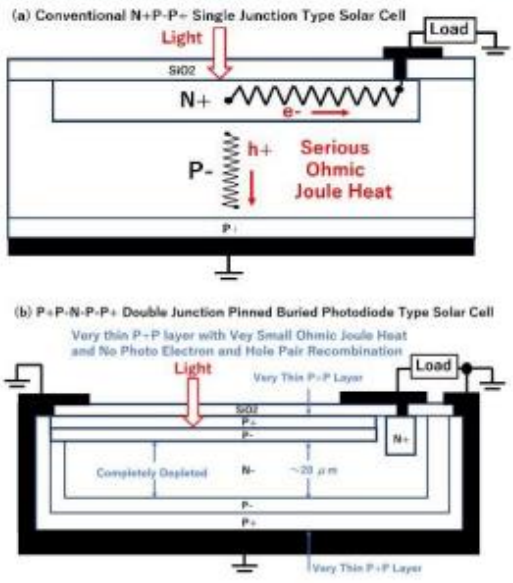

Fig.21 (a) Single Junction Solar Cell and (b) Double Junction Solar Cell.

VI. SILIOCN-BASED PINNED PHOTODIOE TYPE SOLAR CELL

Before CCD image sensor was invented in 1969, the N+P single junction type photodiode, shown in Fig.19a, was used widely both in MOS image sensors and also in ILT CCD image sensors. The single junction type photodiode is still now widely used for low-cost solar cell applications with very low quantum efficiency of less than 20%. In the presence of electric filed, electons and holes can be separeated easily. But ther is no electric filed at the N+ floating silicon surface for the N+P single junction solar cells. The photo electron and hole pairs at the silicon surface stay where they are and eventually sooner or later they all recombine each other and wasted into heat. The sun light contains a plenty of high energy photons of the short-wave blue-light spectrum as shown in Fig.19b. Sun light gives a plenty of the high-energy photons of the short-wave. But they were all wasted because the blue light that cannot penetrate in the deep bulk silicon crystal since the high energy photons cannot penetrate deep into the bulk silicon crystal. They are all recombined at the silicon surface into heat.

VII. ACTIVE IN-PIXEL CURREENT SOURCE AMPLIFER (APS)

Sensitivity of video cameras is defined as the signal to noise (S/N) ratio. Charge Coupled Device (CCD) invented in 1969 and the active pixel sensor (APS) source-follower circuit [25] originally invented by Peter Noble in 1968 both contribute to minimizing the signal noise (N). On the other hand, Pinned Buried Photodiode originally invented in 1975 by Hagiwara at Sony [8-10] has been continuously contributing to maximize the signal (S), since the beginning of development efforts [11-13] by Sony till present. Both CCD and CMOS video cameras are continuously using the triple junction type Pinned Buried Photodiode [8-16] , originally invented by Hagiwara at Sony in 1975, in order to maximize the video cameras signal output (S), since the first development and the production in 1978 by Sony, with the perfect mechanical-parts free electronic shutter function [20-21].

CCD was considered as a super star in the image sensor world till 2000s. Buried Channel type CCD imagers invented in early 1970s showed the excellent 99.999% charge efficiency and achieved the good picture quality in the analog TV era. However, now the typical resolution of a digital high definition (HD) TV picture is about 6000H x 4000V or more. There are more than 10,000 times of the charge transfer steps are required. Consequently the total charge loss for each pixel is more than 10% . Buried Channel CCD loses 0.001 % of the photo-charge per each charge transfer step, 10,000 charge transfer times 0.001 % gives 10% total charge loss, which is too large. Human eyes cannot recognize any noise less than 3% , the 10% noise is too large. CCD became useless in the modern digital HDTV era. A new hero is now on the high-light stage of the image sensor world. As shown in Fig. 20, an active-pixel sensor (APS) has a source-follower type current-amplifier output circuit, which was originally invented by Peter J.W. Noble in 1968 [25] but was never used till recently because the MOS transistor size was much larger than one pixel size in 1970s till early 2000s. In Fig.21, a conversional flat-floating-surface NPP+ single junction type low-QE solar cell structure (a) is compared with a P+PNP-PP+ double junction Pinned Buried Photodiode type (b). The diffrence in the quantum efficiency (QE) between the two photodiode strucutures is very important data to be measured. The double junction Pinned Buried Photodiode type solar cell has the buried N- region being completely depleted of majrity carrier photo electons, being removed swifly and no space for photo electons to be recombined, resulting high QE.

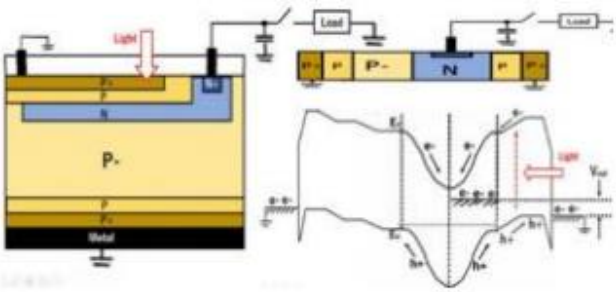

Fig.22 Pinned Buried Photodiode type Solar Cell and its band diagram

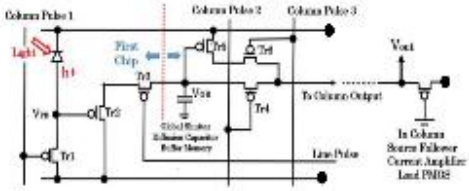

Fig. 23 Active In-Pixel1 Sensor for 3D APS by Hagiwara in 2000

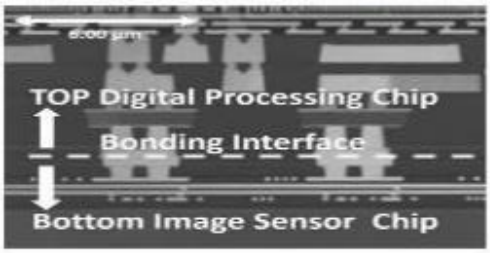

Fig. 24 Sony Two-chip Stacked Back-Lit CMOS Imager

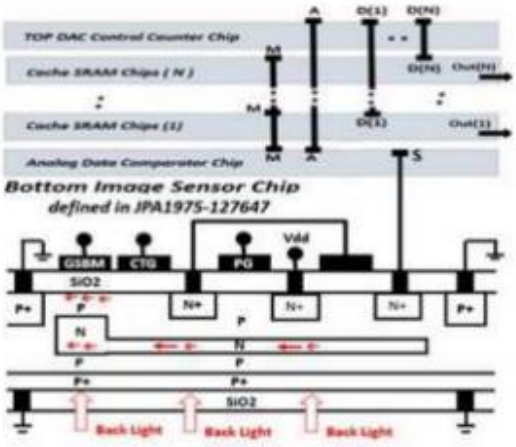

Fig. 25 Active In-Pixel Current AMP 1C6T Circuit (Hagiwara 2020)

Fig. 26 VAR was used in the FIFA at the 2022 World Cup in Qatar.

There is no room and no time for recombination of photo elctron and hole pairs not only at the visinity of the silicon surface but also in the the bulk silicon of the completely depleted buried N- region. By the presense of the strong electric field inside of the empty potential well of the completely depleted buried N storage region and also by creating the surface-barrier electric field generated by the surface conduction band bending created by a careful surface P+P doping engineerings of the surface P+P region, the excellent short-wave blue light sensitivity and also the very low surface dark current can be realized in the double junction Pinned Buried Photodiode type solar cell. See Fig.22.

VIII. Artificial Intelligent Partner System (AIPS)

One very important task of AIPS is the real-time fast compare-and-match operations for the pattern-recognition with big-data. Hardware elements and software elements are both important to realize AIPS. Clever decision making software algorithm must be incorporated the smart robot vision real time system of AIPS.A 128 bit data-stream real-time fast comparator chip was designed by Caltech graduate students in 1972 under the guidance of Prof. C. A. Mead at Caltech and fabricated at Intel in 1973 [26]. This simple 128-bit data-stream comparator was the first attempt to realize the real-time fast big-data compare-and-match operation and the pattern recognition for AIPS.

In order to realize the real-time big-data compare-and-match operations for pattern-recognition and big-data compare-and judge-operations, fast-access-time cache-SRAM chips are also needed for very fast real-time corrections, enhancements and image recognition processing units in AIPS. A fast Cache 4 Mega Bit SRAM with the 25 nanosecond access time world-fastest SRAM was developed by Sony in 1989, with the dynamic bit line load refresh and sense amp circuits invented by Miyaji at Sony, and was used as the very fast digital data buffer memory [27]. Fig. 24 shows the cross sectional view of the two chip stacked back-illuminated CMOS image sensor using the unique cupper technology developed by Sony in 2019 [28]. This was the first development effort to open future image sensor world of 3-D multichip smart-intelligent AIPS robot-vision system [29-35] . Fig.25 shows the concept of the 3D multichip smart real-time vision sensor system (AIPS) with unique in-pixel analog comparator control circuits to generate the match digital output signal (M) from the reference analog voltage (A) and the image sensor analog signal (S).

FIFA's use of VAR at the 2022 World Cup in Qatar was different from the Premier League's use with the addition of a semi-automatic offside system. The new element uses 12 dedicated cameras that tracks the ball and all players to calculate their exact position on the pitch. Each camera, installed under the roof of the stadium, receive 50 data points per second. See Fig.26. They focus on 29 data points, including every limb of every player and the limbs needed for offside. The match ball will also provide a key element. The future of real-time computing will include massive assemblies of parallel processors over mesh-connected wireless networks to execute the vast amounts of computation with vast number of sensors of all types in order to assist the way humans and computers interact in order to meet our human needs.

CONCLUSION

In 1977 Sony developed Pinned Buried Photodiode for the first time in the world [11], originally invented in 1975 [8-10], which has the built-in VOD structure capable of the electronic shutter and snapshot picture functions, and produced for the first time in the world the all-solid-state snapshot fast-action video cameras in 1987 [20-21], and opened a new image sensor world of completely free from mechanical parts. The feature of the global shutter function using an in-pixel MOS capacitor-type global buffer memory became a reality in modern backlit CMOS image sensors by the young generation of Sony engineers after the 45 years since the invention in 1975 [28-35].

Pinned Buried Photodiode [8], with the back light illumination scheme, is the most important feature needed to build the super sensitive modern 3D CMOS image sensor with the high blue-light quantum efficiency and the excellent color reproduction at low light level to capture fast action pictures with no image lag. Future AI traffic control system will need at least the high definition 8K image format of 7680H x 4320V, with 33 million pixels or more, to obtain the details of flash action images, with the in-pixel flash AD converters, and fast Cache SRAM chips. The 3D multichip CMOS image sensor with the more complex future digital circuit system implementations is desired to realize the human friendly artificial intelligent partner system (AIPS). Smart AI image sensors are needed to build the real-time AI robot vision, home AI security and care systems.

And in order to see the specific practical significance and practical solutions for comparisons with other related studies, it remains further to be verified by the research through real experiments and new innovations based on many practical experimental data [36-38].

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Biography: Yoshiaki Daimon Hagiwara graduated California Institute of Technology (Caltech) in Pasadena California USA with BS71 with honor, MS1972 and PhD1975. While working at Sony in Japan during 1975 till 2008, he was engaged in the early developments of image sensor and the digital camera chip set including the ADC, DRAM and high-speed Cache SRAM buffer memory chips and digital processor chips used for the AIBO, PS2 and PS3 cells. He was invited to talk at IEEE sponsored CCD'79, ECS1980, ESSCIRC2001, ESSCIRC2008 and ISSCC2013 conferences for his works at Sony.

In 1992, he also served as a member of JEDEC memory standardization committee and also as the IEC TC47 technical committee chair of the international standard committee (IEC). He also served as the international program chair and an operational committee member in IEEE EDS sponsored ICMTS conferences since 1991 till 2008, IEEE ISSCC conferences for which he served as the ISSCC Asian Committee chair and also as the ISSCC international technical program (ITC) chair in series. He was also a member of the PC and OC since 1991 and now an advisory committee member of IEEE Cool Chips conferences.

In 2008 he founded and worked as the president in the artificial intelligent partner system laboratory (AIPLAB consortium), a nonprofit research organization (NPO) registered by Kanagawa prefecture government in Japan.

Since 1998 till 1999, he served as a visiting professor at Prof. C. A. Mead Lab of the electrical department at Caltech and also at Prof. T.C. McGill Lab of the applied physics department at Caltech. Since 2003 till 2006, he served also as a visiting professor at Prof. H. Kobayashi Lab in the electronic engineering department at Gunma University in Japan.

Since 2009 till 2017, he taught graduate and undergraduate students as a full professor of the information science department at Sojo University in Kumamoto city Japan. Currently he is serving as a specially appointed professor at the president office in Sojo University and also as a member of the educational committee in Society of Semiconductor Industry Specialists (SSIS) in Japan. He is a Caltech Distinguished Alumni and an IEEE Life Fellow.

Speech Title: Artificial Intelligent Partner System (AIPS) with Pinned Photodiode used for Robot Vision and Solar Panel

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