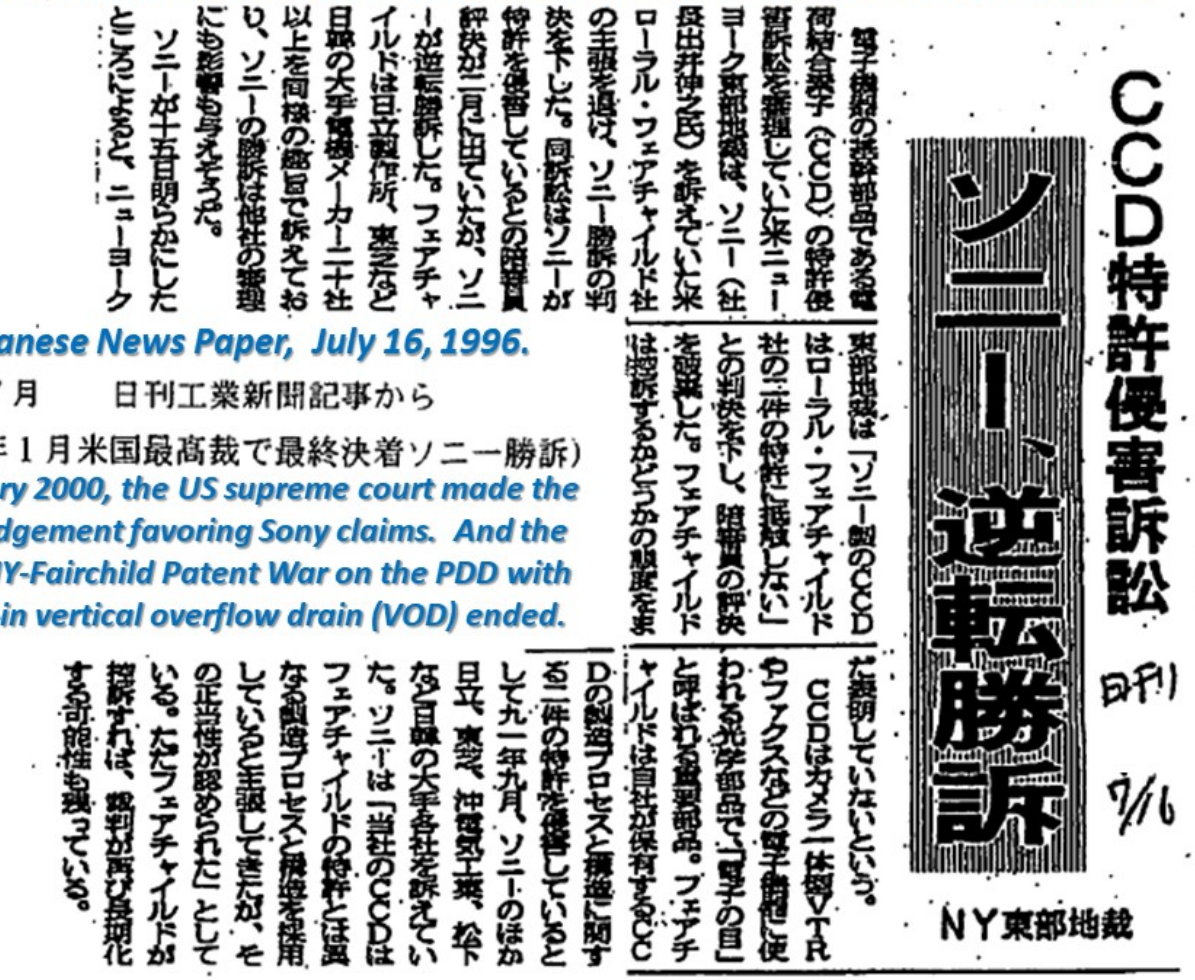
## SONY- Fairchild Patent War (1991-2000) on Pinned Photo Diode with Vertical OFD



CCD特許侵害訴訟

ソニー、逆転勝訴

日刊 7/16

NY東部地裁

電子機器の基幹部品である電荷結合素子（CCD）の特許侵害訴訟を審理していた米ニューヨーク東部地裁は、ソニー（社長出井伸之氏）を訴えていた米ローラル・フェアチャイルド社の主張を退け、ソニー勝訴の判決を下した。同訴訟はソニーが特許を侵害しているとの陪審員評決が二月に出ていたが、ソニーが逆転勝訴した。フェアチャイルドは日立製作所、東芝など日米の大手電機メーカー二十社以上を同様の趣旨で訴えており、ソニーの勝訴は他社の審理にも影響を与えそうだ。

ソニーが十五日明らかにしたところによると、ニューヨーク東部地裁は「ソニー製のCCDはローラル・フェアチャイルド社の二件の特許に抵触しない」との判決を下し、陪審員の評決を破棄した。フェアチャイルドは控訴するかどうかの態度をまだ表明していないという。

CCDはカメラ一体型VTRやファクスなどの電子機器に使われる光学部品で、「電子の目」と呼ばれる重要部品。フェアチャイルドは自社が保有するCCDの製造プロセスと構造に関する二件の特許を侵害しているとして九一年九月、ソニーのほか日立、東芝、沖電気工業、松下など日米の大手各社を訴えていた。ソニーは「当社のCCDはフェアチャイルドの特許とは異なる製造プロセスと構造を採用していると主張してきたが、その正当性が認められた」としている。ただフェアチャイルドが控訴すれば、裁判が再び長期化する可能性も残っている。

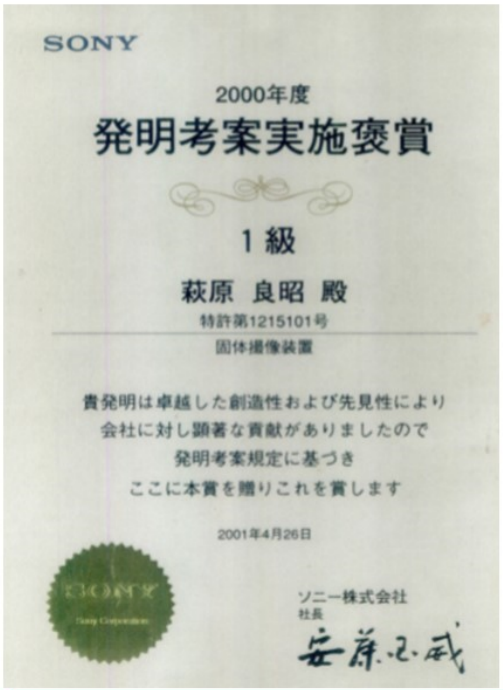
*From Japanese News Paper, July 16, 1996.*

1996 年 7 月　　日刊工業新聞記事から

（2000 年 1 月米国最高裁で最終決着ソニー勝訴）

*In January 2000, the US supreme court made the final judgement favoring Sony claims. And the long SONY-Fairchild Patent War on the PDD with the built-in vertical overflow drain (VOD) ended.*

## 米国Fairchild社とSONYとの特許戦争(1991-2000)の真相



SONY

2000年度

発明考案実施褒賞

1級

萩原　良昭　殿

特許第1215101号

固体撮像装置

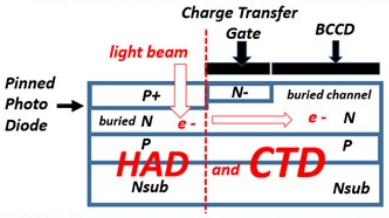
貴発明は卓越した創造性および先見性により
会社に対し顕著な貢献がありましたので
発明考案規定に基づき
ここに本賞を贈りこれを賞します

2001年4月26日

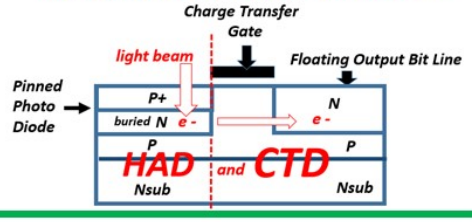
ソニー株式会社
社長
安藤国威

*萩原が1975年発明した　Pinned Photo Diode　は、米国Fairchild社との特許戦争(1991-2000)に勝利し、またNEC社との特許戦争にも勝利し、SONY社内での評価も確立し、やっと萩原は特許褒賞を受けた。*

Case(1)　*Hagiwara Diode 1975 ( Sony HAD ) Application with a Charge Transfer Device ( a CCD type CTD case ) defined in Hagiwara 1975 Japanese Patent 58-1215101*




Case(2)　*Hagiwara Diode 1975 ( Sony HAD ) Application with a Charge Transfer Device ( a CMOS type CTD case ) defined in Hagiwara 1975 Japanese Patent 58-1215101*




See Hagiwara Japanese Patent Application ( 50-134985, 1975 )

## Old Boys of Sony Semiconductor Group support that Hagiwara at Sony is the true inventor of Pinned Photodiode.

各位　　2019年7月25日

半導体産業において、重要な役割を持つイメージセンサの受光素子である、Pinned Photodiodeの発明者は、もとSONYの萩原良昭氏です。萩原良昭氏が1975年に出願した、以下の3件の日本国特許がその証拠です。

昭50－127646、昭50－127647、昭50－134985

この3件の特許の実施例には、この受光素子構造が Interline Transfer方式の CCD Image Sensorにも応用できると明示しています。CMOS Image Sensorにも適用可能で、広く現在採用されています。萩原良昭氏の業績は社会的に認知されるべきものです。

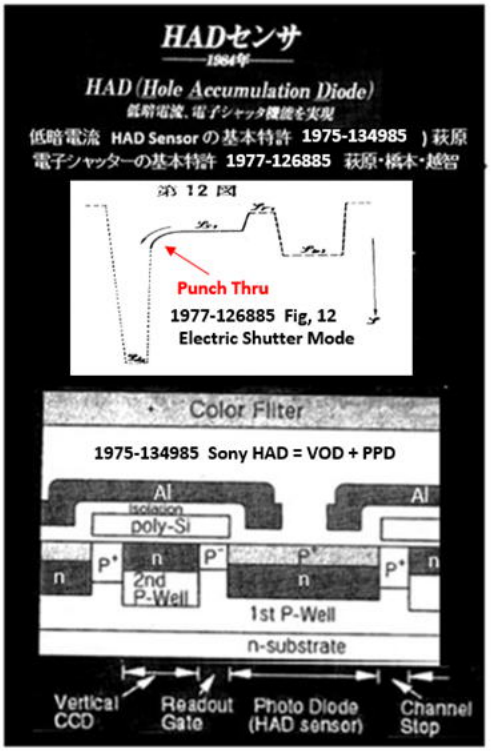
ソニー半導体OB会

会長　露木忠晴　露木忠晴

有志　川名喜之　川名喜之

加藤俊夫　加藤俊夫

## The Pinned Photodiode（Sony Original HAD sensor）Structure



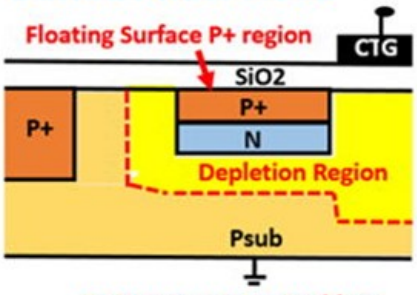

( from SONY Product Catalog )

**Electric Shutter Basic Patent Award from Sony President Idei to Yoshiaki Hagiwara for Japanese Patent 1977-126885 by Hagiwara**

# Difference of Buried Photodiode and Pinned Photodiode

## Figure 5 does not have the P+ channel stop nearby.

### Buried Photodiode




Serious Image Lag Problem

### NEC IEDM1982 Paper

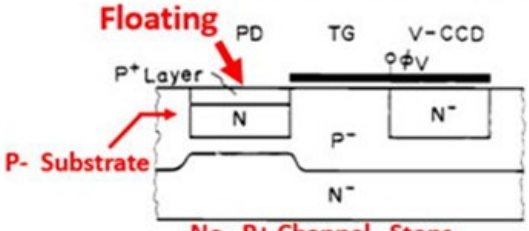
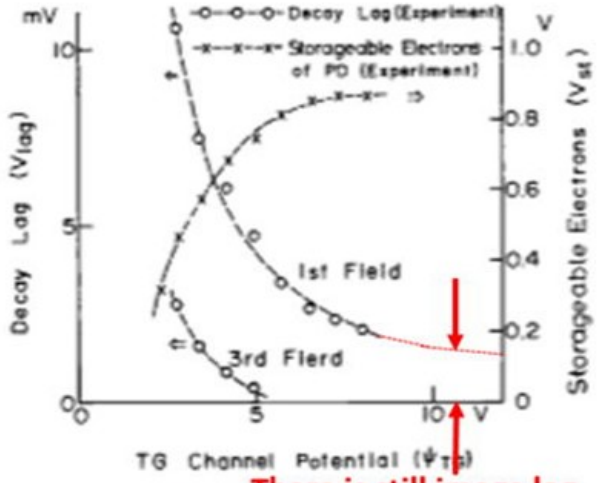



Fig.5. P⁺NP⁻ structure photodiode
(a) Unit cell cross sectional view




There is still image lag
at the CTD gate voltage more than 10 volt.

Fig.6. Storageable electrons vs. transfer gate channel potential, and decay lag vs. transfer gate channel potential in the P⁺NP⁻ structure photodiode

## NEC IEDM1982 Paper reported Image Lag

Figure 6 shows that there is still image lag at the CTG gate voltage of > 10 volt.

## Fossum insulted in his 2014 paper Sony and Hagiwara 1975 PPD invention.

Indeed, Hagiwara invented PPD with VOD and the virtual charge transfer in 1975 !!

IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY, VOL. 2, NO. 3, MAY 2014 33

Sony HAD (PPD+VOD) does not use LOCOS !!!

### A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, *Fellow, IEEE*, and Donald B. Hondongwa, *Student Member, IEEE*

False

Many people now said this is a fake paper !

*C. Other Contributions to the PPD Invention*

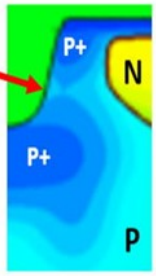
The PPD structure, while invented for low lag ILT CCD application, shares a strong resemblance to the Hynecek virtual-phase CCD structure, with the exception of the VOD. The two inventions were solving different problems with essentially the same device structure and operating principles.

In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top *p* layer was connected by metal to a bias used to control full-well capacity and the *n*-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called "Hole Accumulation Diode," or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the "narrow-gate" CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

The PPD, as it is most commonly used today, bears the strongest resemblance to the Teranishi et al. ILT CCD device. Thus, these days Teranishi is considered as the primary inventor of the modern PPD [29].

False

The surface P+ layer is NOT connected to the LOCOS P+ layer. The surface P+ layer may be floating and this photodiode may have serious image lag.




Serious Image Lag ?

NOT connected

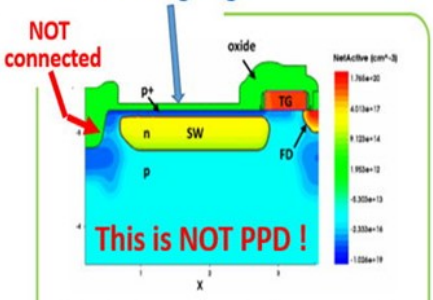



Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

## Hagiwara in 1975 invented PPD with VOD and the virtual charge transfer.

## Study the Japanese Patents 1975-127646, 1975-127647 and 1975-134985.

**Albert J.P. Theuwissen, Jan T.J. Bosiers, Edwin Roks, " The Hole Role ", an invited paper at IEDM2005, Washington DC, Techn. Dig. , 2005.**

But in the case that parts of the depleted n-type CCD channels are not covered by gate material, their surface potential is undefined ! Such a structure will suffer from charge transport issues during operation, because charge can be trapped in local potential pockets. The effect can be solved by defining the potential in the open areas through an extension of the $p^+$ channel stopper. A simple self-aligned implant of $2x10^{13}$ /$cm^2$ boron ions is sufficient to extend the channel stop areas to the gate edge and consequently fix the potential in the open areas [2]. The result after this self-aligned implant is shown in Figure 3. The presence of enough holes plays a crucial role in fixing the potential for the regions "beyond control" of the gates. (Is this structure the mother of the pinned-photodiode or buried diode or hole-accumulation device ?)

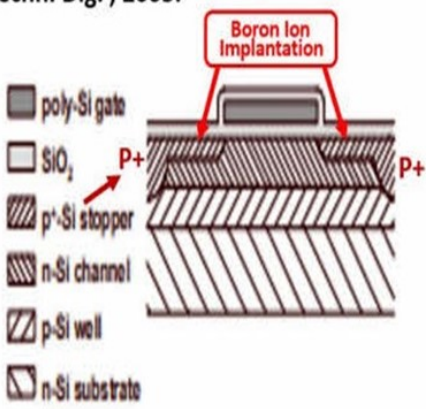



*Figure 3. Cross section of a buried-channel CCD on n-Si substrate including light windows and pinned interface potential in the non-covered CCD channels (the cross section is made perpendicular to the CCD channel).*

[2] Y. Daimon-Hagiwara et.al., Proc. 10th Conf. on Solid-State Devices, Tokyo, 1978, pp.335-340,

ELECTRICALENGINEERING

## Difference between Buried Photodiode and Pinned Photodiode

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

This is a commonly misunderstood misused set of terminologies.

First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

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# Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

Sony Corporation
Sony Semiconductor Solutions Corporation

**https://www.sony.net/SonyInfo/News/notice/20200626/**

## Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

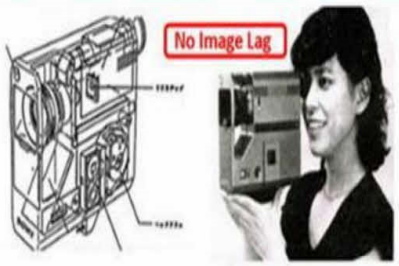
The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

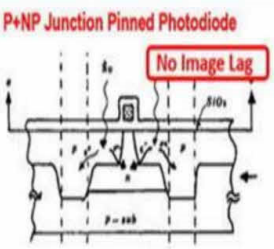
In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

References:
【1】M. Hamasaki, T. Suzuki, Y. Kagawa, K. Ishikawa, K. Miyata and H. Kambe, "An IT-CCD imager with electronically variable shutter speed" , Technical Report of The Institute of Image Information and Television Engineers, vol. 12, no. 12, pp. 31-36, (1988)
【3】Y. Hagiwara, Japanese Patent JP1975—134985
【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)
【6】I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara, "Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain", Technical Report of The Institute of Image Information and Television Engineers, vol. 5, no. 29, pp.

Image Sensor Story

**Sony original 570H x 498 V one-chip FT CCD Image Sensor with Pinned Photodiode, July 1980**




On July 1980, Iwama Kazuo at Sony Tokyo Press Conference and Morita Akio at New York Press Conference announced the one chip CCD video camera with the 8 mm VTR in one box.

**See the Original 1978 Publication of the Pinned Photodiode Sensor**

Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates," Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Appllied Physics , vol. 18, supplement 18–1, pp. 335–340, 1979

**High quality picture of SONY CMOS Imager is also based on SONY HAD ( Pinned Photodiode).**

**These figures shows (1) Excellent Blue Light Sensitivity (2) Low Surface Dark Current and (3) NO Image Lag Features of the P+NP junction type Pinned Photodiode.**

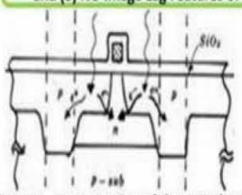


Figure 2 Cross Section of the CCD charge Transfer Region with the P+NP junction tvpe Pinned Photodiode (PPD)

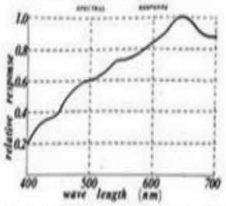



Figure 13 Spectral Response of the P+NP junction Pinned Photodiode (PPD) with the excellent blue light sensitivity

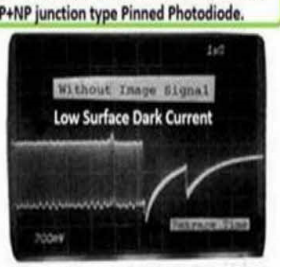




Figure 14 Comparison of CCD image sensor output signals with and without image signal.

## ●発明協会の公式 Homepageの記載には事実誤認があります？

## http://koueki.jiii.or.jp/innovation100/

### イメージセンサー（CCD・CMOS）

概要 | イノベーションに至る経緯 | 発明技術開発の概要 | 主な受賞歴 | 参考文献等

### 概要

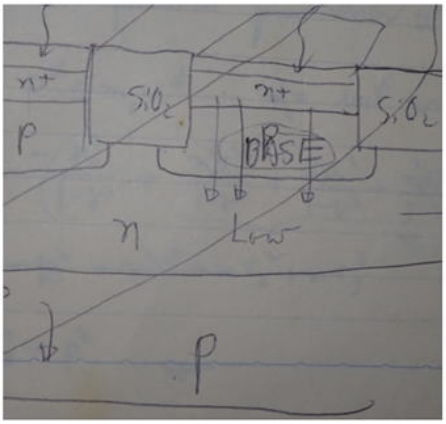
撮像デバイスの研究開発は、19世紀後期のテレビジョン研究がスタートである。機械式、撮像管、固体撮像素子（以下「イメージセンサー」と呼ぶ）と発展し、社会に大きなインパクトを与えつつ、大きく発展してきた。

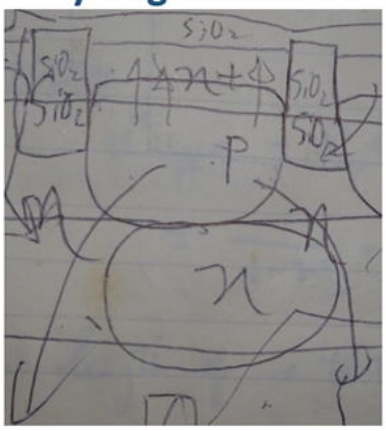
真空管の一種である撮像管は、サイズが大きい、割れ物である、消費電力が大きい、画像にゆがみがある、高価である、などの欠点があり、固体化が望まれていた。1960年代半ばにイメージセンサーの開発がスタートした。そのときは、ＭＯＳ（Metal Oxide Semiconductor）型が中心であった。

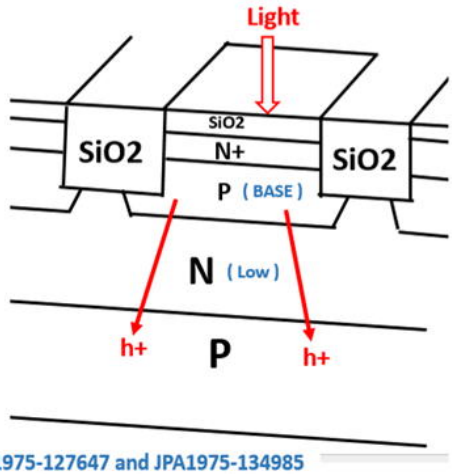
1970年にBoyleとSmith（当時Bell研究所）がＣＣＤ（Charge-Coupled Device、電荷結合素子）を発表した[1]。構造が単純であり、イメージセンサーのような大規模なアレイ構造を製造するのに適していること、矢継ぎ早にＣＣＤに改善が加えられたことから、イメージセンサー開発の中心はＣＣＤになった。1970年後半からは開発の中心は日本に移った。1978年、山田哲生（当時 東芝）は、強い光が入射したときに縦線の偽信号を発生させるブルーミングを抑制する縦型オーバーフロードレイン構造を発明した[2]。1979年には寺西信一（当時 ＮＥＣ）が、白傷や暗電流を大幅に低減し、残像や転送ノイズを解消する埋込フォトダイオード（Pinned Photodiode）を発明した[3]。これらの結果、ＣＣＤはまずムービーを、引き続きコンパクトデジタルスチルカメラを主な市場として量産されていった。

事実誤認？

## The N+PNP junction type Dynamic Photo Transistor Structure Pinned Photodiode and Sony Hole Accumulation Diode (HAD) with the vertical overflow drain (VOD) function invented by Hagiwara at Sony in 1975




Hagiwara's Lab Note at Sony in February 1975

In 1975 at Sony, Yoshiaki Hagiwara filed three Japanese patents JPA1975-127646, JPA1975-127647 and JPA1975-134985 on the Pinned Surface Photodiode with the VOD function which is later called as Sony Hole Accumulation Diode (HAD). Hagiwara did not file a patent on the SiO2 device isolation but this lab note shows that Hagiwara had an idea of forming the Shallow Trench Isolation by the Local Oxidation Method, which was hinted by the LOCOS isolation in 1970s.

To search page

# 1975-80
# Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

**~ Discrete Semiconductor/Others ~**

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Photodiodes are used for photodetectors of image sensors. In 1987, Sony introduced a 2 / 3-inch, 380,000-pixel CCD image sensor (ICX022) using a new type of photodetector, now called a Pinned Photodiode (Sony named it HAD: Hole Accumulation Diode)[1].

The Pinned Photodiode is a photodiode in which the entire N layer is covered with a P layer. The part of the P layer on the light incident surface is heavily doped P+ (Fig-1). Kodak named this structure Pinned Photodiode in 1984 because the P + surface of the light incident surface was pinned to the substrate potential. This device has features such as high light sensitivity, wide dynamic range, image lag free, much smaller dark current due to reduced influence of GR center on the light receiving surface, and no white scars.

In 1975, Sony proposed using a PNP transistor as the photodetector[3]. By providing a P + layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated, greatly improving the light sensitivity. This P + layer was also a proposal to reduce the dark current and image lag which became the basis of the pinned photodiode.

In 1978, Sony presented a 93,000-pixel FT (Frame Transfer) -CCD image sensor compliant with the Analog TV Broadcasting Standard (SDTV) for the first time in the world[5], using the photodiode with the same structure as above. Sony succeeded in 1981 in trial production of a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor by further improvement of this technology[6].

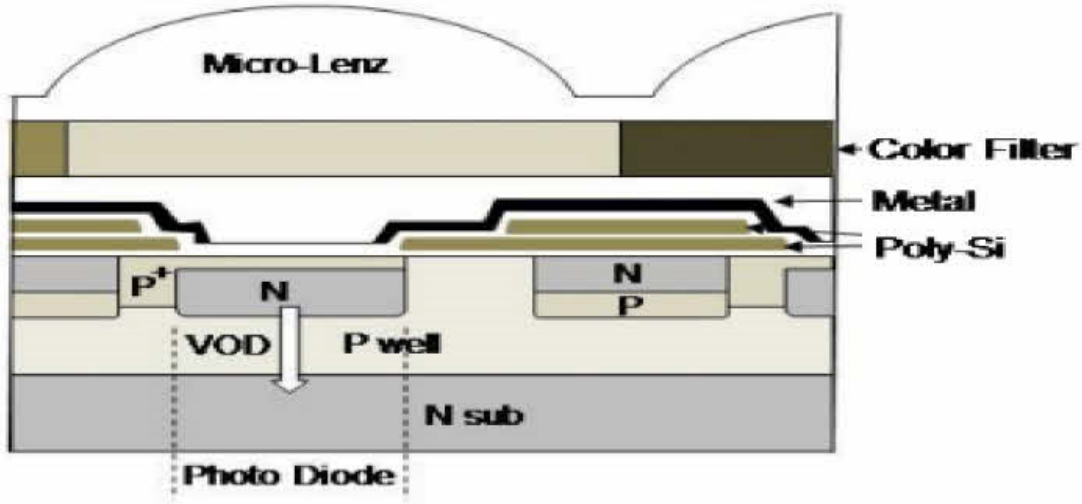



Fig-1 Recent Image Sensor with Pinned Photodiode

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【3】Y. Hagiwara, Japanese Patent JP1975—134985

【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

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