IEEE Symposium on Low-Power and High-Speed Chips

COOL Chips 20

YokohamaJoho Bunka Center, Yokohama, Japan
(Yokohama Media & Communications Center)

April 19-21, 2017

Panel Discussion

Topics: "Cool chips for the next decade"

Yoshiaki Hagiwara

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ISSCC® 2013 | February 17-21

60 Years of (Em)Powering the Future

Plenary Talks (Monday, February 18)

Lisa Su
Senior Vice President and General Manager, AMD

Architecting the Future through Heterogeneous Computing

Martin van den Brink
Executive Vice President and Chief Product & Technology Officer, ASML

Next Generation Lithography : Progress and Outlook

Yoshiyuki Miyabe
Managing Director and CTO, Panasonic

Smart Life Solutions from Home to Cities

Carver Mead
Professor Emeritus, Caltech

The Evolution of Technology

60th Anniversary Distinguished Evening Panel
(Monday, February 18) "Antiques from the Innovations Attic"

Robert Brodersen
Professor Emeritus
University of California, Berkeley

Rinaldo Castello
Professor
University of Pavia

Yoshiaki Daimon Hagihara
Professor
Sojo University

Thomas Lee
Director
Microsystems Technology Office, DARPA

Nicky Lu
Chairman
Etron Technology

Eric Vittoz
Independent Consultant

International Solid-State Circuits Conference

February 17–21, 2013 | San Francisco, CA

Welcome to the 2013 IEEE International Solid-State Circuits Conference (ISSCC). This year, we will celebrate the 60th anniversary of ISSCC. ISSCC is the flagship conference of the Solid-State Circuits Society, and is the premier forum for the presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity to network with leading experts in the field. For 2013, the Conference theme is "60 Years of (Em)Powering the Future". more

Yoshiaki Higihara: The p-n-p-n Diode in Future Linear Motor Cars and in Modern Imagers

John Louis Moll (1921–2011) was studying a p-n-p-n diode switch in his Ph.D. dissertation work when the first ISSCC was held in 1954. In a normal operation mode, this device works as a thyristor, which can drive a large current and is the key device structure of an IGBT applied for a linear motor car of the future (see Figure 9). In a dynamic operation mode, this device may work as a simple p-n-p-n dynamic capacitance that can detect and store one single electron, which is a key device structure of the modern image sensor (see Figure 10).

I recall, when I was taking his physics course at Caltech, that Feynman once said that an electron is always free, moving around rapidly in free space, even in solid, and it

FIGURE 9: The p-n-p-n switch diode for a modern linear motor car.

Yoshi Hagihara, Eric Vittoz and Bob Brodersen.

Yoshiaki Hagihara shared his memories of Richard Feynman, his mentor and educator at Caltech, and how he learned from him that control of electrons is at the heart of all electronic devices. As an example from his attic, he pointed to the old p-n-p-n junctions that are now incorporated in modern-day image sensors.

never stops. It is very hard to catch an electron because we do not know exactly where it is. Our civilization today is based on a technology that controls electrons, down to a single one.

Imagine a photon incident to a bipolar transistor base region. The photon energy creates an electron-hole pair. And the photo-electron can be stored in the base region as one single majority carrier. That is, a bipolar transistor can also function as a photon detector and/or a storage container. I thought that a room in a hotel must be empty and clean before the first hotel guest arrives. So must be this transistor base region empty and clean with no guest electrons at the beginning. This transistor in a dynamic p-n-p capacitor mode is useful since it can capture, confine, and control one single electron. But as a

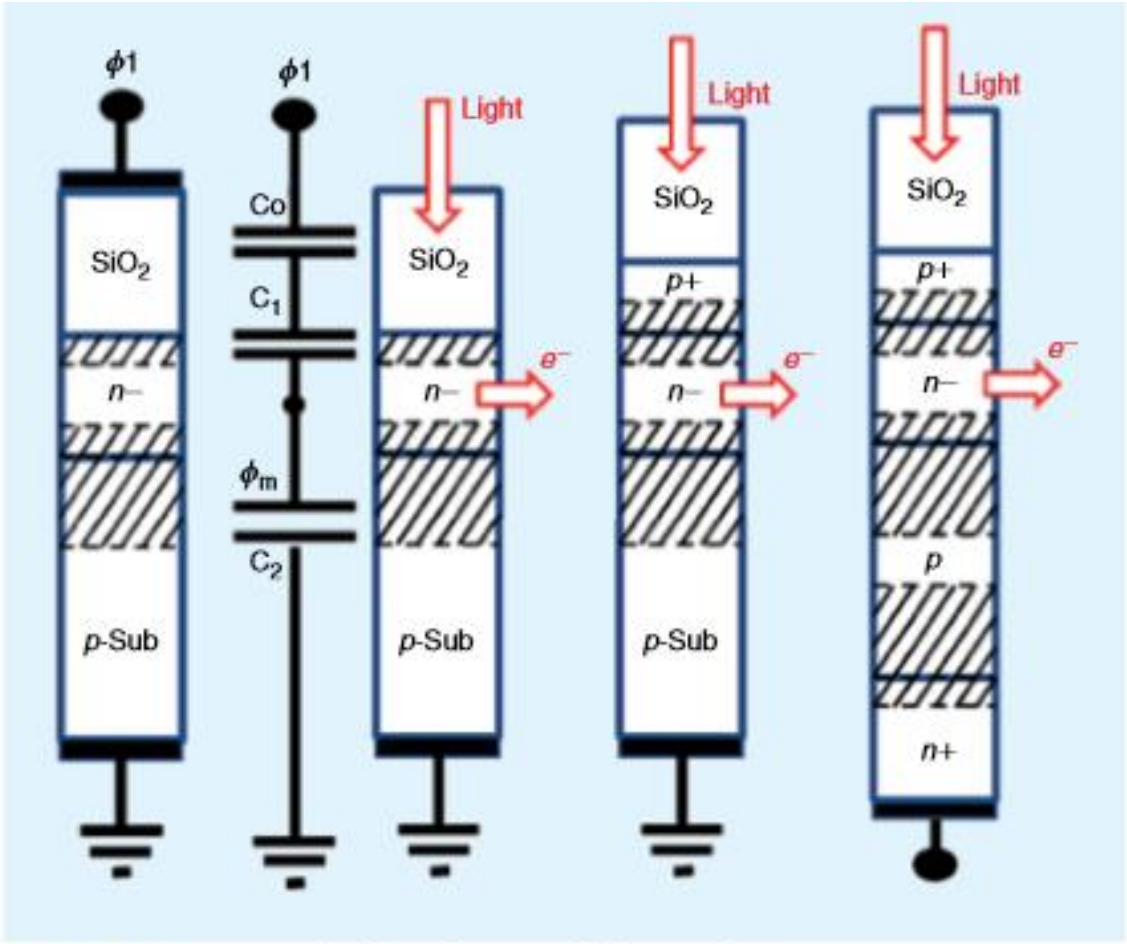
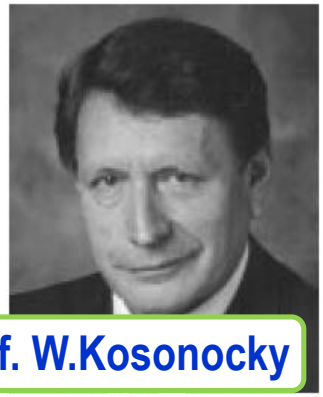


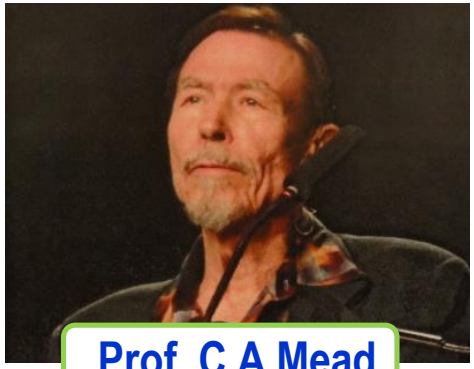
FIGURE 10: From CCD to the dynamic p-n-p-n diode capacitors.

Prof.J.L.Moll



Prof. W.Kosonocky

Prof. R. Fynman



Prof. C.A.Mead

student, I did not know yet how to move that single photoelectron sitting in the base region to the outside world so that we can make use of it as a signal. I had no way yet to know whether the hotel guest has arrived and is resting in the hotel room or not. We had no way yet to ask the hotel guest to come up to the hotel lobby to meet me. I had to wait a few more years (until 1970 in my senior year in college) to find the answer. We all know now it is the CCD structure that can store and transfer one single electron. With a precharge reset set gate and a source-follower circuit, a scheme invented by Walter Kosonocky. We could finally meet our hotel guest at the hotel lobby.

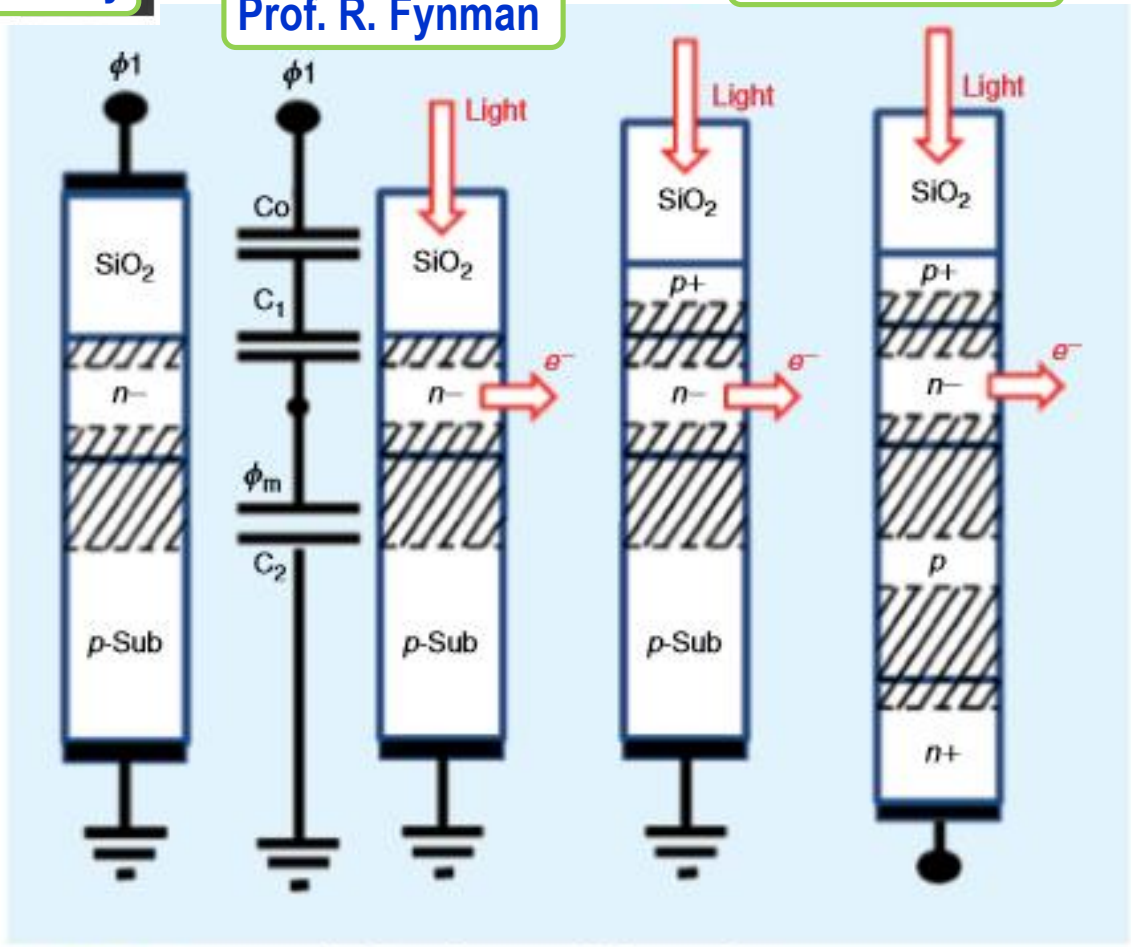


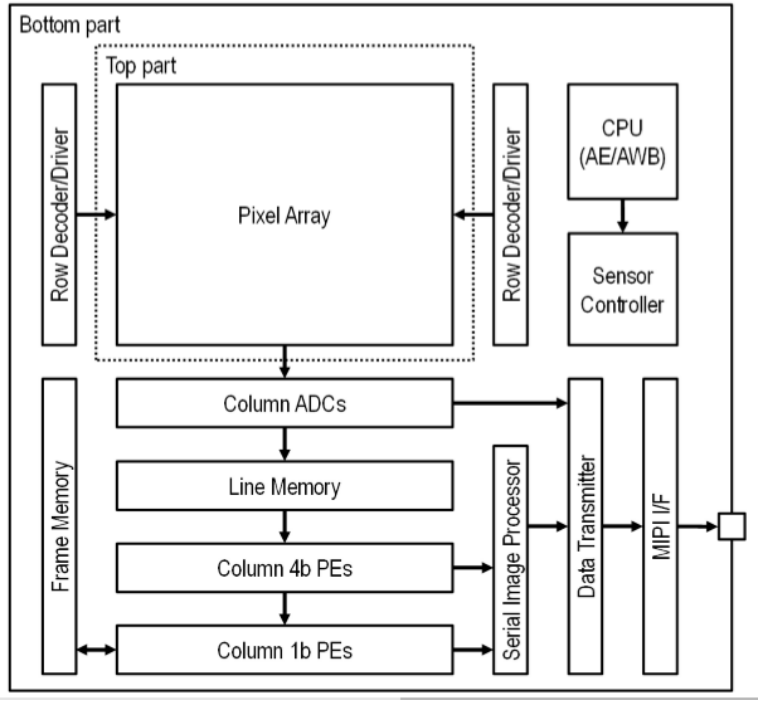
FIGURE 10: From CCD to the dynamic p-n-p-n diode capacitors.

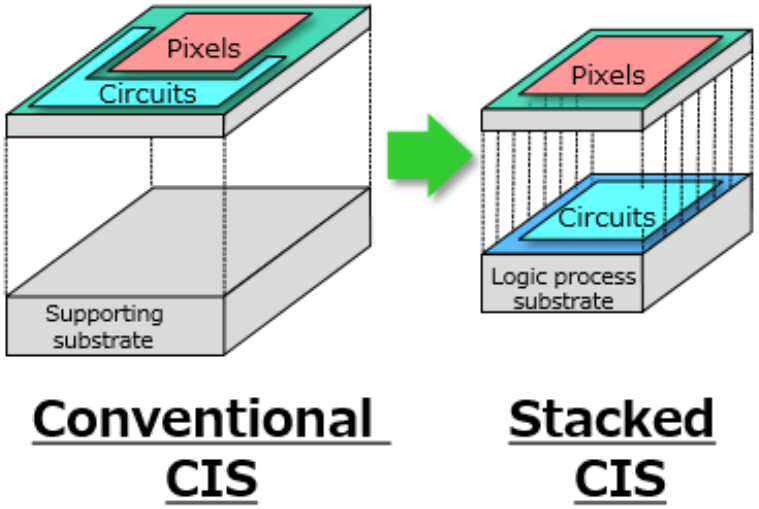
4.9 A 1ms High-Speed Vision Chip with 3D-Stacked 140GOPS Column-Parallel PEs for Spatio-Temporal Image Processing

Tomohiro Yamazaki[1], Hironobu Katayama[1], Shuji Uehara[1], Atsushi Nose[1], Masatsugu Kobayashi[1], Sayaka Shida[1], Masaki Odahara[2], Kenichi Takamiya[2], Yasuaki Hisamatsu[2], Shizunori Matsumoto[2], Leo Miyashita[3], Yoshihiro Watanabe[3], Takashi Izawa[1], Yoshinori Muramatsu[1], Masatoshi Ishikawa[3]

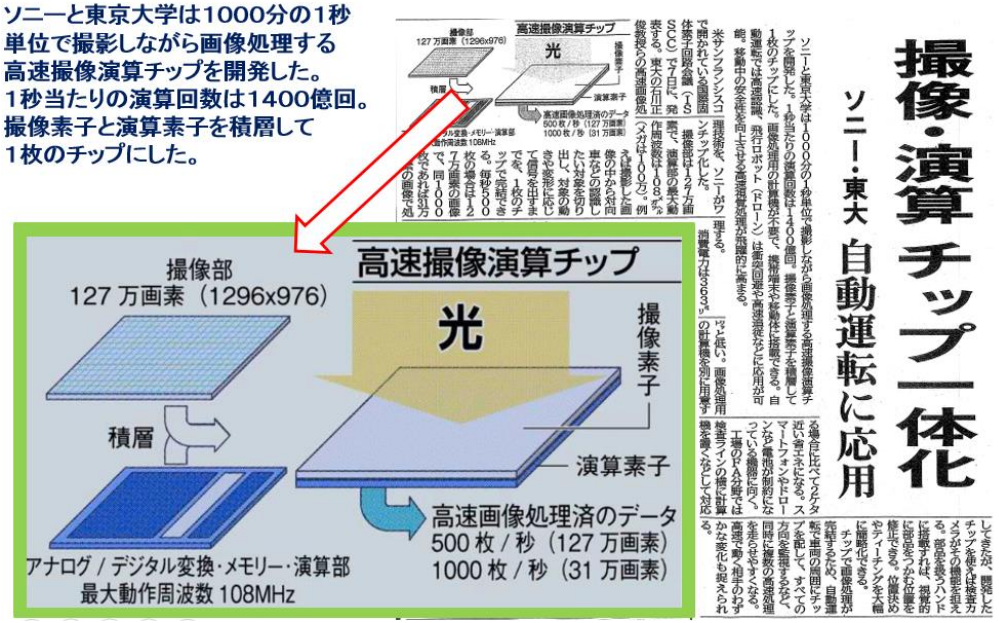
[1]Sony Semiconductor Solutions, Atsugi, Japan
[2]Sony LSI Design, Atsugi, Japan
[3]University of Tokyo, Bunkyo, Japan

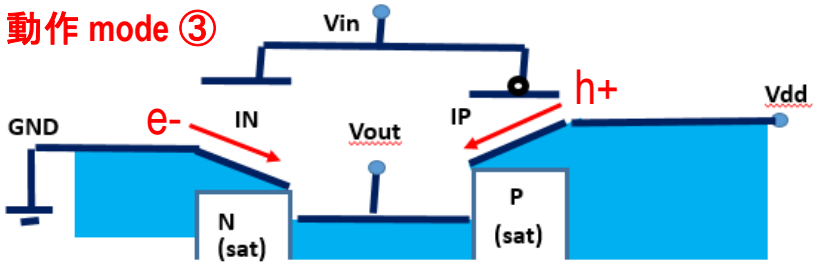
High-speed vision systems that combine high-frame-rate imaging and highly parallel signal processing enable instantaneous visual feedback to rapidly control machines over human-visual-recognition speeds.

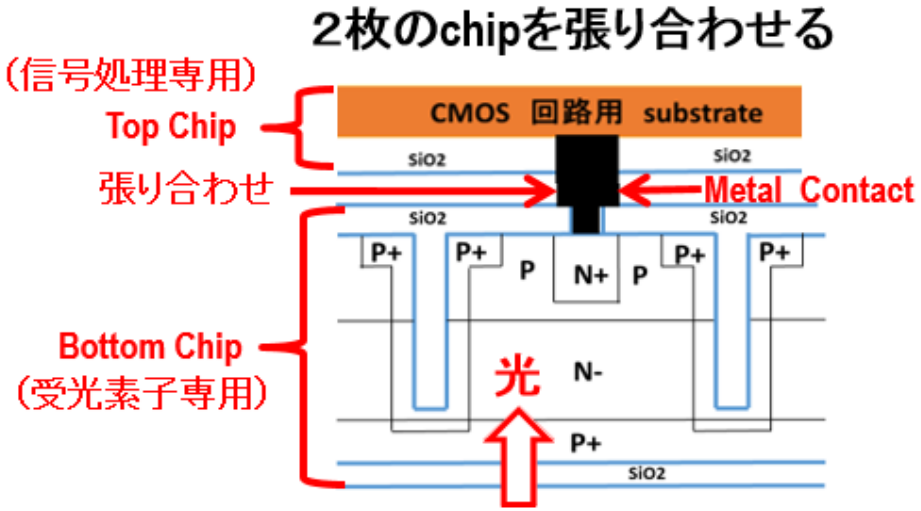


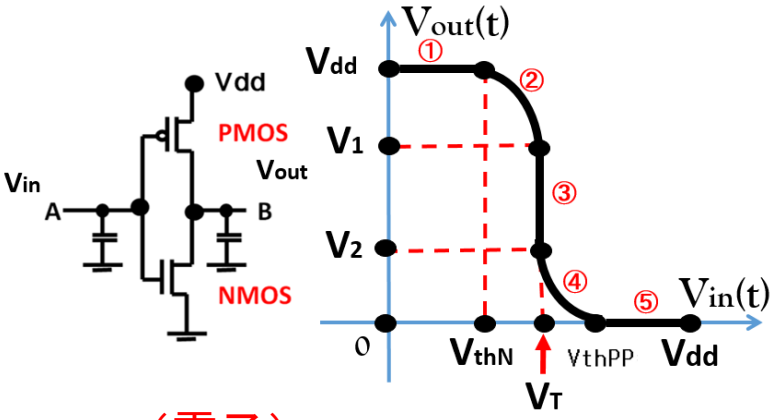


ソニーと東京大学は1000分の1秒単位で撮影しながら画像処理する高速撮像演算チップを開発した。1秒当たりの演算回数は1400億回。撮像素子と演算素子を積層して1枚のチップにした。

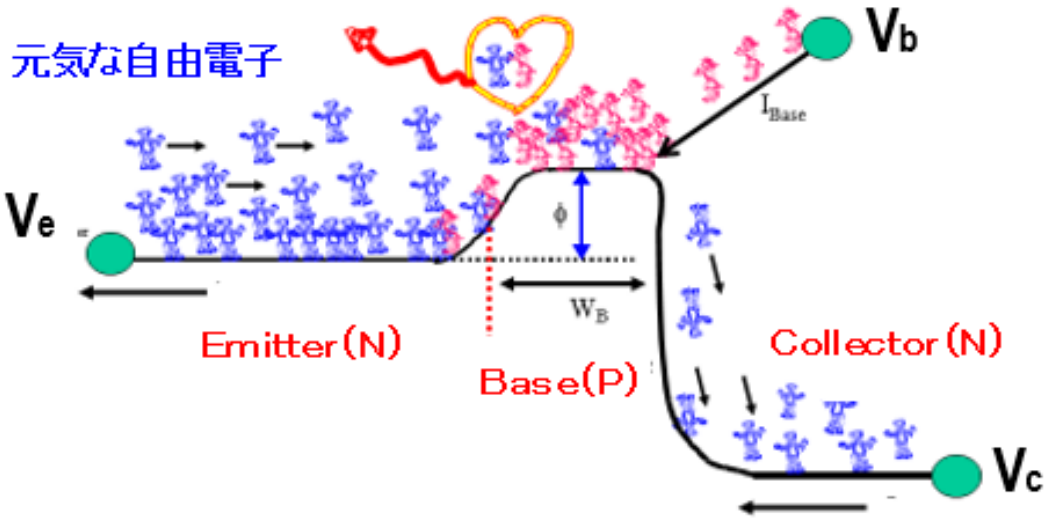



動作 mode ③
Vin
h+
Vdd
GND
e-
IN
Vout
IP
N
(sat)
P
(sat)


2枚のchipを張り合わせる
(信号処理専用)
Top Chip
CMOS 回路用 substrate
SiO2
張り合わせ
Metal Contact
P+
P
N+
Bottom Chip
(受光素子専用)
光
N-


Vout(t)
Vdd
PMOS
Vout
Vin
A
B
NMOS
V1
V2
①
②
③
④
⑤
Vin(t)
0
VthN
VthPP
Vdd
VT

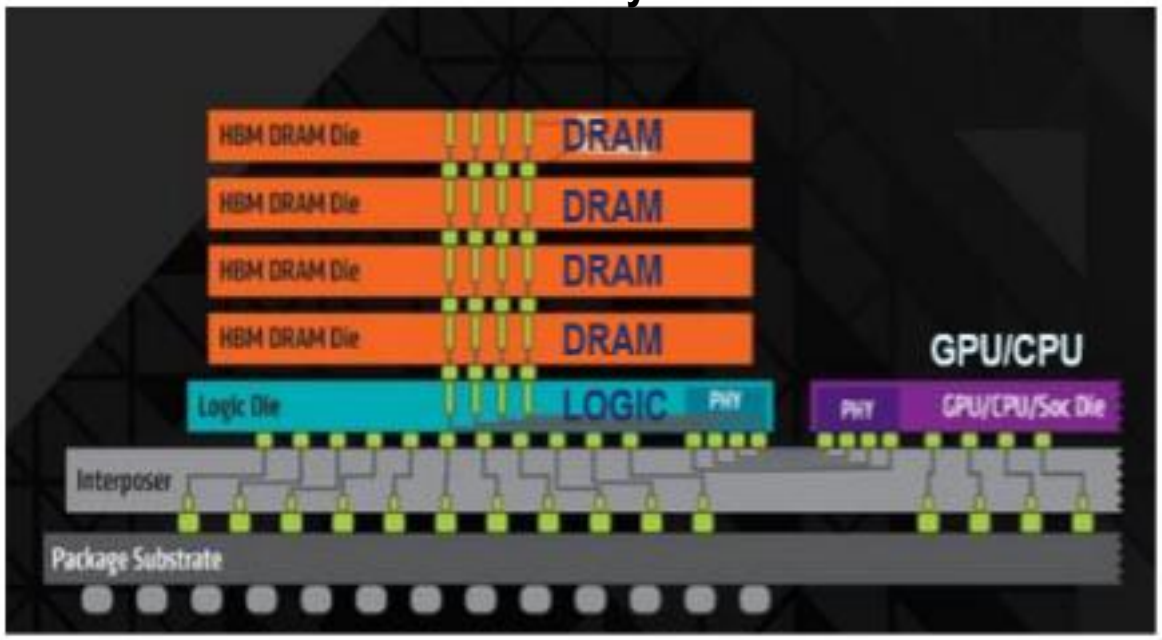
e- =（電子）
h+ =（正孔）

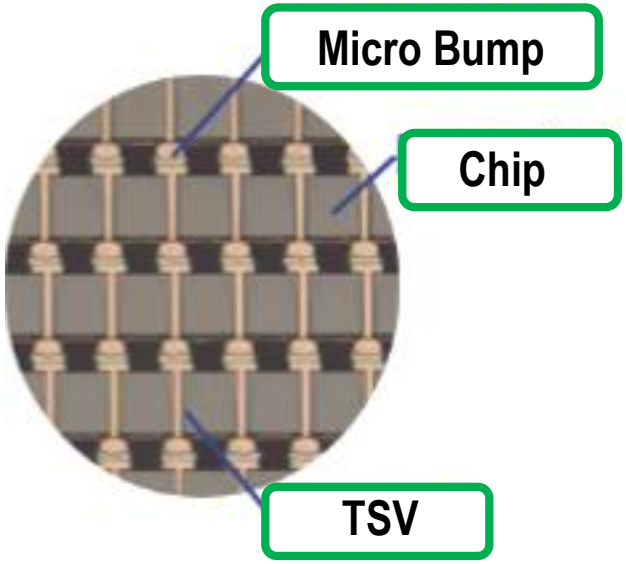

元気な自由電子
Vb
IBase
Ve
ϕ
WB
Emitter(N)
Base(P)
Collector(N)
Vc

Next Generation Memory

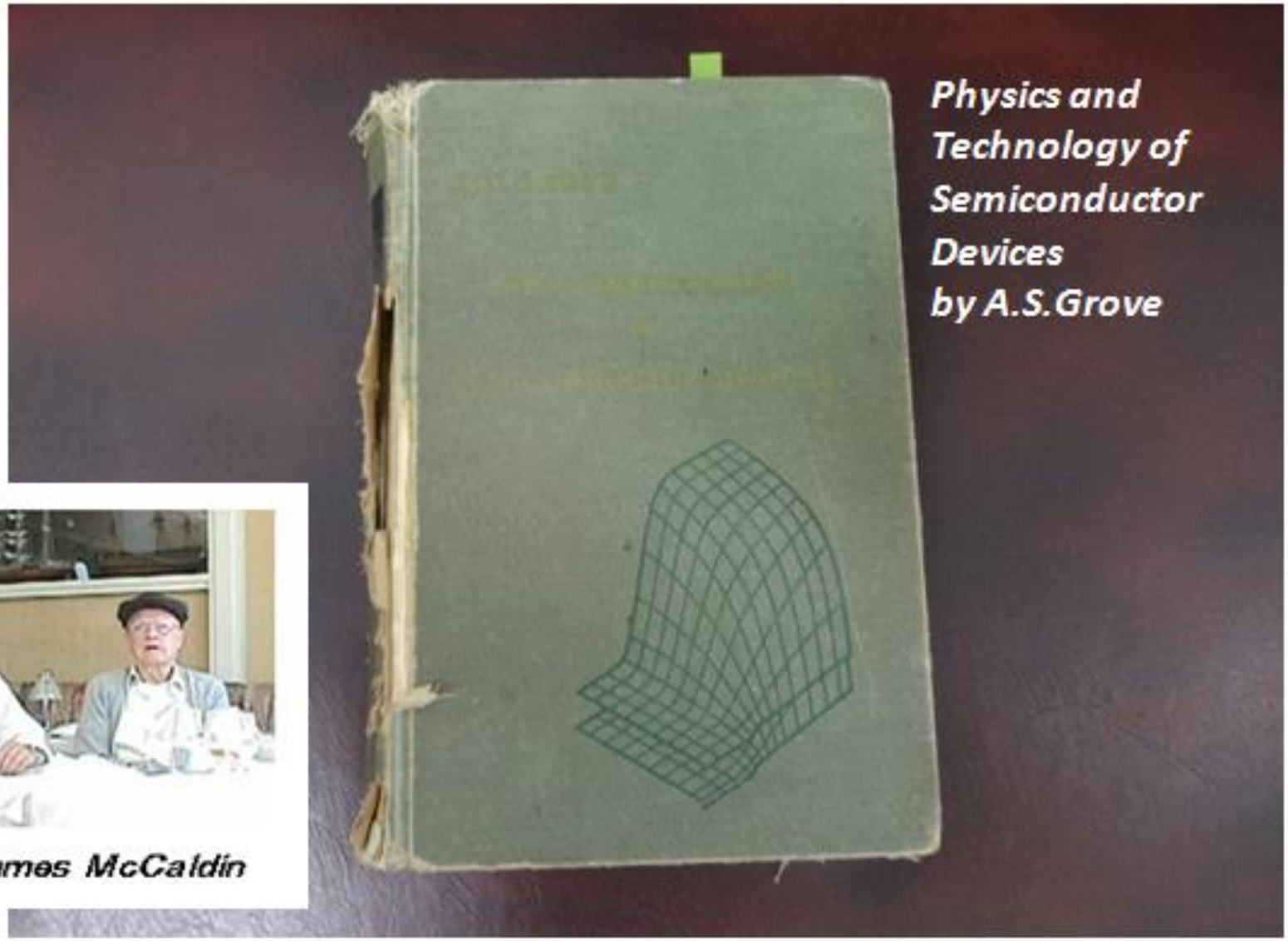
	FeRAM	MRAM	STT-MRAM	PRAM	ReRAM
信号比	10	1	6	100	10,000
微細化	×⇒○	×	○	○	○
読み出し	破壊	非破壊	非破壊	非破壊	非破壊
書換寿命	10^{12}	10^{16}	10^{16}	10^{12}	$>10^{6}$
書込時間	50n～100ns	10ns	＜10ns	＞30ns	＜10ns
セルサイズ	～$15F^2$	～$8F^2$	～$8F^2$	$4F^2$～$6F^2$	$4F^2$

3D memory stack

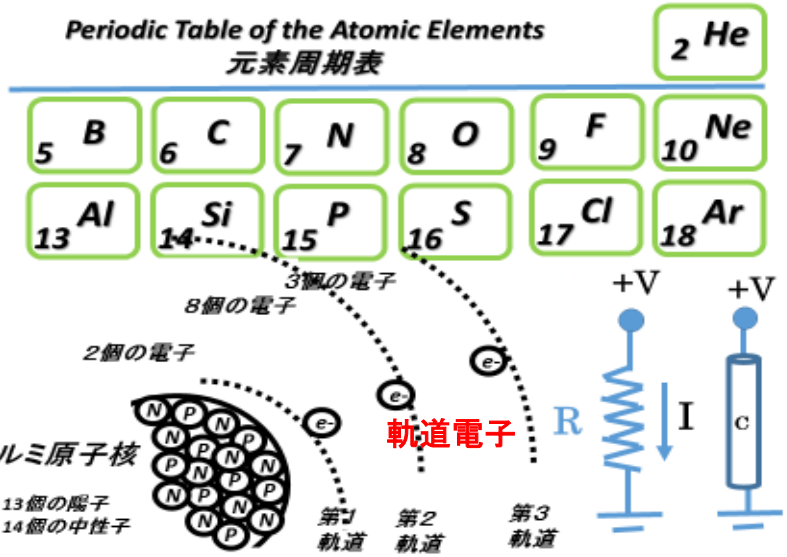


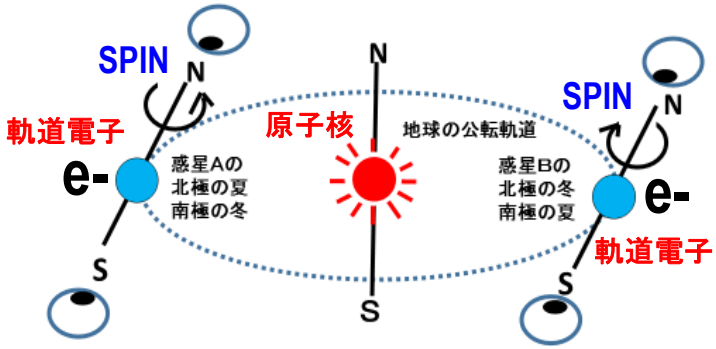


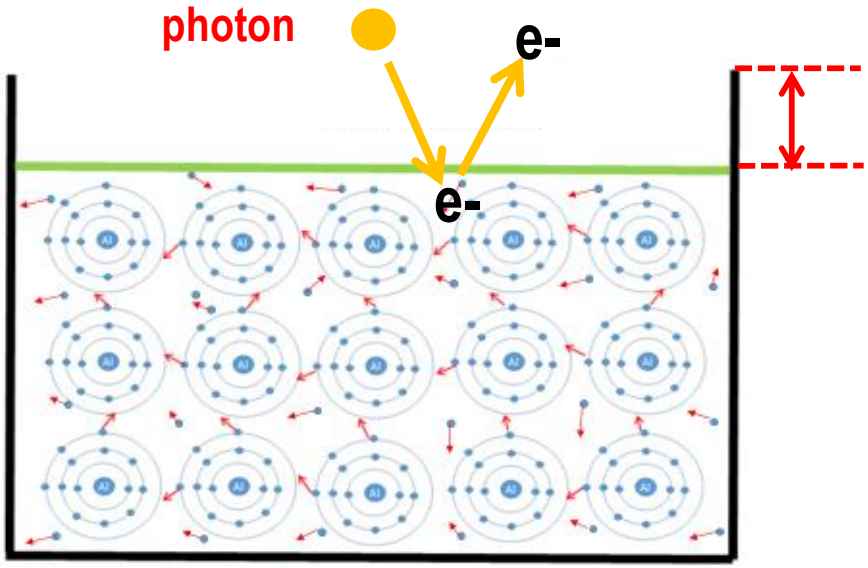
TSV=through Silicon Via



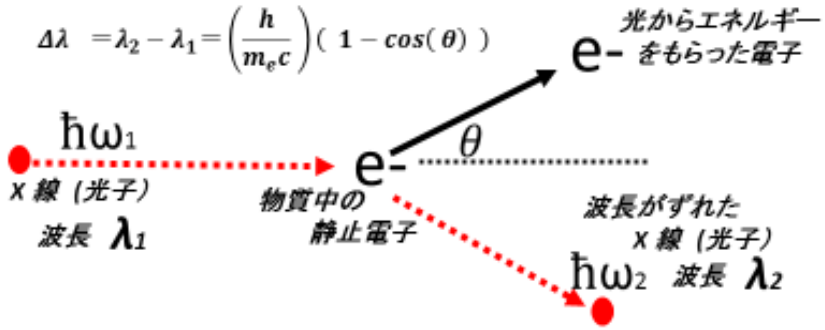
Prof. James McCaldin

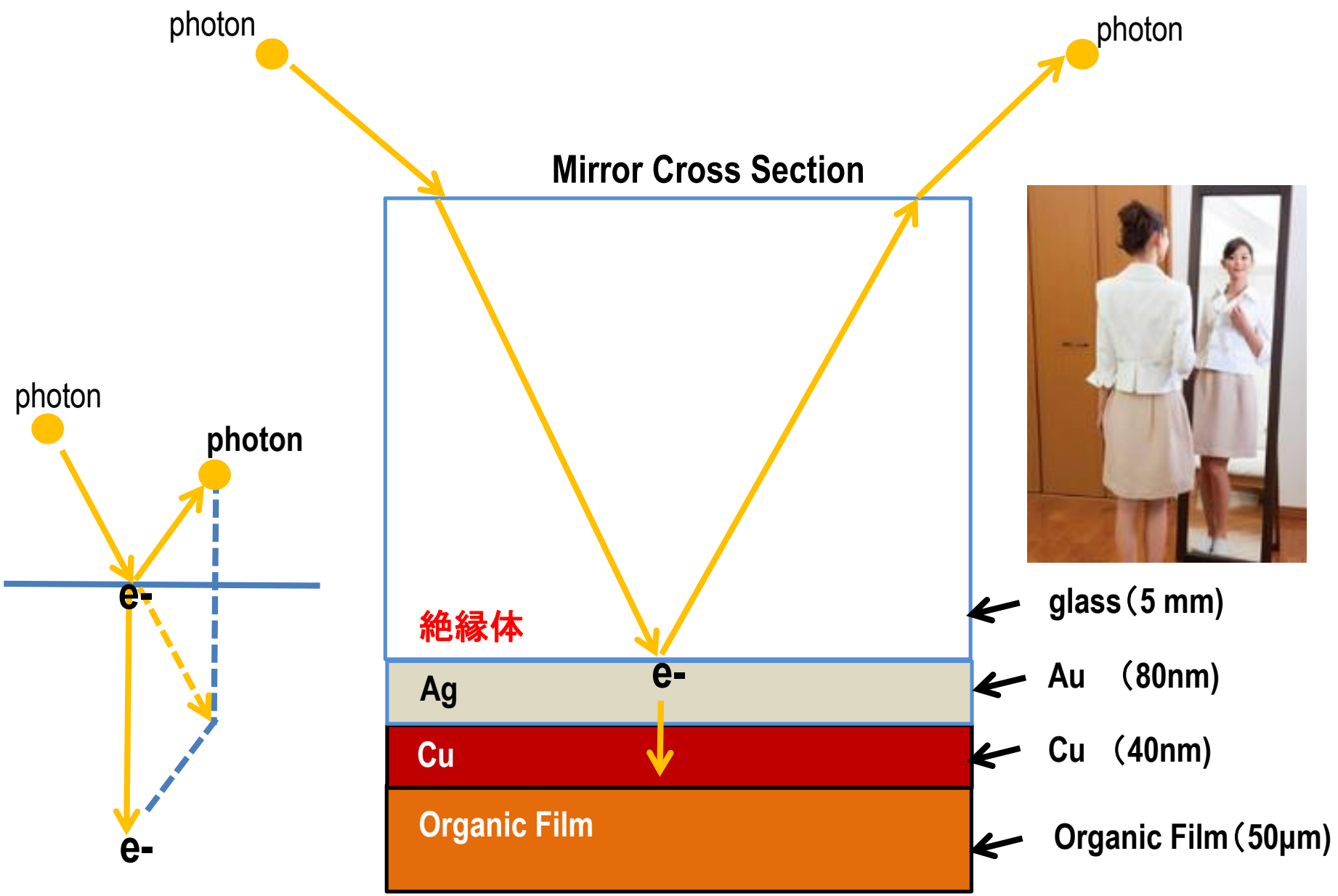


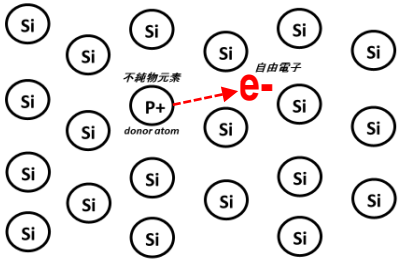


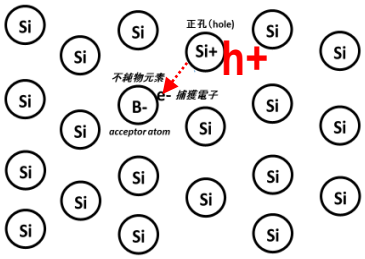


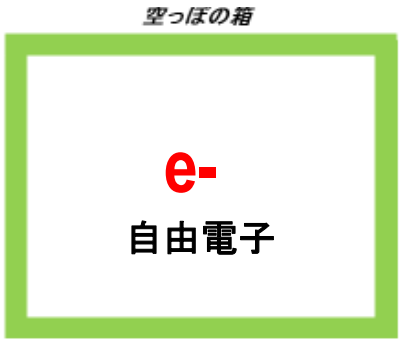
$$\Delta\lambda = \lambda_2 - \lambda_1 = \left(\frac{h}{m_e c}\right)(1 - \cos(\theta))$$

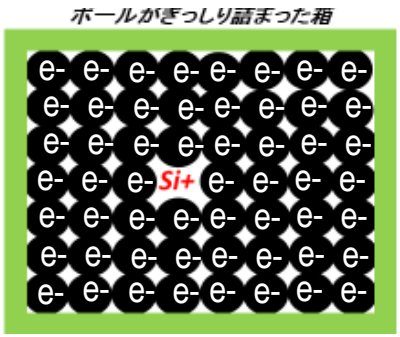


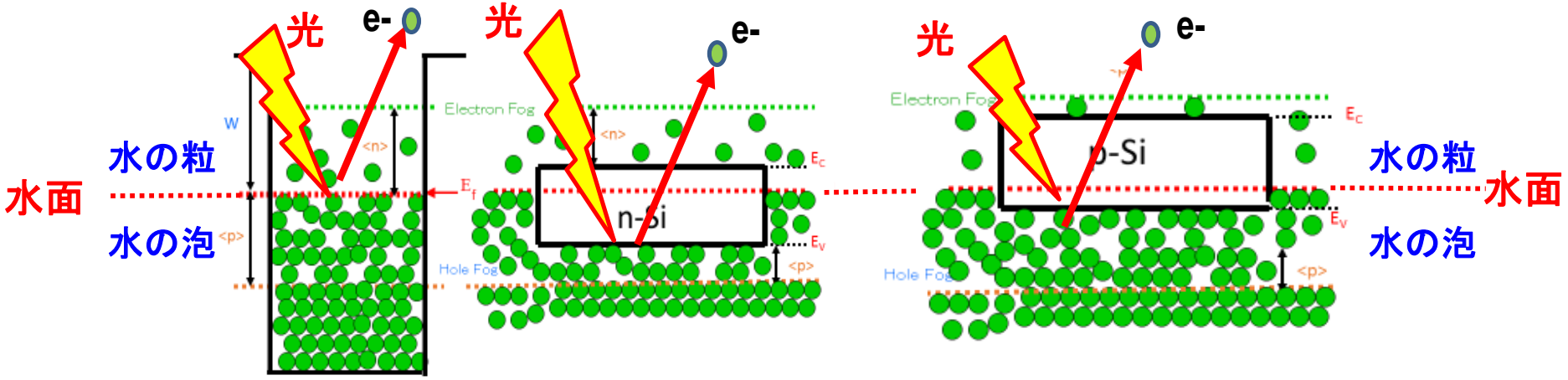

photon
photon
Mirror Cross Section
photon
photon
e-
e-
絶縁体
e-
Ag
Cu
Organic Film
glass（5 mm)
Au （80nm)
Cu （40nm)
Organic Film（50μm)


Si
不純物元素
P+
donor atom
自由電子
e-

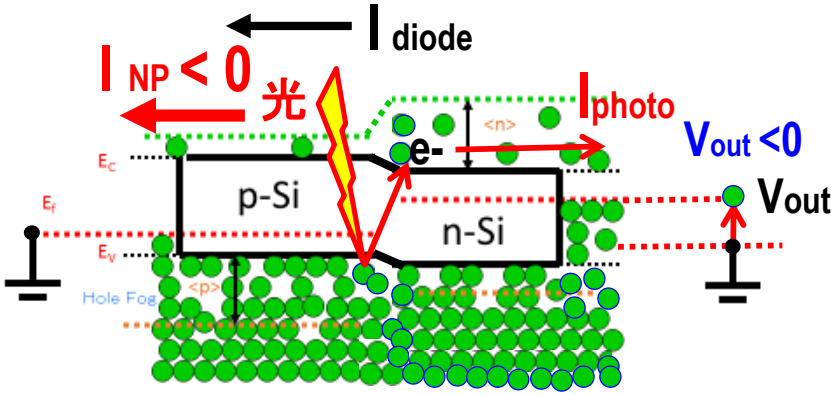

Si
正孔(hole)
Si+
h+
不純物元素
B-
acceptor atom
捕獲電子


空っぽの箱
e-
自由電子

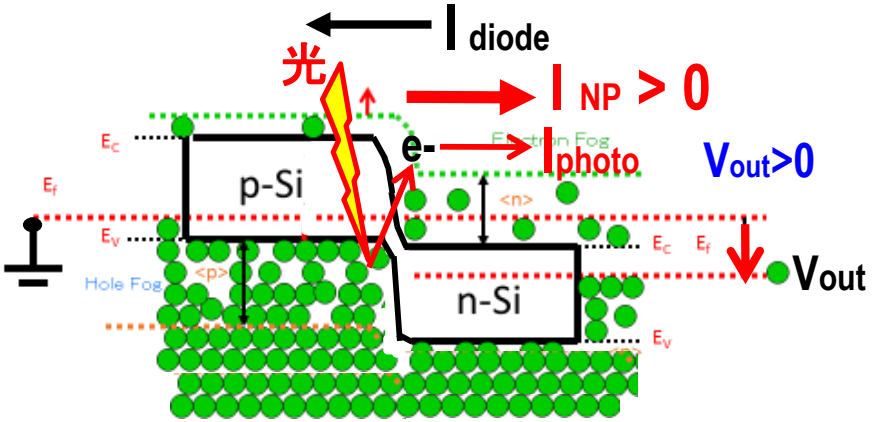

ホールがぎっしり詰まった箱
e-
Si+


光
e-
水面
水の粒
水の泡
W
<n>
<p>
Electron Fog
Hole Fog
E_f
E_c
E_v
n-Si
p-Si

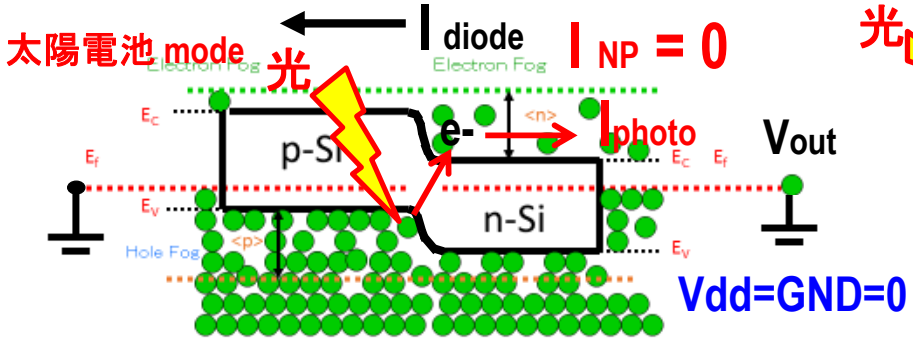
(1)電源電圧　Vdd<0 (順バイアス mode)　の場合

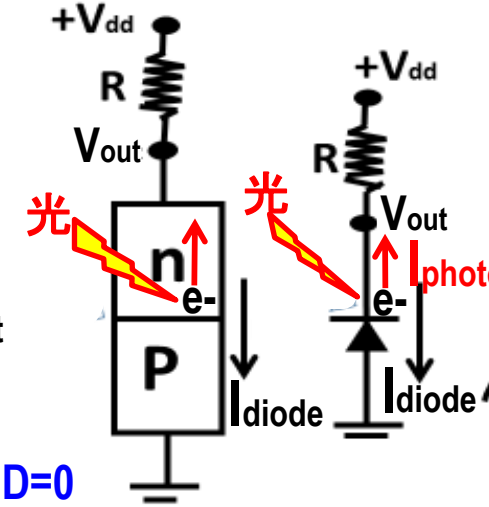


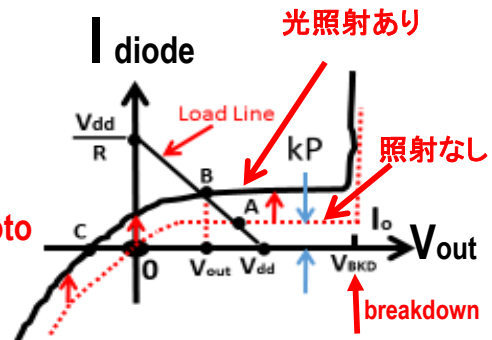
(3)電源電圧　Vdd>0 (逆バイアス mode)の場合



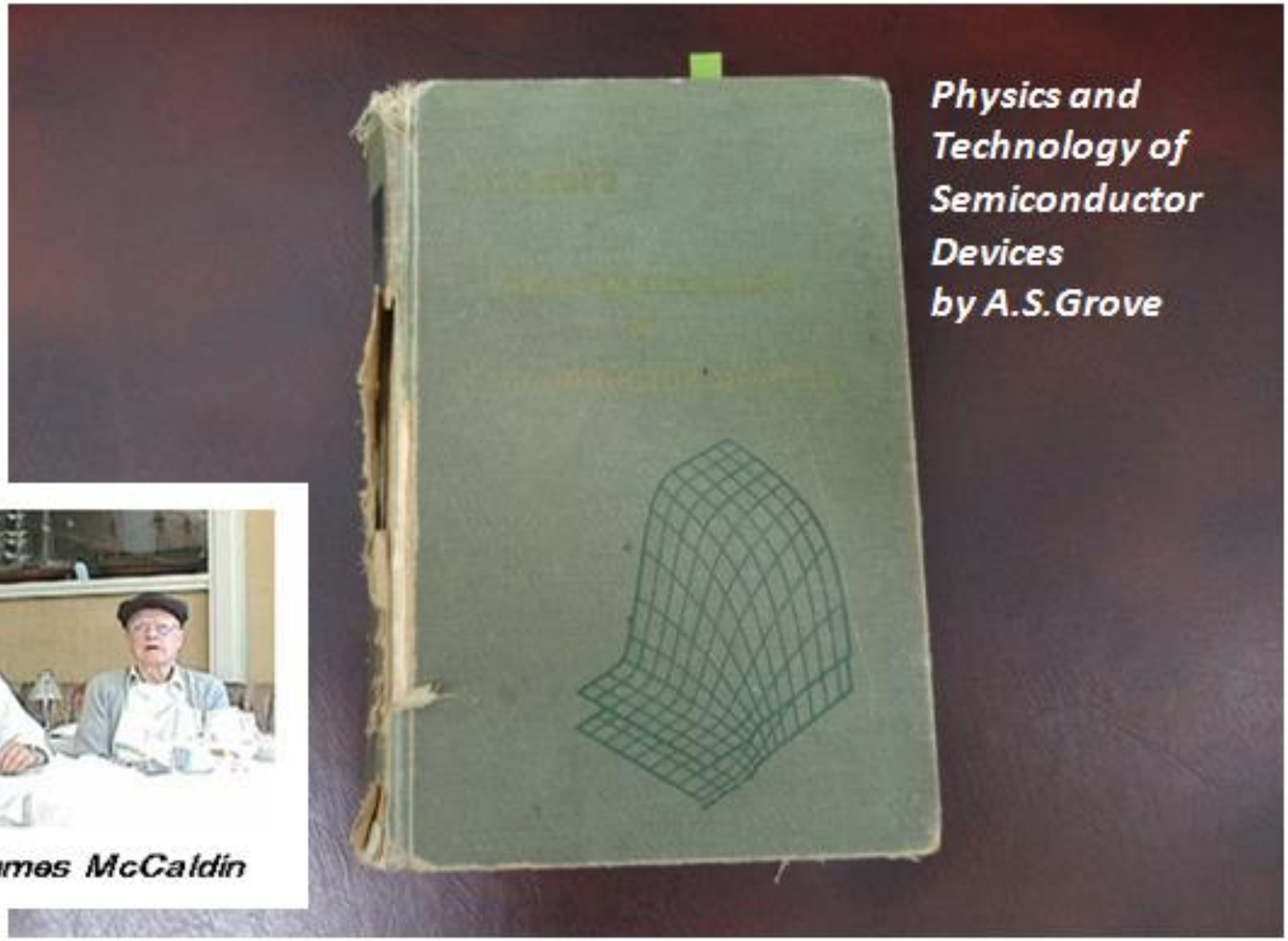
(2)電源電圧　Vdd=GND=0 (NOバイアス mode)の場合



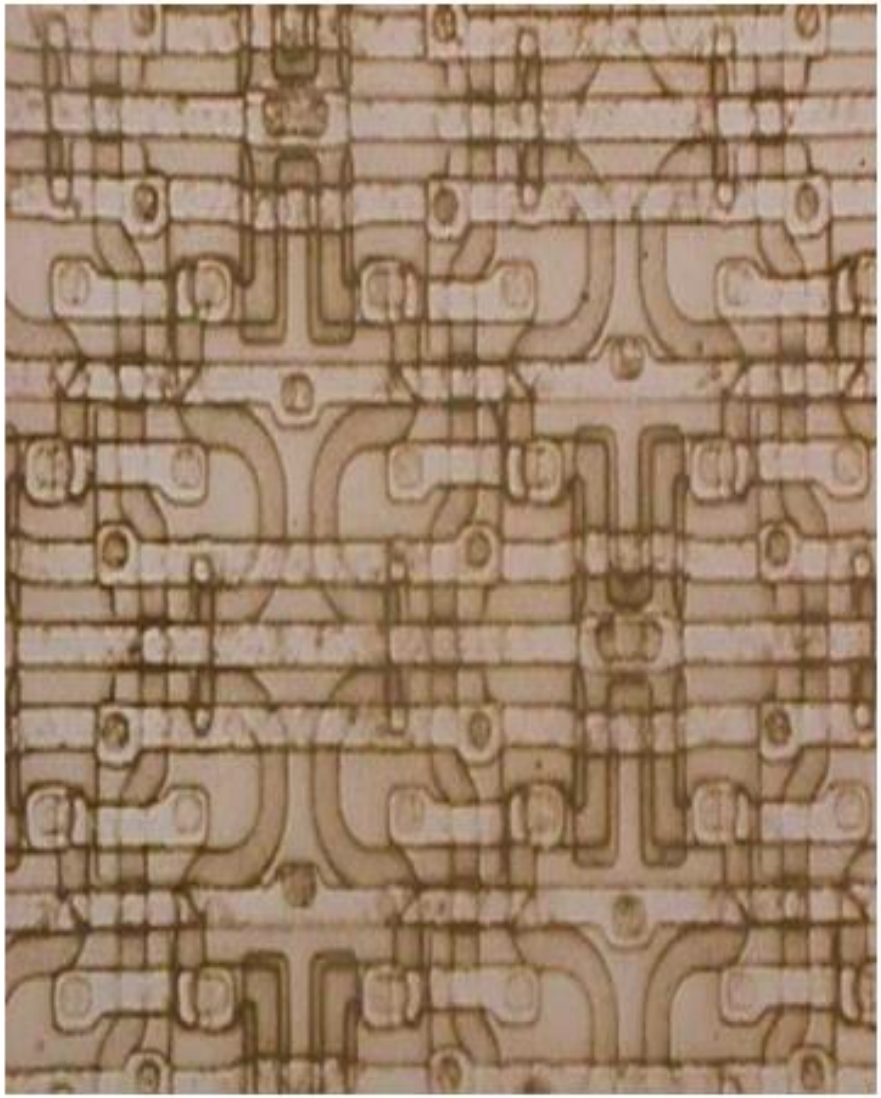


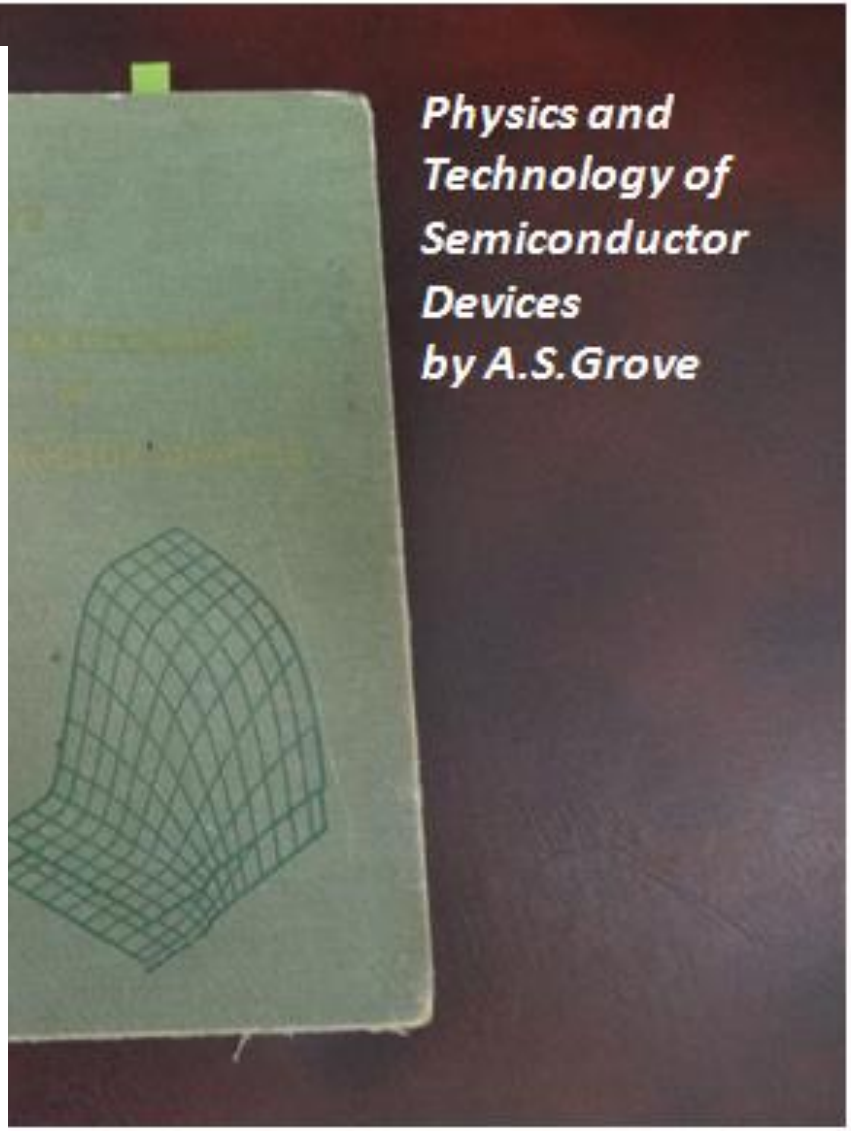


光を照射すると電流が流れる！

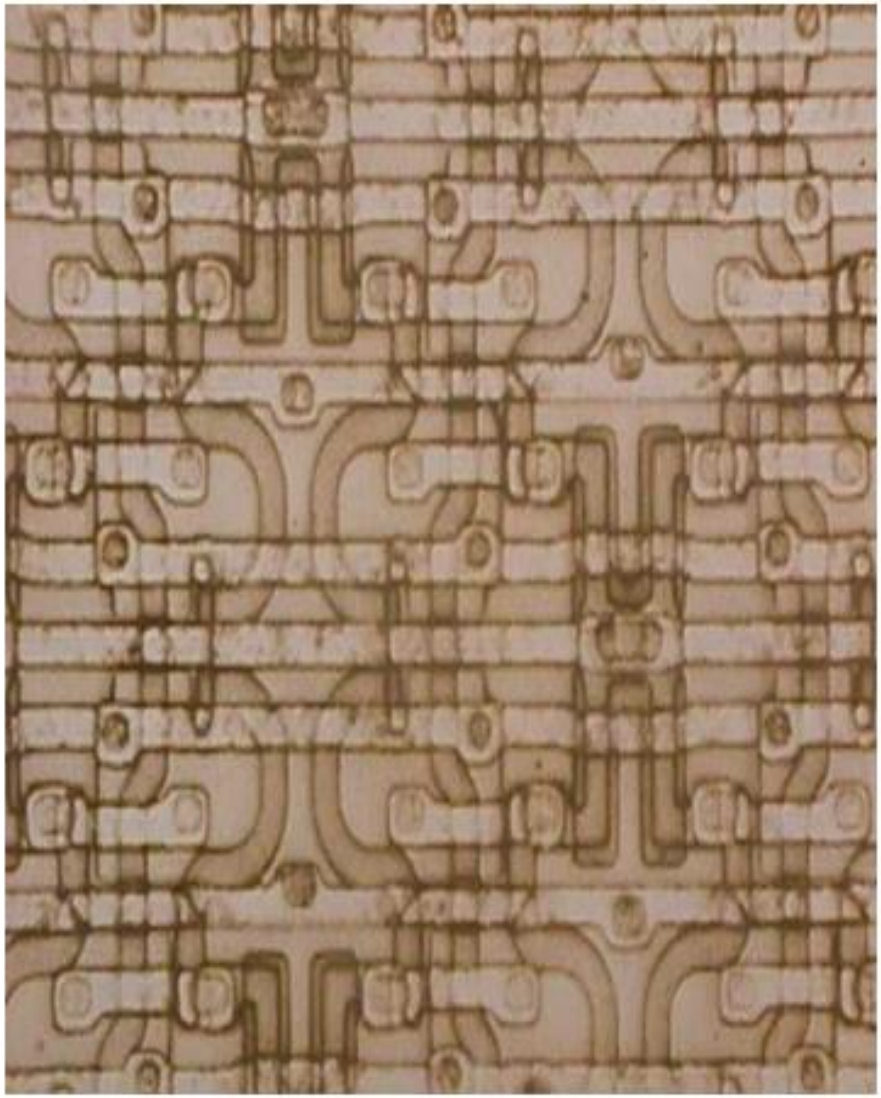


Prof. James McCaldin

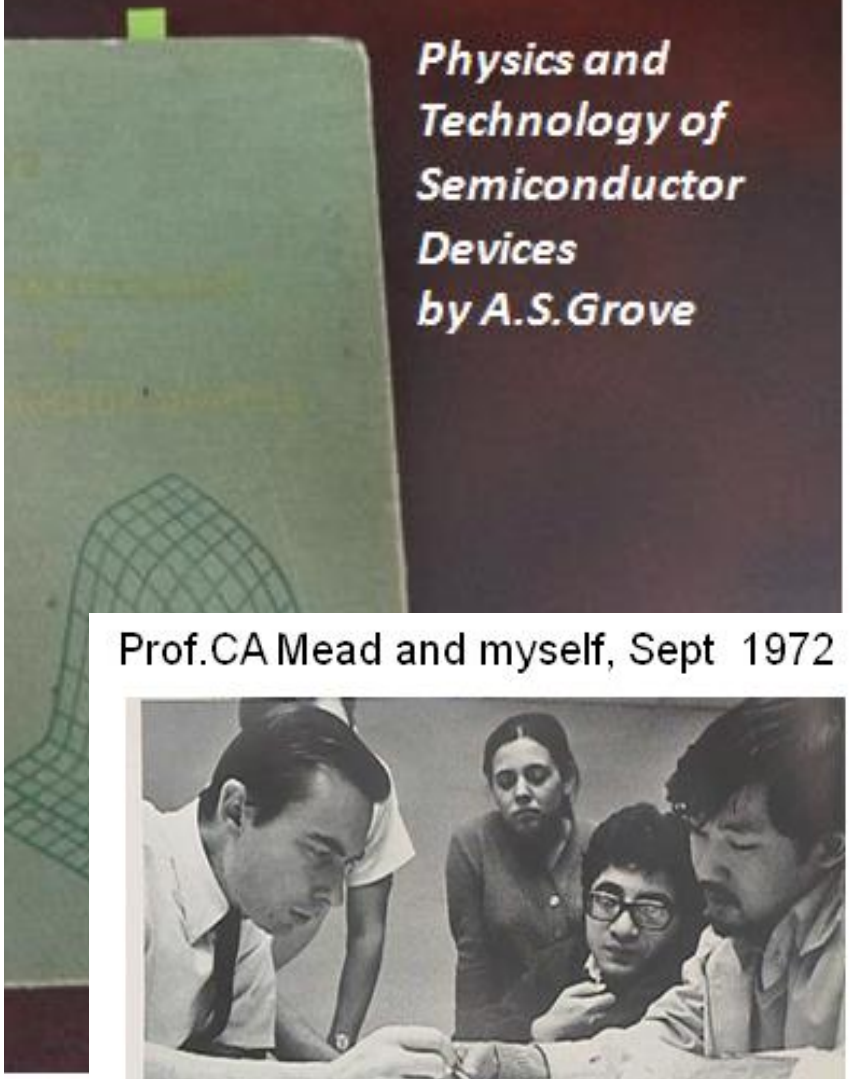




1971 Intel 1101 256bit RAM



1971 Intel 1101 256bit RAM



Prof.CA Mead and myself, Sept 1972

128 bit data comparator chip designed by CalTech and fabricated in Intel, 1972.

128-Bit Multicomparator

CARVER A. MEAD, RICHARD D. PASHLEY, MEMBER, IEEE, LEE D. BRITTON, YOSHIAKI T. DAIMON, AND STEWART F. SANDO, JR., MEMBER, IEEE

Abstract—A 128-bit multicomparator was designed to perform the search-sort function on arbitrary length data strings. Devices can be cascaded for longer block lengths or paralleled for bit-parallel, word-serial applications. The circuit utilizes a 3-phase static-dynamic shift register cell for data handling and a unique gated EXCLUSIVE-NOR circuit to accomplish the compare function. The compare operation is performed bit parallel between a "data" register and a "key" register with a third "mask" register containing DON'T CARE bits that disable the comparator. The multicomparator was fabricated using p-channel silicon-gate metal-oxide-semiconductor (MOS) technology on a 107 × 150 mil chip containing 3350 devices. With transistor-transistor logic (TTL) input, data rates in excess of 2 MHz have been attained. The average power dissipation was 250 mW in the dynamic mode and 300 mW in the static mode.

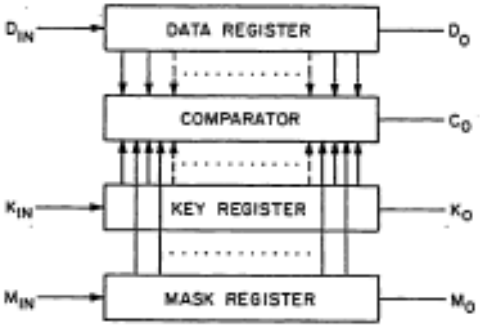
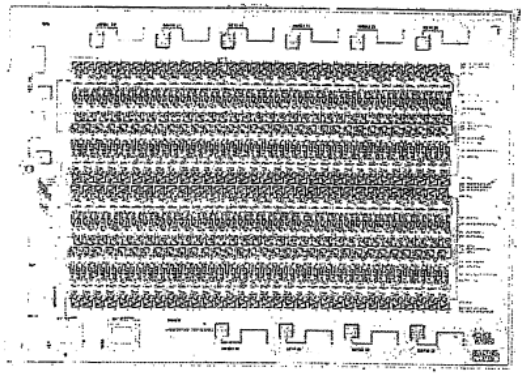
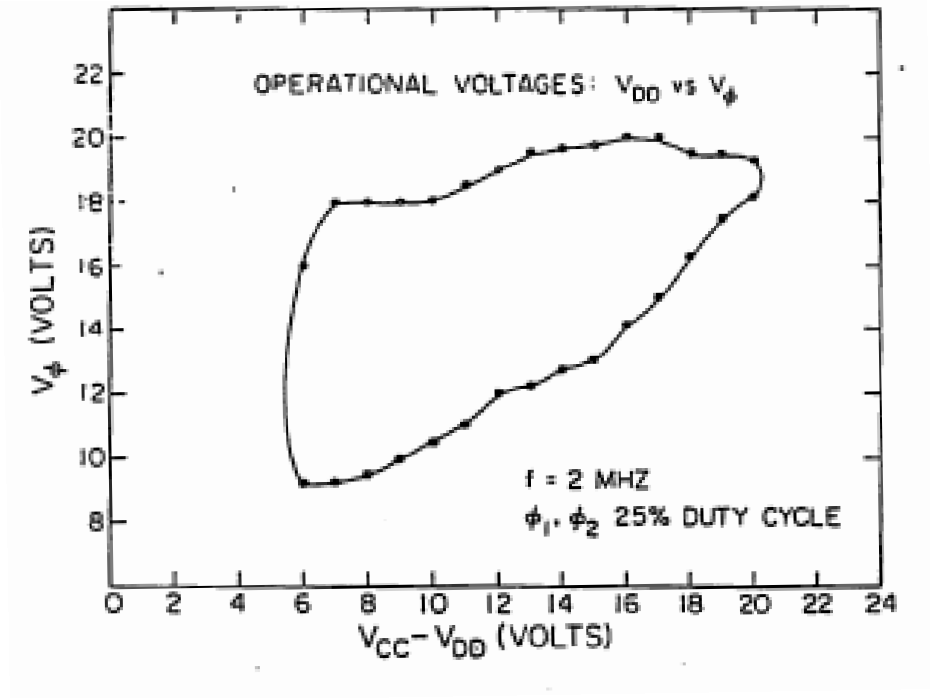
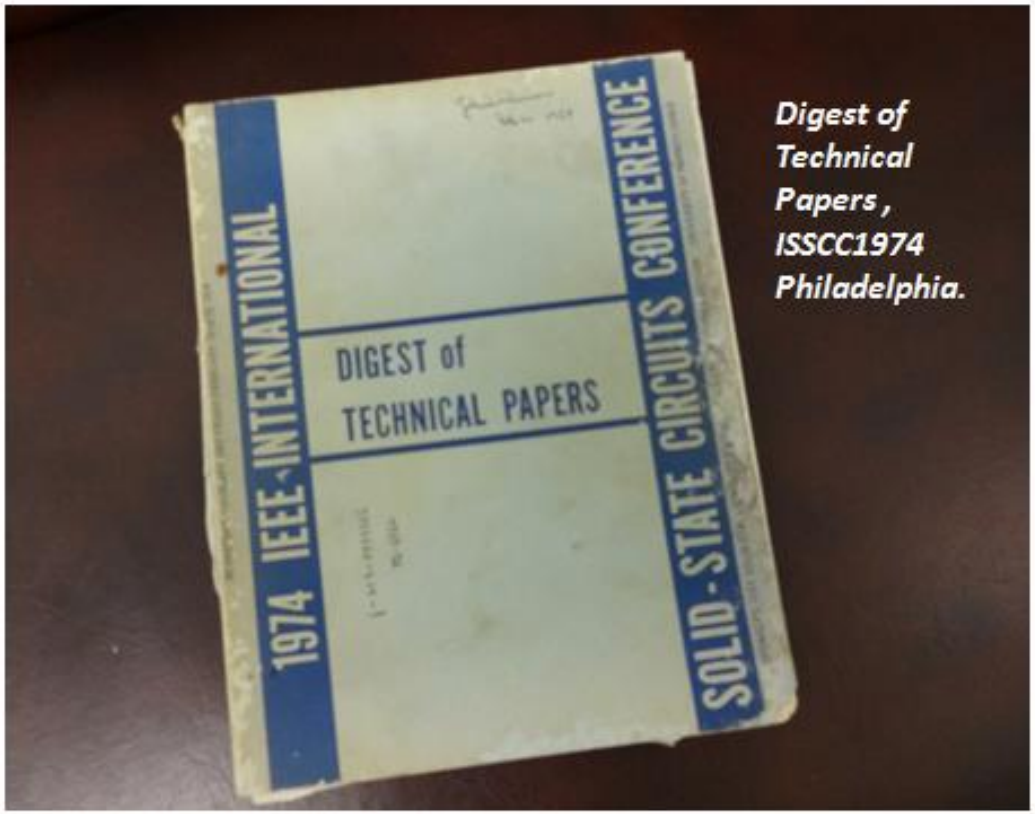


Fig. 1. Block diagram of multicomparator.





Prof.CA Mead and myself, Sept 1972



Digest of Technical Papers, ISSCC1974 Philadelphia.

Charge-Coupled Devices and Applications

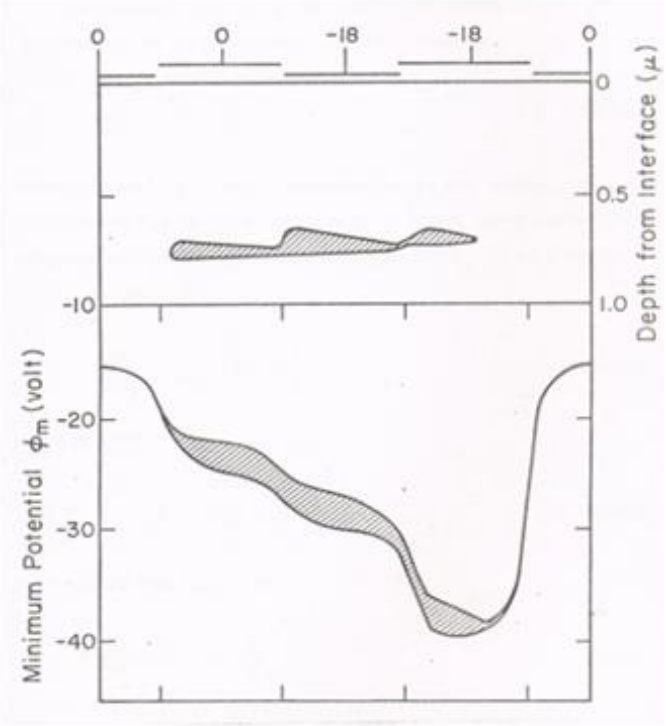
Chairman

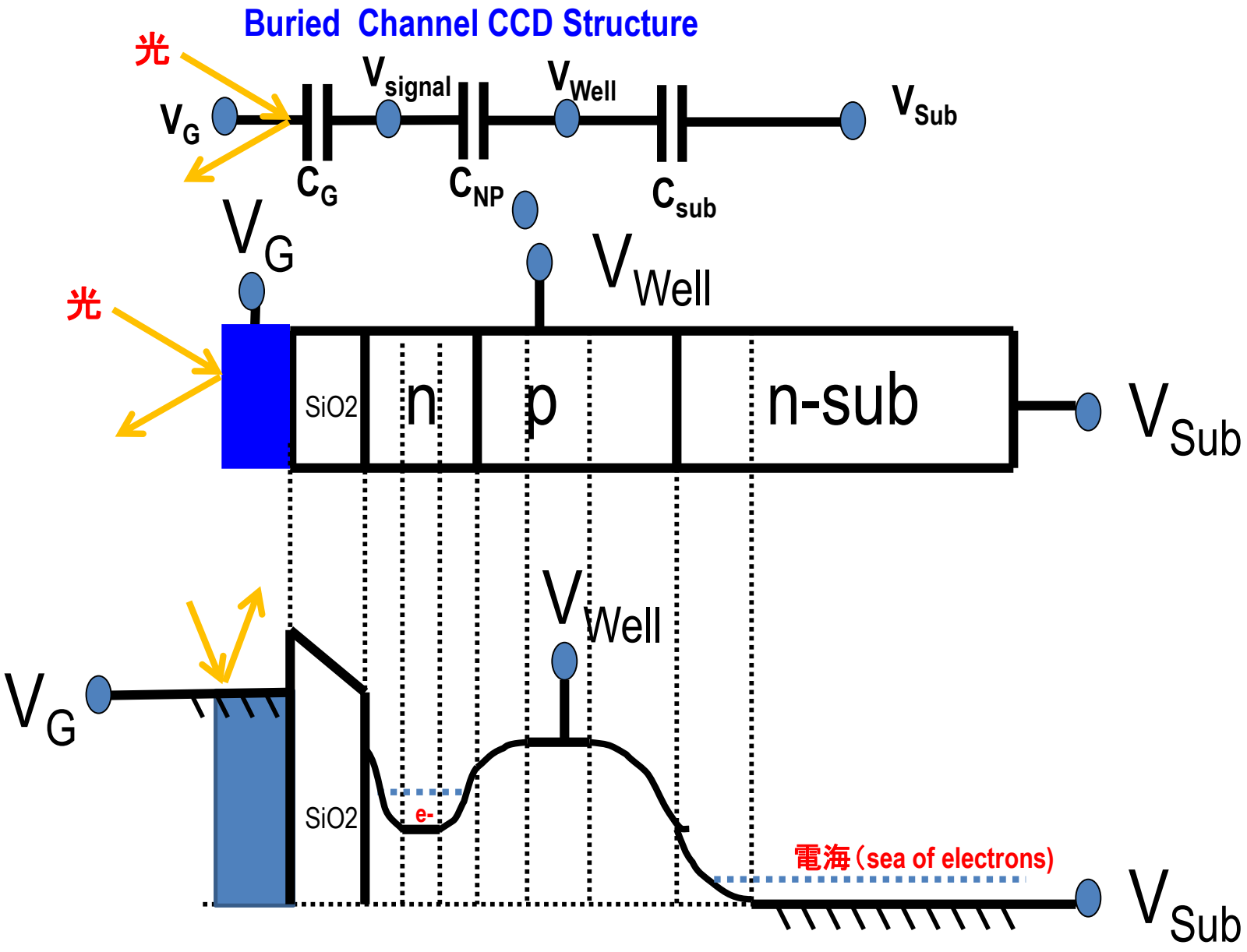
Lewis M. Terman

Testimonial to the importance of the charge-transfer phenomenon is attested to by the Morris N. Liebmann and the David A. Sarnoff awards this year to the originators of the charge-coupled and bucket-brigade devices, respectively. The papers in this session concentrate on the former.

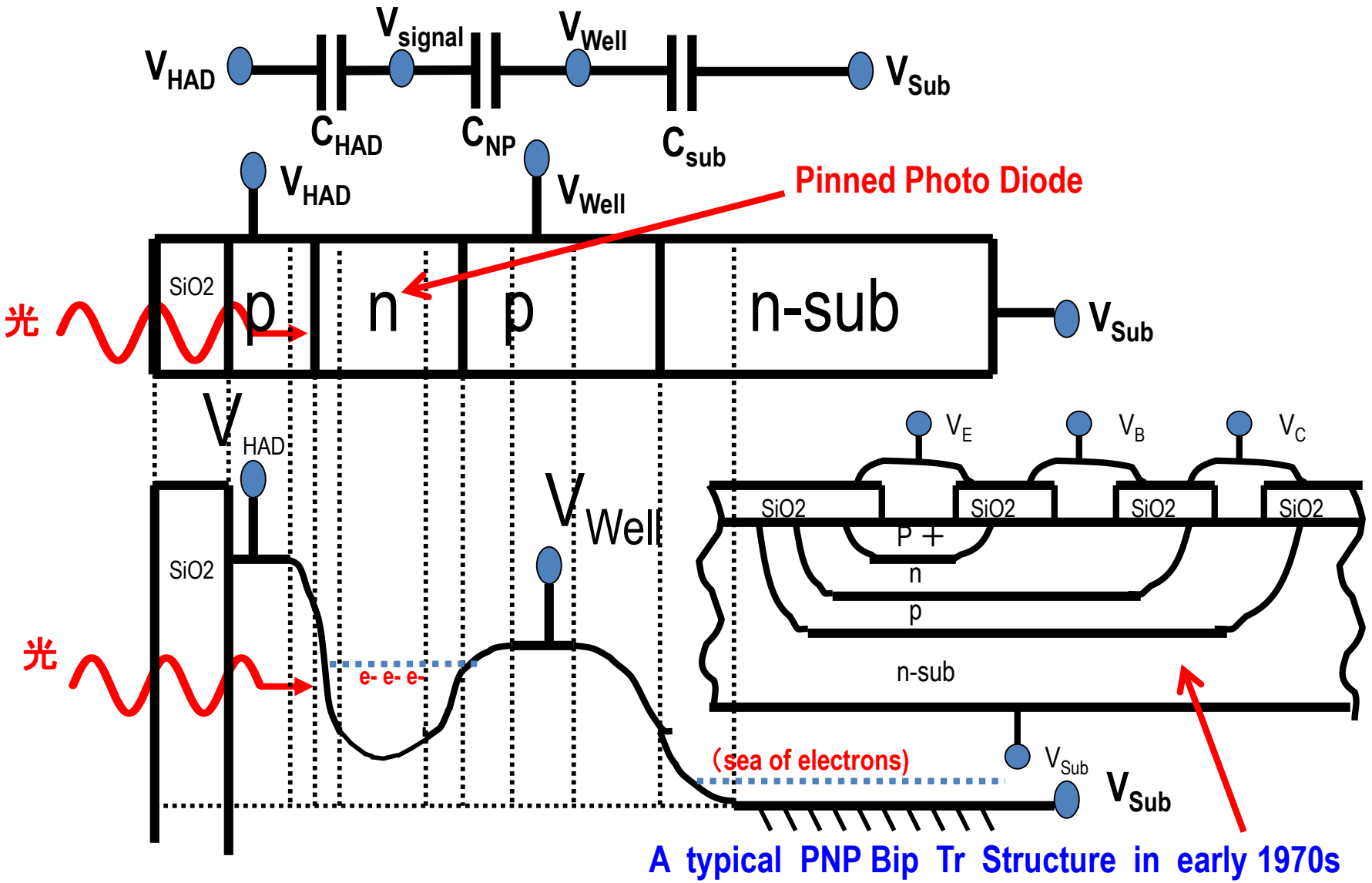
ISSCC1974 PhD Student Paper on buried channel CCD

Prof. T. C. McGill

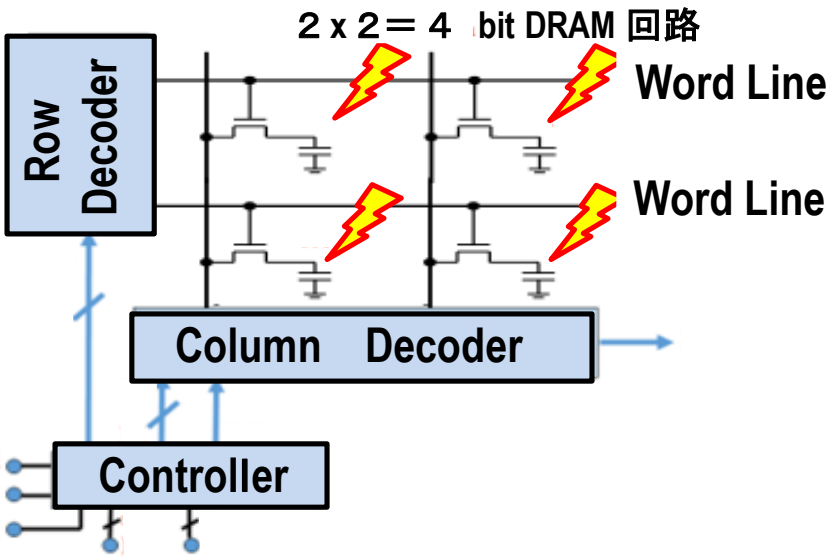


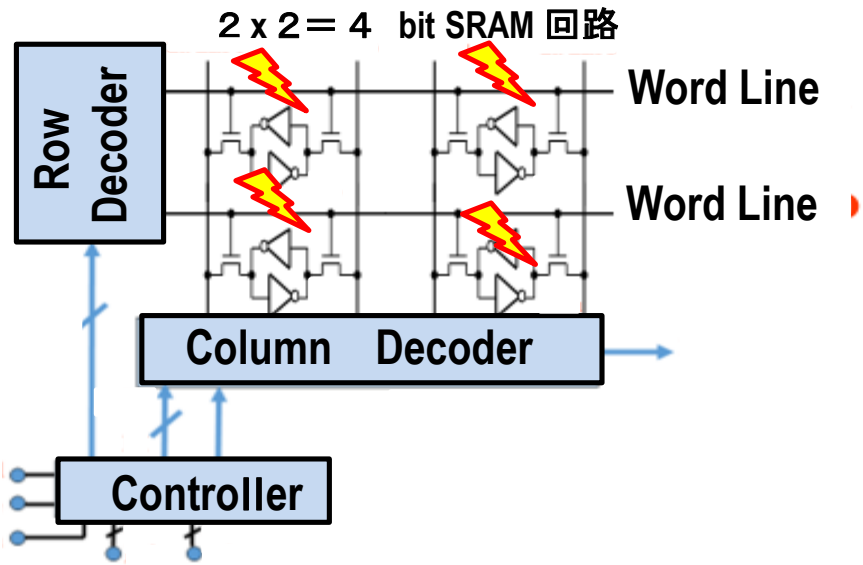

Buried Channel CCD Structure
光
V_G
V_signal
V_Well
V_Sub
C_G
C_NP
C_sub
V_G
V_Well
光
SiO2
n
p
n-sub
V_Sub
V_Well
V_G
SiO2
e-
電海（sea of electrons）
V_Sub

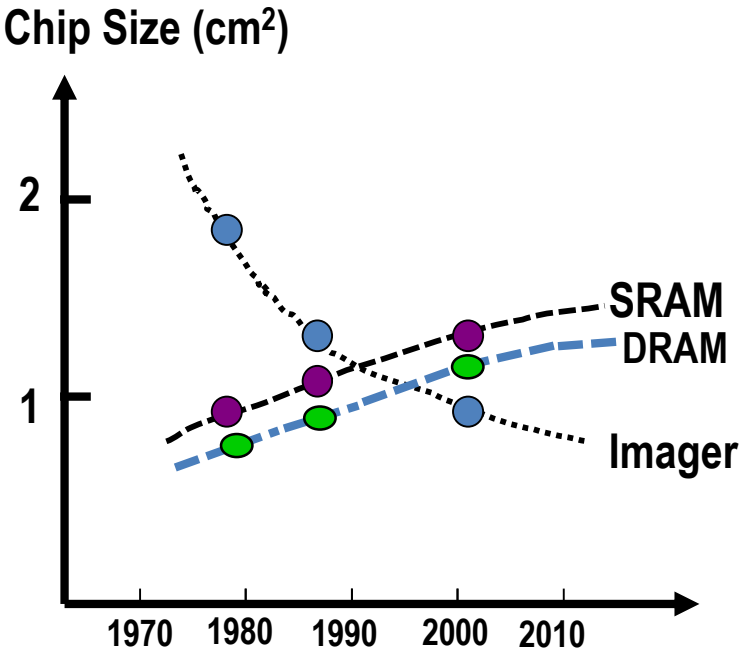
HAD (hole accumulated diode) sensor

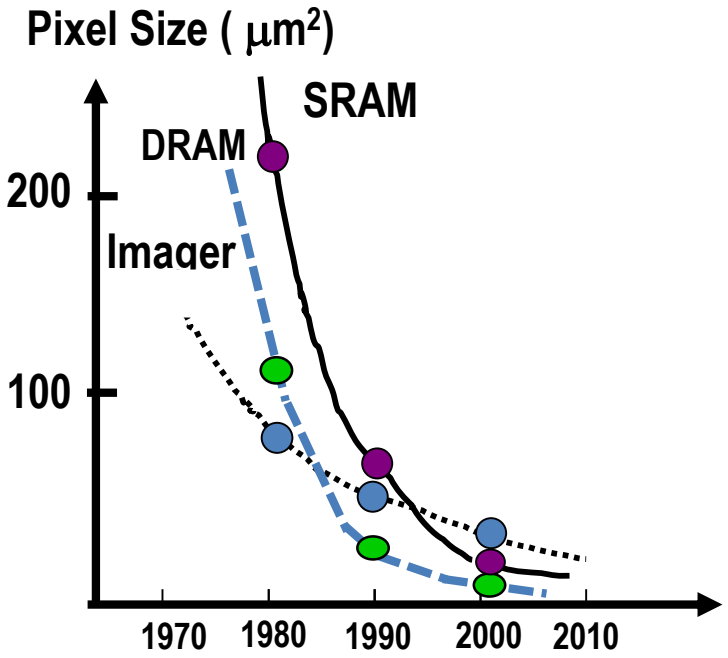


A typical PNP Bip Tr Structure in early 1970s

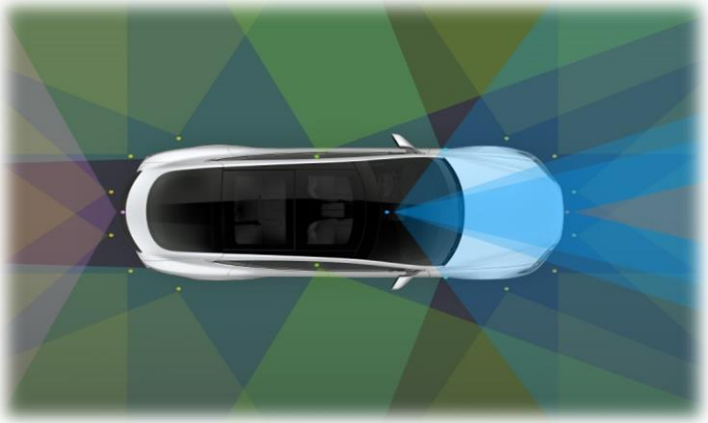

2 x 2＝ 4 bit DRAM 回路
Row Decoder
Word Line
Word Line
Column Decoder
Controller


2 x 2＝ 4 bit SRAM 回路
Row Decoder
Word Line
Word Line
Column Decoder
Controller

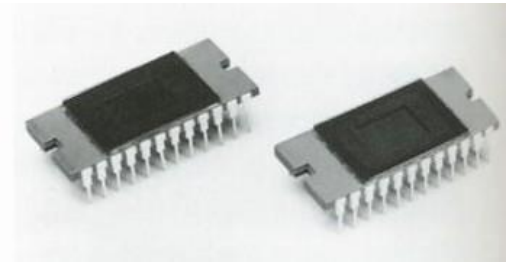

Chip Size (cm²)
2
1
SRAM
DRAM
Imager
1970
1980
1990
2000
2010


Pixel Size (μm²)
SRAM
DRAM
200
Imager
100
1970
1980
1990
2000
2010

XC-1 1980
Two-Chip Color Video Camera



<ICX008>
2/3 Inch 120K Pixcel IT CCD Imager designed



1975-1982 Engineer in CCD Imagers and Camera System
1983-1989 Engineering Manager in SRAM/DRAM/ADC
1990-1998 General manager in Sony /NVM/MCU/PS1
1998-2008 Executive Staff Sony Semiconductor
Strategic Planning PS2/PS3

IEEE Computer Elemets Workshop @ Vail, Colorado, 1995

Mitsuo Saito（Toshiba）

Bob Guensey（IBM）

Ken Kutaragi

Yoshiiaki Hagihara

モンスター級の処理能力を発揮

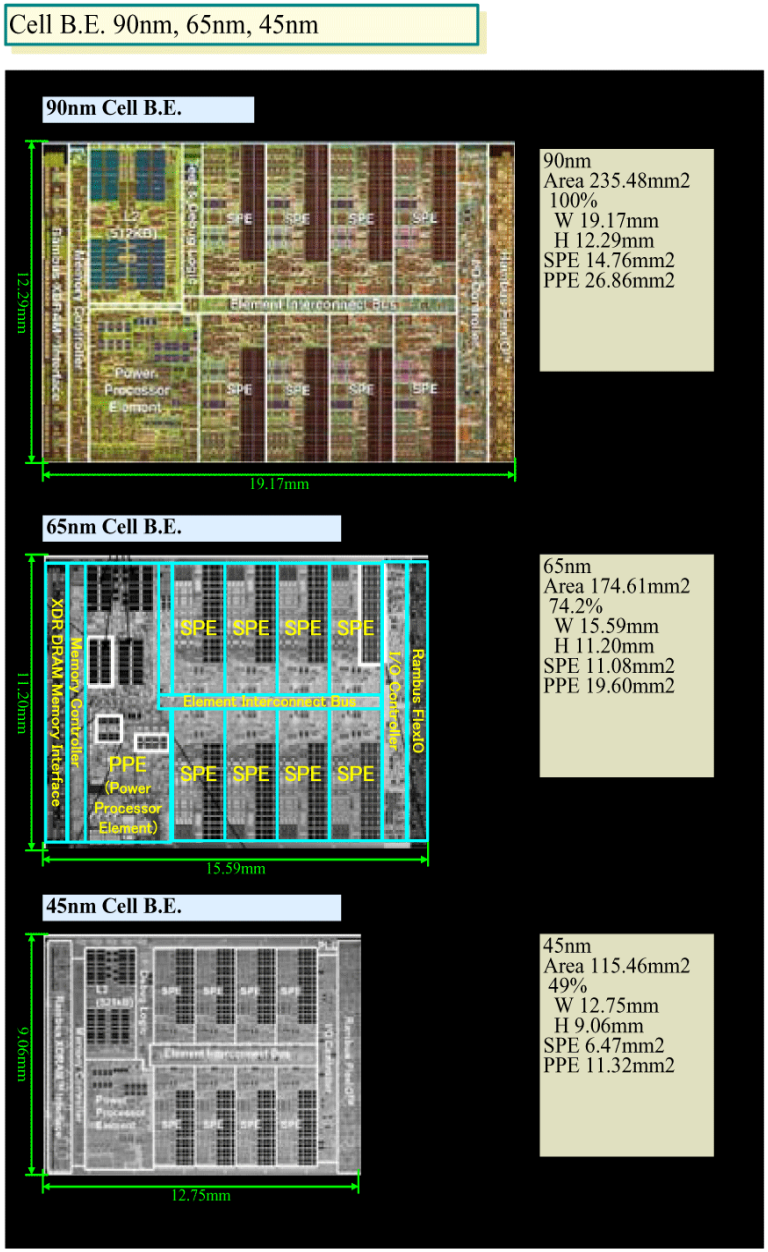
「CELLプラットフォーム」

PS3 の Cell Processor の 微細化によるハードウエアーのコスト低減効果と初期投資の回収:

この電子部品の中身Hardwareを調査研究: Computer の構造とそのアーキテクチャーを学習。

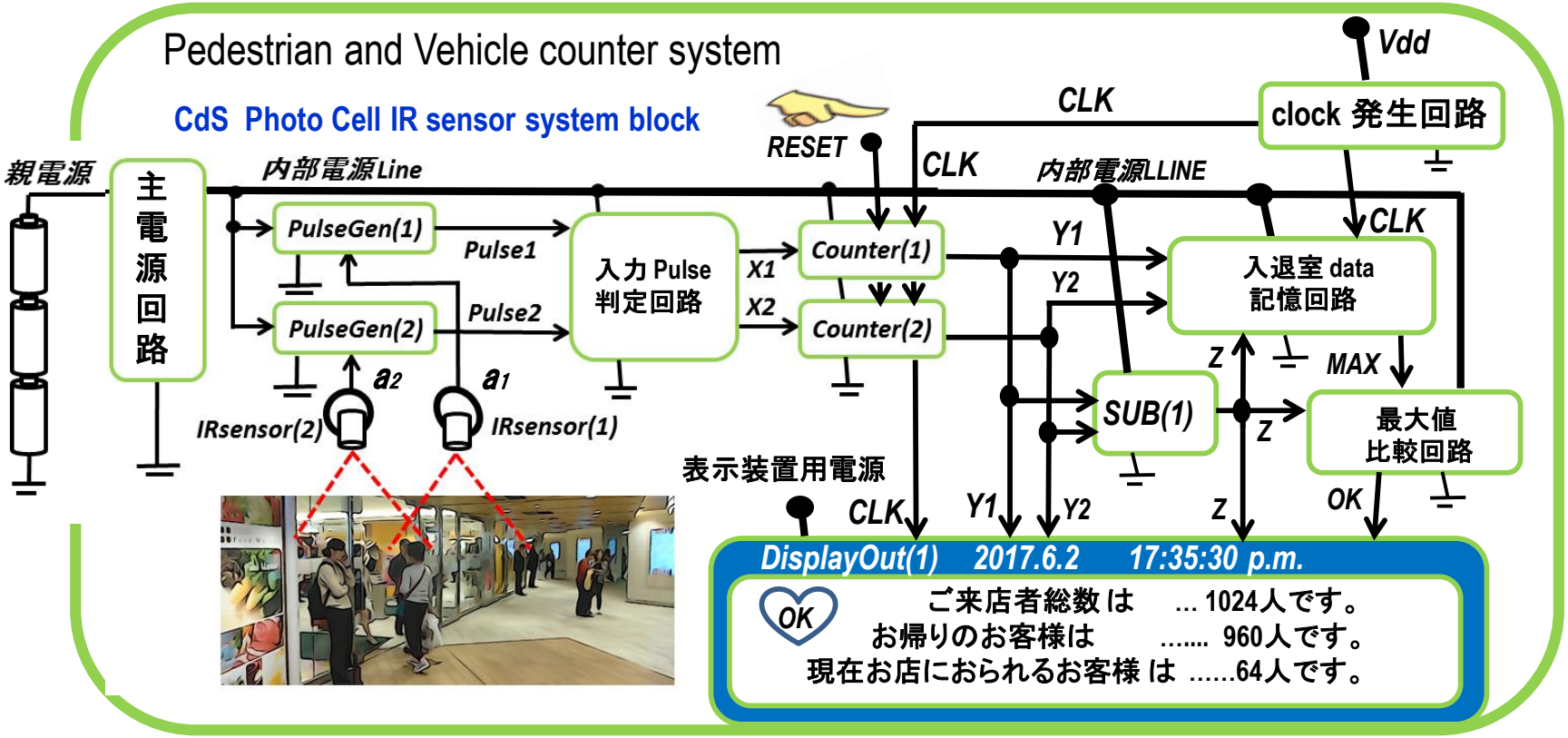
比較対象: 2005年モデルPS3

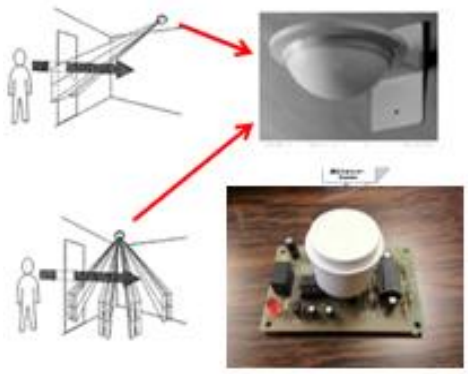
問題点と改良点についてまとめる。

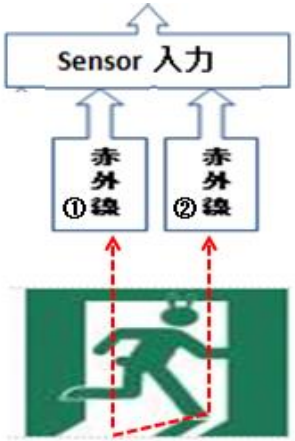


Pedestrian and Vehicle counter system

CdS Photo Cell IR sensor system block

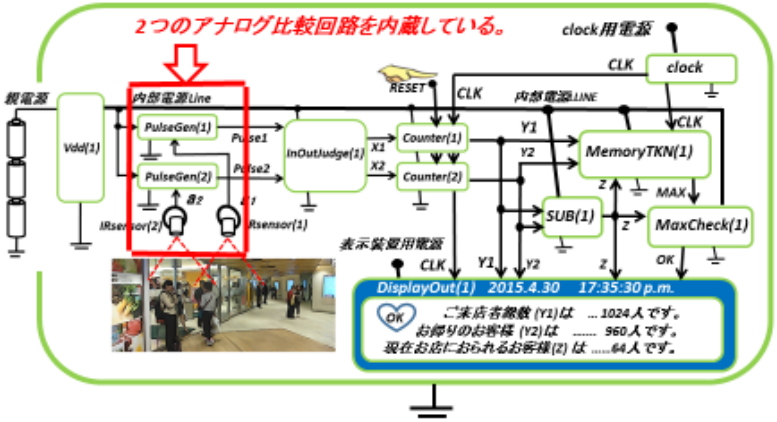




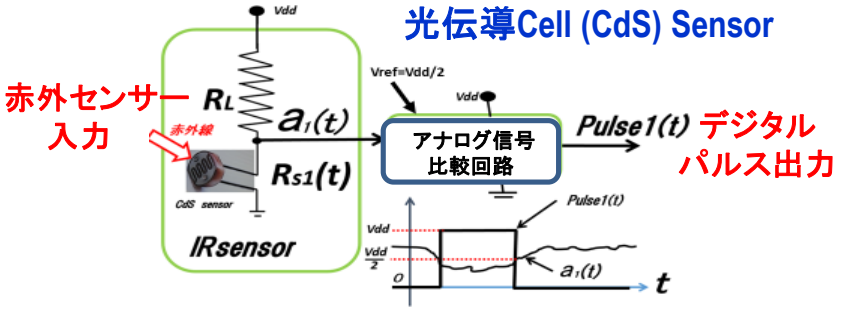


街中での通行人の映像

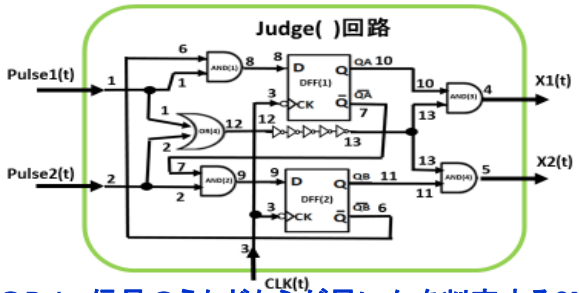
光伝導Cell (CdS) Sensor　System 例



光伝導Cell (CdS) Sensor

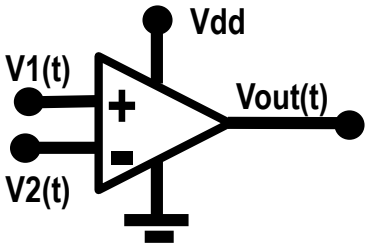


相対Pulse遅延判定回路

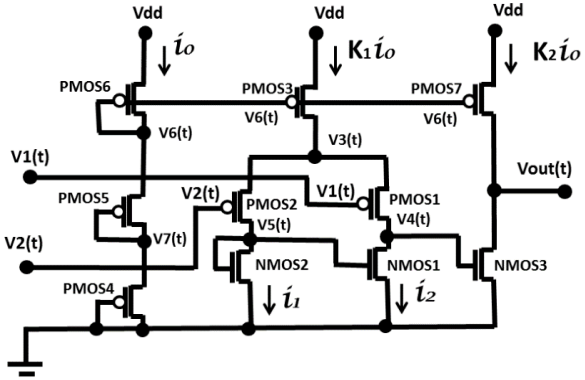


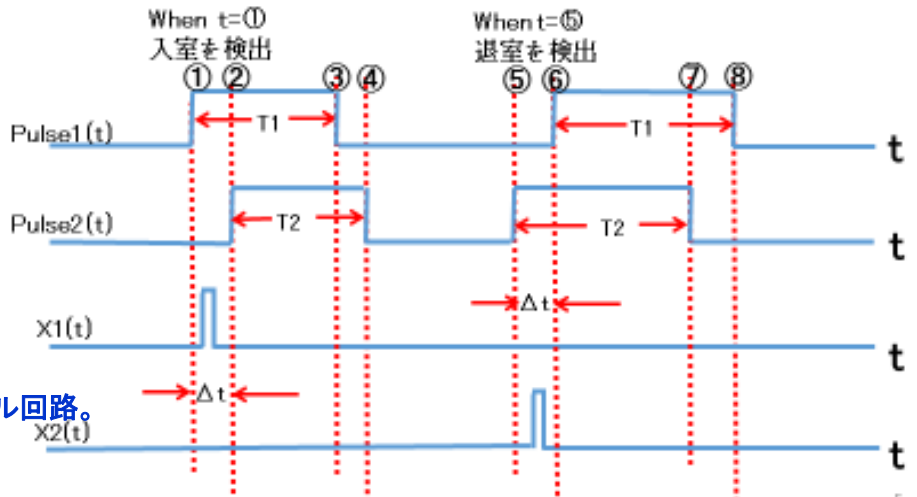
2つのPulse信号のうちどちらが早いかを判定するCMOSデジタル回路。

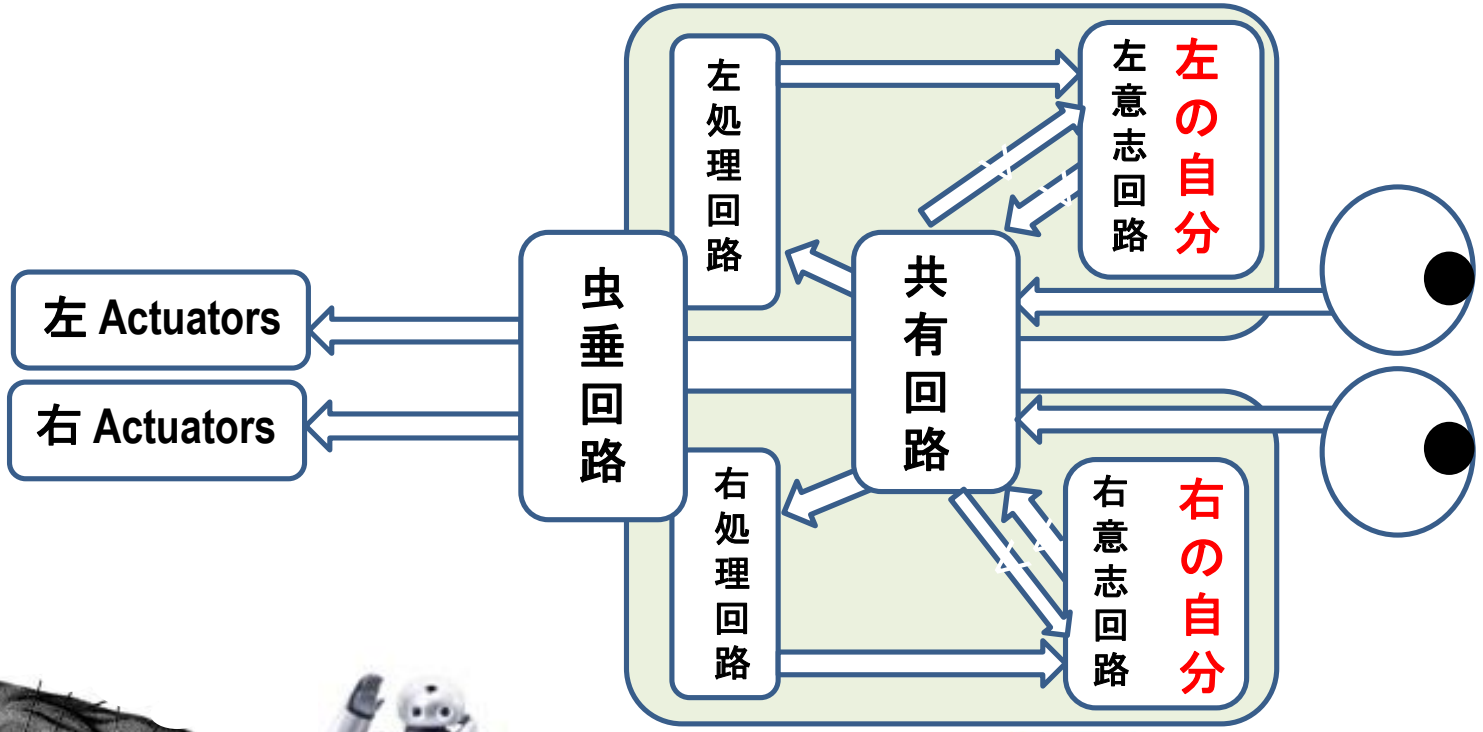
アナログ信号比較回路 （単純な1 bit の　A/D変換器）

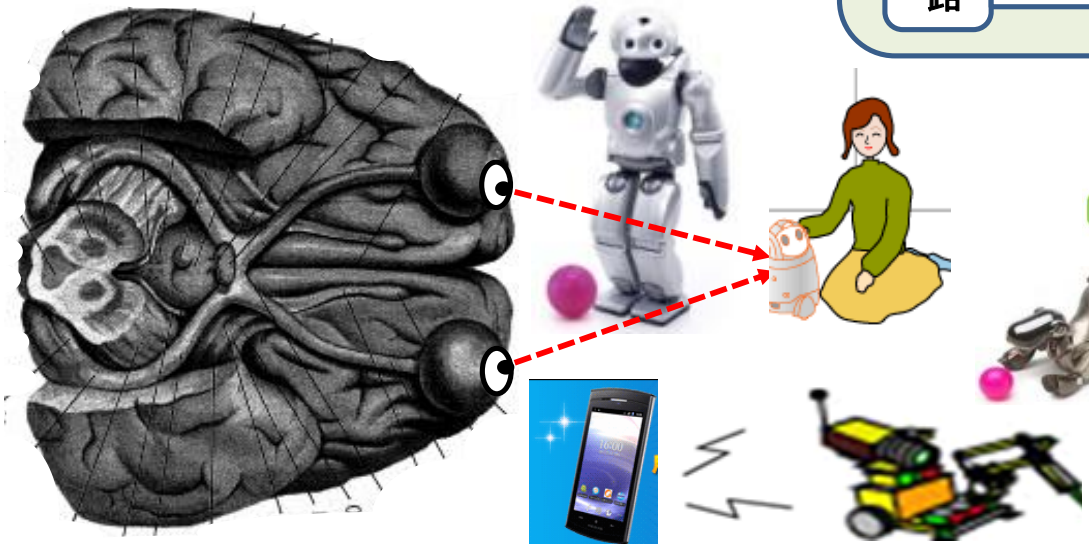


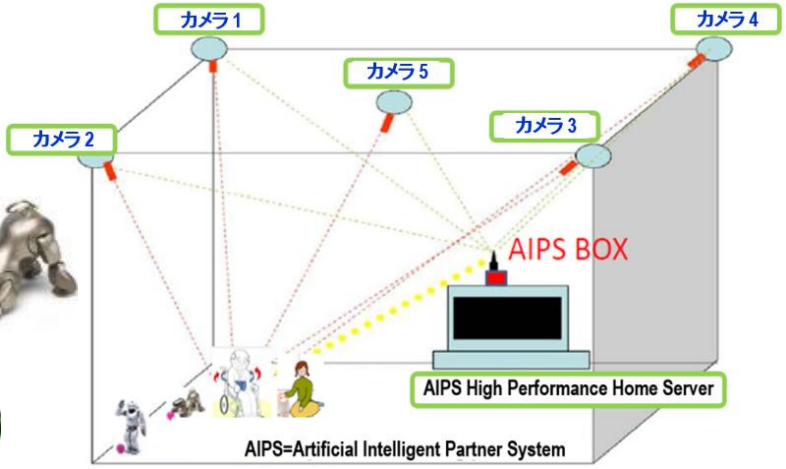
CMOS回路で構成されたアナログ信号比較回路



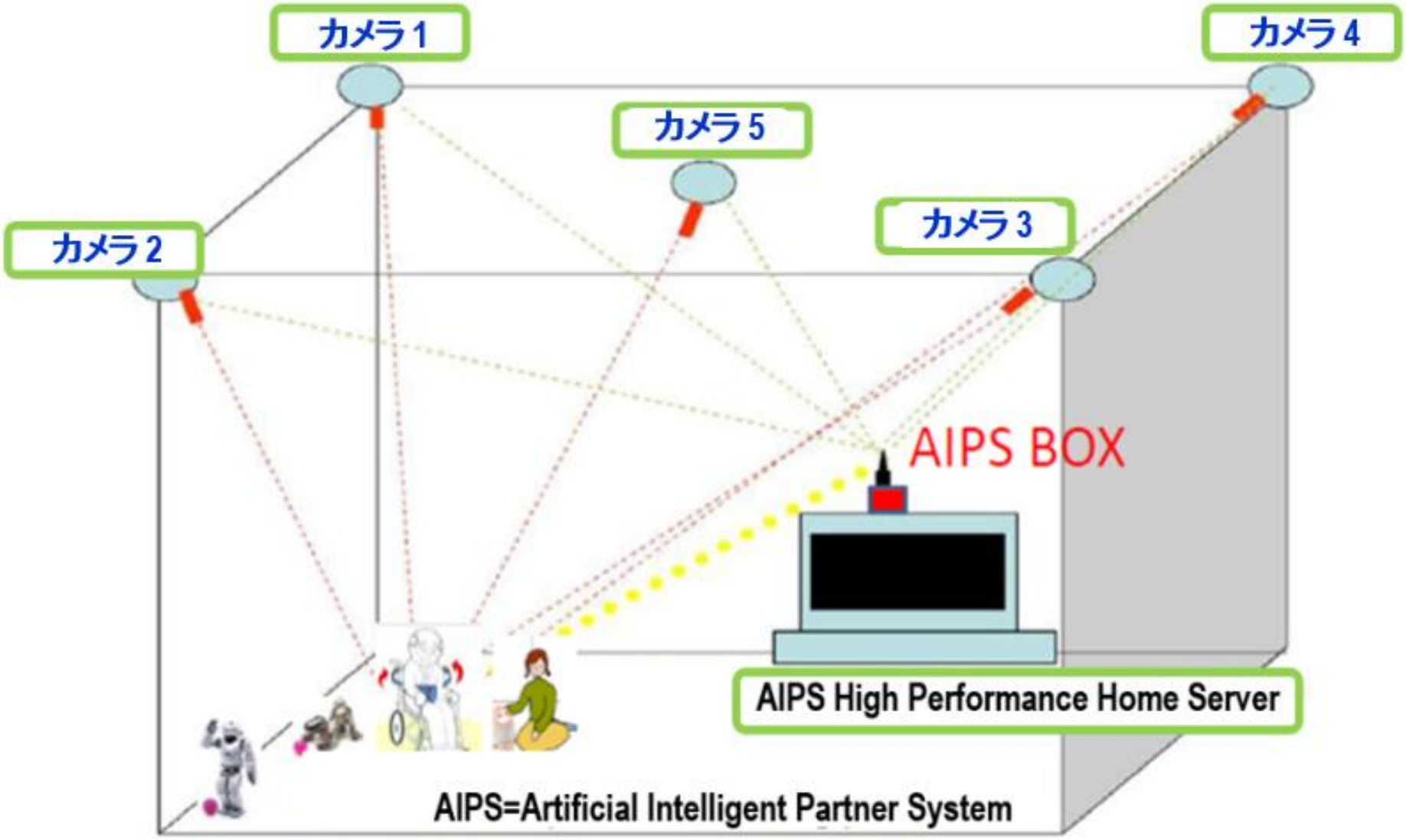








see http://www.aiplab.com /


カメラ1
カメラ4
カメラ5
カメラ3
カメラ2
AIPS BOX
AIPS High Performance Home Server
AIPS=Artificial Intelligent Partner System

2013年3月25日　午後4時
フジテレビ全国NETで放送