The details of explanations are given below regarding the 1975 invention of the First Pinned Photodiode proposed by Yoshiaki Hagiwara at Sony in 1975.

In his 1975 Japanese patents Hagiwara proposed a double junction and a triple junction type photodiodes with the pinned silicon surface hole accumulation region with the excellent short wave blue light sensitivity and also the complete charge transfer capability resulting in the no-image-lag high performance photodiode.

As Prof. Albert Theuwissen wrote in his IEDM2005 paper, the structure that Hagiwara proposed in 1975, that Hagiwara developed in 1978 and that Hagiwara reported in the SSDM1978 conference can be considered as the “mother” of of NEC Buried Photodiode, KODAK Pinned Photodiode and Sony Hole accumulation Diode.


But in the case that parts of the depleted n-type CCD channels are not covered by gate material, their surface potential is undefined! Such a structure will suffer from charge transport issues during operation, because charge can be trapped in local potential pockets. The effect can be solved by defining the potential in the open areas through an extension of the p’ channel stopper. A simple self-aligned implant of 2x10^{11}/cm^2 boron ions is sufficient to extend the channel stop areas to the gate edge and consequently fix the potential in the open areas [2]. The result after this self-aligned implant is shown in Figure 3. The presence of enough holes plays a crucial role in fixing the potential for the regions “beyond control” of the gates. (Is this structure the mother of the pinned-photodiode or buried diode or hole-accumulation device?)

At that time Prof. Albert Theuwissen did not know the details of Hagiwara's 1975 Japanese patents, yet.

Hagiwara did not explain in the past till 2019 his 1975 PPD inventions in details to the English speaking community.

The Hagiwara 1975 Japanese patents, proposing the Buried Pinned Hole Accumulation Photodiode, had never been exposed in details in the English speaking community until in September, 2019.

Hagiwara published a paper in the 3DIC2019 Conference sponsored by IEEE EDS and held in Sendai, Japan.


The P+PNP double junction type Buried Pinned Photodiode (HAD) used in the back light illumination type Modern CMOS Image Sensors

Japanese Patent Application JPA1975-127647 invented by Yoshiaki Hagiwara at Sony in 1975 with the back light illumination scheme and the built-in Global Shutter function

The original 1975 Buried Pinned Photodiode applied for CCD type Charge Transfer Devices

Back Light Illumination type CMOS Image Sensor
The First Pinned Photodiode was invented in 1975 by Yoshiaki Hagiwara at Sony.

Hagiwara also proposed in 1977 the electrical shutter clocking scheme by controlling the punch-thru overflow drain voltage.

Hagiwara realized that we don’t need the control gate over the p-region which bridges the photo charge collecting storage region and the overflow drain (VOD).

Hagiwara realized that the strong overflow drain (VOD) voltage can induce the punch-thru action to transfer all the signal photo charge completely to the VOD.

With these technology, we now can enjoy ourselves in the world of the mechanical free and filmless image sensors.


The electric shutter clocking scheme with the complete signal charge draining of no image lag can be achieved by the OFD punch-thru voltage control for any photodiodes, including not only the type (A) of the conventional CCD/MOS photo capacitor but also (B), (C) and (D) type Pinned Photodiodes.

Type(B) Double Junction type Dynamic Photo Transistor (PPD) invented in 1975 by Hagiwara.  
Type (C) and (D) Triple Junction type Dynamic Photo Thyristor (HAD) invented in 1975 by Hagiwara.

In March 2019, the History Museum of Japan sponsored by the SSIS community said that Hagiwara at Sony proposed the PPD structure in 1975 and developed in 1978.

1975-80

**Improvement of photodiode for image sensor**

*(Sony, Hitachi, NEC, Toshiba)*

~ Discrete Semiconductor/Others ~

Photodiodes are used for photodetectors of image sensors. In 1987, Sony introduced a 2 / 3-inch, 380,000-pixel CCD image sensor (ICX022) using a new type of photodetector, now called a Pinned Photodiode (Sony named it HAD: Hole Accumulation Diode)[1].

The Pinned Photodiode is a photodiode in which the entire N layer is covered with a P layer. The part of the P layer on the light incident surface is heavily doped P+ (Fig-1). Kodak named this structure Pinned Photodiode in 1984 because the P+ surface of the light incident surface was pinned to the substrate potential. This device has features such as high light sensitivity, wide dynamic range, image lag free, much smaller dark current due to reduced influence of GR center on the light receiving surface, and no white scars.

In 1975, Sony proposed using a PNP transistor as the photodetector[3]. By providing a P+ layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated, greatly improving the light sensitivity. This P+ layer was also a proposal to reduce the dark current and image lag which became the basis of the pinned photodiode.

In 1978, Sony presented a 93,000-pixel FT (Frame Transfer)-CCD image sensor compliant with the Analog TV Broadcasting Standard (SDTV) for the first time in the world[5], using the photodiode with the same structure as above. Sony succeeded in 1981 in trial production of a VTR-integrated color video camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor by further improvement of this technology[6].

References:


Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

The oxide exposed surface P+ hole accumulation region of Pinned Photodiode must have the adjacent heavily doped P+ channel stops nearby. The reason can be explained by the observation that, if covered by the surrounding depletion region extended by the strongly reverse biased buried N charge storage region, the surface P+ region would be isolated from the substrate grounded voltage and would become floating.

Consequently the electron potential of the empty potential well would also be floating, being coupled by the adjacent parasitic charge transfer gate (CTG) oxide capacitance. The situation is similar to the case of the classical N+P single junction photodiode with the floating surface N+ charge storage region, being coupled by the adjacent parasitic charge transfer gate (CTG) oxide capacitance, which is well known to have the serious image lag problem due to the incomplete charge transfer operation mode.

The empty potential well of the buried charge storage region must also be pinned to have the complete charge transfer operation mode of the no image lag feature. The adjacent P+ channel stops is a must for Pinned Photodiode to have the no image lag feature. Hagiwara Team developed in 1978 the First Pinned Photodiode with the adjacent P+ channel stops, formed by the high energy ion implantation technology without the conventional LOCOS device isolation technology which induces the serious silicon crystal stress.

Hagiwara reported in the SSDM1978 conference the CCD image sensor signal output data with the excellent short wave blue light sensitivity, the no image lag feature and the very low surface dark current feature. The choice of the high energy ion implantation technology was the key to form the P+ heavily doped adjacent channel stops for the Pinned Photodiode.
In SSDM1978 Hagiwara reported the excellent performance of the P+NP double junction type dynamic photo transistor which was later called as Pinned Photodiode by the IEDM1984 KODAK paper and also as Hole Accumulation Diode (HAD) by Sony in 1987.

However, Buried Photodiode reported by NEC in the IEDM1982 paper had the serious image lag problem and was not Pinned Photodiode by definition because the surface P+ hole accumulation region is not completely pinned. Apparently there was no heavily doped P+ channel stops adjacent to the Buried Photodiode reported by NEC at the IEDM1982.

The IEDM1982 NEC paper indeed reported the serious image lag problem.

So by definition, the photodiode reported in IEDM1984 KODAK paper was Pinned Photodiode while the buried photodiode reported in IEDM1982 NEC paper was not a Pinned Photodiode.

The reason can be explained by the observation that the surface P+ region in the IEDM1982 NEC paper may be isolated from the grounded substrate voltage by the surrounding depletion region extended by the deeply biased buried N charge storage region. The result is the floating P+ surface and the floating empty potential of the buried charge collecting storage region.
Hagiwara reported in the SSDM1978 conference the CCD image sensor signal output data with the excellent short wave blue light sensitivity, the no image lag feature and the very low surface dark current feature. The choice of the high energy ion implantation for the formation of the P+ heavily doped adjacent channel stops was the key technology. Hagiwara Team developed in 1978 the First Pinned Photodiode with the adjacent P+ channel stops, formed by the high energy ion implantation technology. Sony did not used the conventional LOCOS device isolation technology which induces the serious silicon crystal stress.

NEC apparently understood by 1982 that the LOCOS device isolation technology induces the serious silicon crystal stress and is not suited for the image sensor processing. NEC did not use the LOCOS device isolation technology for the buried photodiode process formation. NEC 1982 photodiode was not Pinned Photodiode while KODAK 1984 photodiode was Pinned Photodiode.

NEC in the IEDM1982 paper did not apparently use the high energy ion implantation and had no heavily doped surface P+ channel stops adjacent to the buried photodiode. This may be the reason why the P+ surface becomes floating and causing the serious image lag problem in the NEC IEDM1982 buried photodiode. On the other hand, the IEDM1984 KODAK paper used the LOCOS isolation technology which has the hidden P+ channel stops under the LOCOS region that would pin down the adjacent P+ surface potential. Hence the KODAK Photodiode is Pinned Photodiode, for the first time used in the Interline Transfer CCD image sensor.
Pinned Photodiode is by necessity Buried Photodiode, but not all Buried Photodiodes are pinned.

The first Pinned Photodiode was invented by Hagiwara at Sony and is used in ILT CCD Pinned Photodiodes, these same Pinned Photodiodes and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

Hagiwara proposed in JPA 1975-134985 the double Junction (P+NP) type dynamic Photo Transistor in the (Nsub) substrate with the Pinned P+ surface Hole Accumulation layer.

Edited this Answer to acknowledge Hagiwara-san's contribution, it has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors).

Teranishi did not invent the Pinned Photodiode. The NEC IEDM1982 paper had the serious image lag problem. It was NOT Pinned Photodiode. It was just a Buried Photodiode with the serious image lag problem. Fossum did not invent the in-Pixel source follower amplifier circuit for the Active Amp CMOS image sensors. Peter Noble invented the in-Pixel Amp in 1968. Fossum wrote a fake paper in 2016 in which Fossum insulted SONY and Hagiwara by making a false statement, saying that Hagiwara 1975 patent application had no description on the image lag feature, which is not true. Hagiwara 1975 PPD patents indeed had clear descriptions of the complete charge transfer and no image lag feature.
The First PPD was invented by Hagiwara in 1975. Teranishi did not invent PPD.


Fossum did not invent the in-Pixel Amp Active CMOS Image Sensor.


**KODAK also had the USP patent on the CMOS process applied to the In Pixel Source Follower Amplifier circuit for modern CMOS Image Sensors.**

Kodak still used the LOCOS technology for the image sensor process. Yes, there is possibly hidden P+ channel stops for pinning under the **LOCOS (1)** Area Edge and also at the boundary **LOCOS (2)**.
Fossum wrote a fake paper in 2016 in which Fossum insulted SONY and Hagiwara by making a false statement, saying that Hagiwara 1975 patent application had no description on the image lag feature, which is not true.

Sony does not use the LOCOS technology which may have the serious trouble of the silicon crystal stress and also the possible disconnection between the heavily dope P+ channel stops under the LOCOS and the P+ surface hole accumulation layer. Hagiwara 1975 PPD patents indeed had clear description of the empty potential well, the evidence of complete charge transfer and no image lag feature.
Hagiwara applied two Japanese Patents JPA1975-127646, and JPA1975-127647 for the back light illumination type Pinned Photodiode with Global Shutter Function which is a very important feature needed for the modern CMOS image sensors. The complete charge transfer mode and the no image lag feature is also shown and implied by the empty potential well of the buried charge storage region.
Hagiwara also applied two Japanese Patents JPA1975-134985 for the PPD structure with the VOD and also JPA1977-126885 on the electrical shutter clocking scheme controlling the overflow drain voltage in the punch-thru mode.


**Pinned Photodiode and Sony Hole Accumulation Diode (HAD)**

Pinned Surface Double Junction P+NP Dynamic Photo Transistor in the silicon substrate (Nsub)

Pinned Photodiode with the vertical overflow drain (VOD) function in the silicon substrate (Nsub)

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Double Junction Dynamic Photo Transistor (PPD) invented in 1975 by Hagiwara at Sony.


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Japanese Patent JPA 1977-126885 on Electrical Shutter Clocking Scheme


The First Pinned Photodiode was invented in 1975 by Yoshiaki Hagiwara at Sony

Difference of the static and dynamic photo transistors are illustrated in these figures. Sony Hole Accumulation Diode (HAD) is the P+NPNsub junction dynamic photo transistor with the surface P+ hole collecting and accumulation region is pinned and grounded, which is now widely called as Pinned Photodiode with the vertical overflow drain (VOD) function. Only Pinned Photodiode with the VOD function can realize the electrical shutter function.

SONY HAD Sensor 1975 was hinted by SONY PNP Bipolar Transistor Process Technology

Conventional Static Phototransistor

(by John Northrup Shive, 1950)

Dynamic Phototransistor Operation

by Yoshiaki Hagiwara at Sony in 1975

Dynamic Memory function is involved.

Collector

According to the light intensity, the collector current is modified in the conventional phototransistor

Emitter

The charge transfer device (CTD) can be CCD or CMOS type.

No memory function is involved.


textual content continues...
**Four Types of Image Sensor Structure**

1. **The N+P Single Junction Type**
   - Classical Floating Surface Dynamic Photodiode

2. **The CCD/MOS Metal Oxide Gate Dynamic Photo Capacitor**
   - Invented and developed by Boyle/Smith in 1969

3. **The P-NPSub Double Junction Type**
   - Pinned Photodiode invented by Hagiwara in 1975 and developed in 1978 by Hagiwara Team in Sony with Excellent Blue Light Sensitivity No Image Lag and No Surface Dark Current

4. **The P-NPNSub Triple Junction Type**
   - Pinned Photodiode invented by Hagiwara in 1975 and developed in 1987 by Hamazaki Team in Sony with Completely Mechanical Parts-Free No Image Lag Electric Shutter

<table>
<thead>
<tr>
<th></th>
<th>Blue Light Sensitivity</th>
<th>Image Lag</th>
<th>Surface Dark Current</th>
<th>Electric Shutter</th>
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<td>1</td>
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<td>✗</td>
<td>✓</td>
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**Four Types of Image Sensor Structure**
Since PPD also has the complete charge transfer capability, a single polysilicon electrode type CCD delay line becomes possible with the complete charge transfer, by creating the pinned potential wells of PPD at the polysilicon electrode gaps.
The electric shutter function becomes possible only in the CCD/MOS type photo capacitor sensor and Pinned Photodiode (PPD), both of which have the complete charge transfer capability of no image lag. However, Buried Photodiode (BPD) is not always Pinned Photodiode (PPD). But, Pinned Photodiode (PPD) is always Buried Photodiode (BPD). Buried Photodiode (BPD) and Pinned Photodiode (PPD) are both the same double junction type PNP dynamic photo transistors invented by Yoshiaki Hagiwara in 1975.

Hagiwara applied two Japanese Patents JPA1975-127646, and JPA1975-127647 for the back light illumination type Pinned Photodiode with Global Shutter Function which is a very important feature needed for the modern CMOS image sensors. The complete charge transfer mode and the no image lag feature is also shown and implied by the empty potential well of the buried charge storage region.

Hagiwara also applied two Japanese Patents JPA1975-134985 for the PPD structure with the VOD and also JPA1977-126885 on the electrical shutter clocking scheme controlling the overflow drain voltage in the punch thru mode.

Teranishi did not invent Pinned Photodiode. The NEC IEDM1982 paper had the serious image lag problem. It was NOT Pinned Photodiode. It was just a Buried Photodiode with the serious image lag problem. We cannot not obtain the empty potential well unless the surface P+ hole accumulation layer is completely pinned.
The simple analysis of the saturation mode MOS transistor Current and Voltage Relationship can be used to explain why the classical floating N+P junction type photodiode has the serious image lag problem. The limited time allowed for reset is the cause of the serious image lag problem since it would take a long time for transferring the signal charge $Q_{\text{sig}}$ thru the adjacent charge transfer gate (CTG).

The floating N+P junction type photodiode has the serious Image Lag Problem.

Buried Photodiode with no Pinned Surface also has the serious Image Lag problem.

Enen the P+NPNsub junction type Sony Hole Accumulation Diode (HAD) would have the serious image lag and would not have been operated in the complete image lag free mode with the electrical shutter capability unless the surface P+ hole accumulation layer is pinned by the adjacent heavily doped P+ channel stops.

If the surface P+ hole accumulation layer is floating, it may be at some positive value potential and would have no enough voltage drop between the surface P+ hole accumulation layer and the buried N type signal charge storage region. The buried N type signal charge storage potential would stay at a strong positive potential and the signal charge would not be transferred completely to the charge transfer gate (CTG) nearby and would suffer the serious image lag problem.
Hagiwara in 1975 proposed the PPD Charge Transfer which is later called as Virtual Phase Charge Transfer. Hagiwara in 1975 proposed also the NEC Buried Photodiode, the KODAK PPD and the Sony HAD. Study Japanese Patent 1975-127646, 1975-127647 and 1975-134985 for the details.
Pinned Photodiode (PPD) has the excellent short wave blue light sensitivity, the very low surface dark leakage current feature and the complete charge transfer capability for the excellent image lag free picture quality needed for the electric shutter. Now this double junction type PPD is proposed to apply for solar cells.
The First Pinned Photodiode was invented in 1975 by Yoshiaki Hagiwara at Sony.

Silicon Based Solar Cells of the energy gap \( E_g = 1.10 \text{ eV} \) cannot convert photon energy of the wavelength more than \( \lambda = 1.12 \mu\text{m} \).

Hagiwara invented PNP junction type PPD in 1975 with
1. blue light 100% QE,
2. No Surface Dark Current and
3. No Image Lag, Complete Charge Transfer features.
The Barrier Potential $V_B$ and the Width $W_B$

- $V_B = kT \ln \left( \frac{N_{pp}}{N_p} \right)$
- $W_B = W_0 \frac{V_B}{V_o}$

$D(x) = -N_p - N_{pp} \exp \left( -\frac{x^2}{R^2} \right)$ for $x > 0$

$\frac{d^2 D(x)}{dx^2} = 0$ at $x = W_0$

$W_0 = \frac{R}{\sqrt{2}}$

$\varepsilon_s \frac{d^2 V(x)}{dx^2} = -D(x) - (N_p + N_{pp}) \exp \left( -\frac{V(x)}{kT} \right)$

- $V(x) = 0$ at $x = 0$
- $V(x) = V_B$ at $x = W_B$

$N_0 = N_p + N_{pp} \exp \left( -\frac{W_0^2}{R^2} \right)$

$N_0 = (N_p + N_{pp}) \exp \left( -\frac{V_0}{kT} \right)$

P+P Doping Slope Barrier Potential $V_B$

- $V(x) = e^-e^-$
- $e^+ e^+ e^+$

$\rho(x) = D(x) + \text{hole}(x)$
Origin of 1975 Pinned Photodiode Concept was hinted by CCD/MOS type Buried Photodiode

See JPA 1975-127646, JPA 1975-127647 and JPA 1975-134985
by Yoshiaki Hagiwara in 1975

Numerical Computation of Potential V(x) of Arbitrary Doping Profile D(x) from x = 0 to x = Xw with the given boundary condition V(x) = Vs and dV(x)/dx = Es at x = 0.
Find the proper value of V(x) = Vs so that we have V(x) = Vw and dV(x)/dx = Ew at x = Xw.

For x < 0 in Type(1) and Type(2)
\[ \frac{d^2V(x)}{dx^2} = 0 \]
gives at x = 0
\[ E_s = C_{ox} \left( V_s - V_G + V_{mo} - V_{os} \right) / E_{si} \]

For 0 < x < Xw in all types (1) thru (4)
\[ E_{si} \frac{d^2V(x)}{dx^2} = D(x) - N_{pp} \exp \left( - \frac{V(x)}{kT} \right) \]
needs to be solved numerically for any arbitrary doping function D(x).

For x < 0 in Type(3) and Type(4)
\[ \varepsilon_{si} \frac{d^2V(x)}{dx^2} = N_{pp} - N_{pp} \exp \left( \frac{V_{pin} - V(x)}{kT} \right) \]
gives at x = 0
\[ E_s = \sqrt{\frac{2N_{pp}kT}{\varepsilon_{si}}} \left( \frac{V_s}{kT} - 1 + \exp \left( - \frac{V_s}{kT} \right) \right) \]

For Xw < x in all types (1) thru (4)
\[ \varepsilon_{si} \frac{d^2V(x)}{dx^2} = N_{pp} - N_{pp} \exp \left( - \frac{V(x)}{kT} \right) \]
gives at x = Xw
\[ E_w = -\sqrt{\frac{2N_{pp}kT}{\varepsilon_{si}}} \left( \frac{V_w}{kT} - 1 + \exp \left( - \frac{V_w}{kT} \right) \right) \]

The conventional Buried Channel CCD/MOS type photodiode has a very large surface electric field E_s.

The surface electric field E_s of the P+NP junction type Pinned Photodiode is also very large which is worse since the surface electric field depends also on the surface P+ doping level N_{pp}. Type (2) and Type (3) modifications may help reducing the surface electric field E_s.
Hagiwara had the idea of the lightly doped drain (LDD) concept and used for the CCD output of Sony FT (FCX018) and ILT (ICX008) CCD image sensors that Hagiwara designed and developed with other Sony engineers in 1978. But Hagiwara did not disclose the details of CCD design knowhow to the public. Hagiwara did not file any patent on the LDD concept in 1978.

Sony used already in early 1970s the correlated double sampling (CDS) technique intensively for the clock noise reduction for CCD image sensors. This CDS technique reduced the clock noise of MOS image sensors much more drastically.

Sony reported “High Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor” in ISSCC2006.

Modern CMOS Image Sensors have (1) HAD (2) APS and (3) CDS.

(1) HAD (PPD) was invented by Y. Hagiwara in 1975.
(2) APS was invented by Peter Noble in 1968.
(3) CDS was invented by M. White in 1972.

(4) Sony engineers perfected these technologies in 2006.

We all came to a long way since Peter Noble invented the Active Amp in 1968. Modern CMOS Image Sensors used the technology of CDS, Active Amp and PPD.

CMOS Inverter and Source Follower circuits are basics for digital circuit design. But we had to wait till the advancement of CMOS process scaling rule, in order to place the source follower active circuit in each small picture cell area. Meanwhile CCD had a great role in the advancement of image sensors in 1980s. For modern high definition TV image sensor applications, CCD has the power issue and also the limit in charge transfer efficiency of 99.999%, which is not enough now.
In classical image sensors, the single junction type N+P dynamic photodiode was used with the floating surface charge collecting storage N+ region, which suffered the incomplete charge transfer that created the serious image lag problem.

Hagiwara at Sony proposed in 1975 the double junction type P+NP dynamic photo transistor, Pinned Photodiode (PPD), with the pinned surface hole accumulation P+ layer with no image lag feature and the extremely low surface dark current feature. Hagiwara also proposed at the same time in 1975 the triple junction type P+NPN_{sub} dynamic photo thyristor, Sony Hole Accumulation Diode (HAD), with the in-pixel Vertical Overflow Drain (VOD) function with no image lag feature which made possible to achieve the electrical shutter function.
The First Pinned Photodiode was invented in 1975 by Yoshiaki Hagiwara at Sony.

In Japanese Patent Application JPA 1975-124676, Yoshiaki Hagiwara at Sony in 1975 invented the First Pinned Photodiode in the form of a triple junction N+NP+NP dynamic photo thyristor with the electron-accumulation pinned N+ surface layer and which has the surface N+N barrier electric field that can separate effectively the photo electron and hole pairs generated within the 0.2 \( \mu \text{m} \) in the vicinity of the pinned N+ Si surface.

**Japanese Patent Application**  
**JPA 1975-127646**  
**on the triple junction N+N-P+NP-P type**  
**Dynamic Photo Thyristor**  
**< the first Pinned Photodiode >**  
**with the in-pixel built-in vertical charge draining and overflow draining (VOD) capability and the MOS buffer memory for the Global Shutter function with the N+N Pinned Surface.**

![Diagram](image)

It is well known that the short wave blue light cannot penetrate more than 0.2 \( \mu \text{m} \) in depth into the silicon crystal. However, the surface N+N barrier electric field can be created at the silicon surface within the 0.2 \( \mu \text{m} \) in depth and can be used effectively to separate photo electron and hole pairs generated in the vicinity of the Si surface.

On the other hand it is very difficult to create, within the silicon surface of the 0.2\( \mu \text{m} \) in depth, the N+P junction depletion region for the photo electron hole pair separation.

In conventional single junction type N+P photodiodes, the floating surface N+ region has a flat surface potential of no surface electric field. The pairs cannot be separated effectively in the surface floating N+ region. Eventually, the pairs in the floating N+ surface will be recombined, not contributing the photo electron and hole generations.

This is why the classical single junction type N+P dynamic photodiode has the poor short wave blue light sensitivity. Conventional solar cells also use the classical N+P single junction type photodiode with the floating N+ surface of poor short wave blue light sensitivity. This is why the current solar cell has a poor efficiency of about 20%.
Hagiwara proposed the MOS capacitor type buffer memory for the Global Shutter function, absolutely needed for the modern CMOS image sensors. See JPA 1975–124647.

Hagiwara also proposed the double junction type Dynamic Photo Transistor with the complete charge transfer operation capability of no image lag feature to achieve the electrical shutter function for digital cameras, completely free from mechanical parts.

N+NP+N junction type Buried Pinned Photodiode
with Built-in MOS Capacitor Buffer Memory Global Shutter Function and the surface N+N doping slope Carrier Electric Filed Photo Pair Generation

Hagiwara also proposed in JPA 1975–134985, the double junction P+NP type Dynamic Photo Transistor on the silicon substrate (Nsub), which was later called as Sony Hole Accumulation Diode (HAD) in 1987 with the vertical overflow drain (VOD) function. It has also the complete charge transfer operation capability of no image lag feature with the pinned P+ surface potential, which is needed absolutely in order to achieve the electrical shutter function for digital cameras, completely free from mechanical parts. Hagiwara also proposed in JPA 1977–126885 the basic clocking scheme of the electrical shutter operation using the punch thru operation mode of the in-pixel overflow drain voltage control scheme.

PNPN junction Transistor type Pinned Photodiode
Visit https://www.j-plupat.jp/en/ and put the patent number 1975–134985

PNPN junction Transistor type Pinned Photodiode