受光表面P＋層と裏面のP+層の両面がピン留め接地された、P+PNPP+接合型新型太陽電池の提案

非常に複雑な半導体電子デバイスの物理動作とその構造の説明に挑戦する事になる。できるだけ直観に訴える方法で説明し、数式は極力さけて、基本原理動作を直観的なイメージで理解できる様に工夫をこらして文系の一般社会人の皆様にも親しみを感じる半導体の基礎知識の紹介となればと希望する。

(1)金属と絶縁体の違い

(2)半導体の基本特性

(3) single接合型のダイオードの整流特性

(4) double 接合型バイポーラトランジスタの電流増幅特性

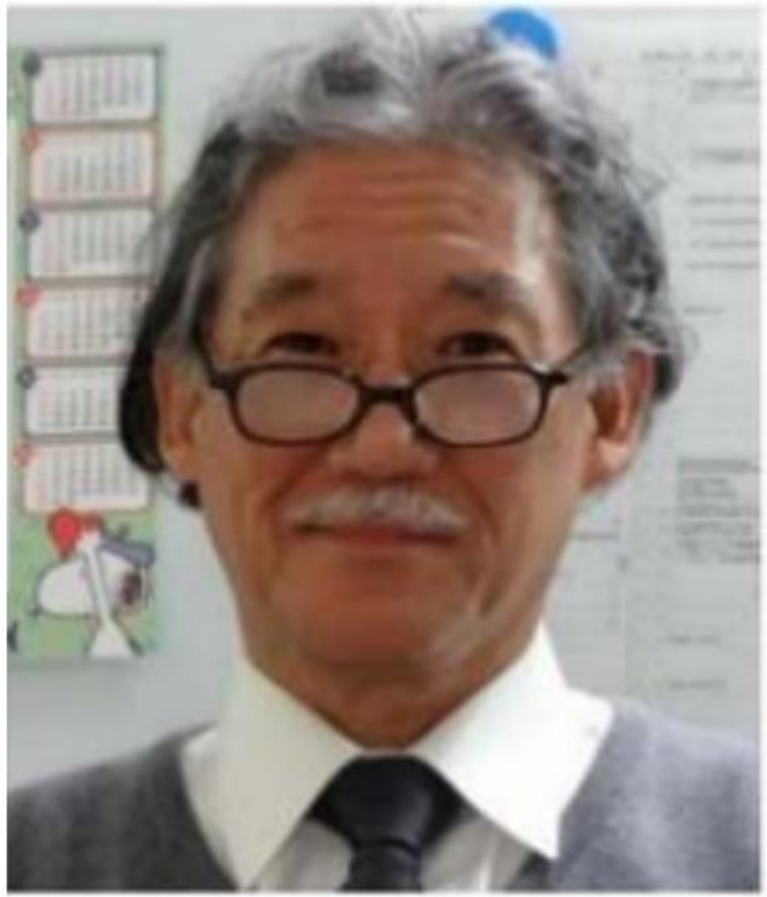
(5) triple 接合型サイリスター型の理想的な高速Switch動作特性

(6) MOS型のトランジスタの電流増幅特性

(7) CMOS型インバータ回路の省エネ特性

(8) 超光感度のCMOS型イメージセンサーの特性

(9) double接合型の新型太陽電池の構造とその動作原理



崇城大学 理事長付き 特任教授
IEEE Life Fellow, Ph.D., 工学博士

受光表面P＋層と裏面のP+層の両面がピン留め接地された、P+PNPP+接合型新型太陽電池の提案

(7) CMOS型インバータ回路の省エネ特性

詳細は青山社出版の人工知能パートナーシステム(AIPS)を支える「デジタル回路の世界」に記載。

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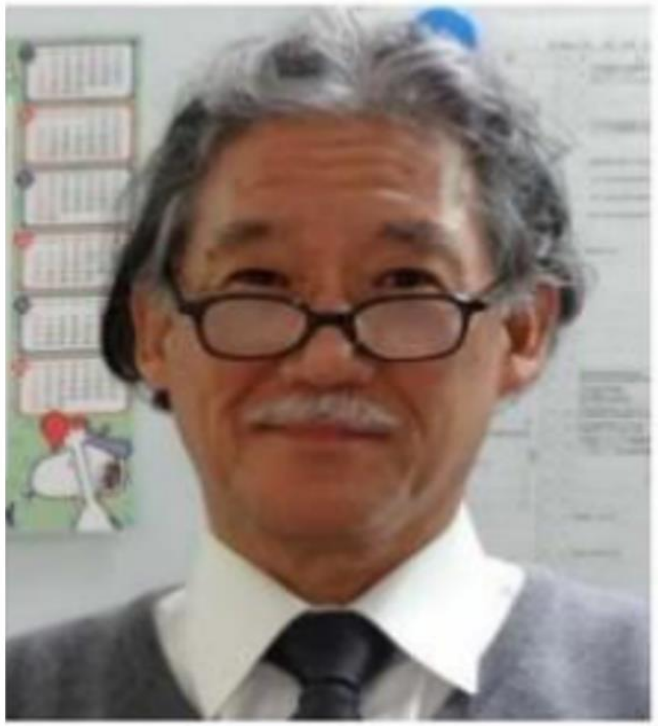


崇城大学 理事長付き 特任教授

IEEE Life Fellow, Ph.D., 工学博士

人工知能パートナーシステム(AIPS)を支える

デジタル回路の世界

IEEE Life Fellow, Ph.D.

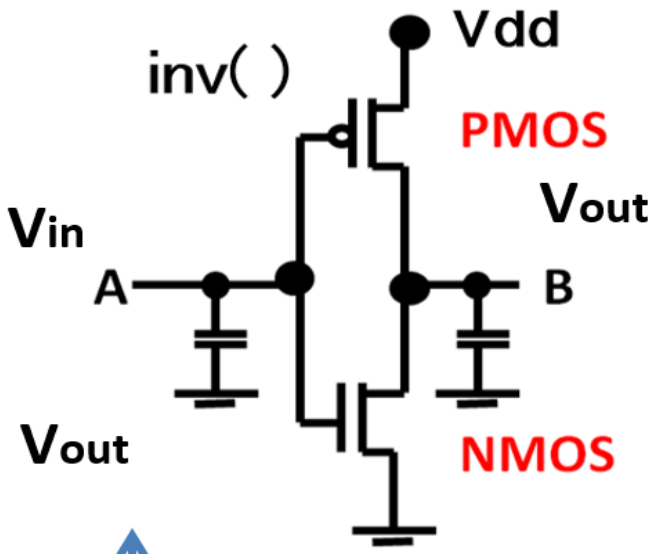
萩原 良昭 著

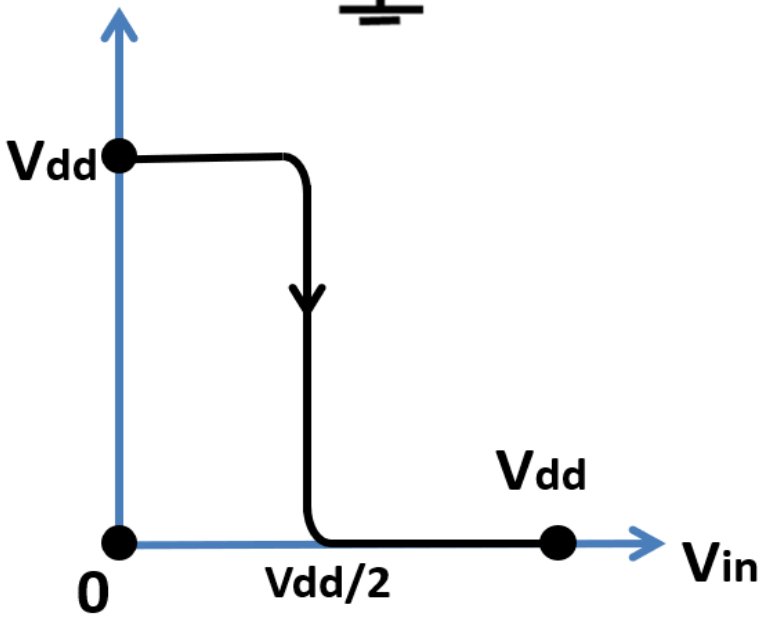
ISBN978-4-88359-339-2 B5判 上製 475頁

定価(本体9,000円＋税)

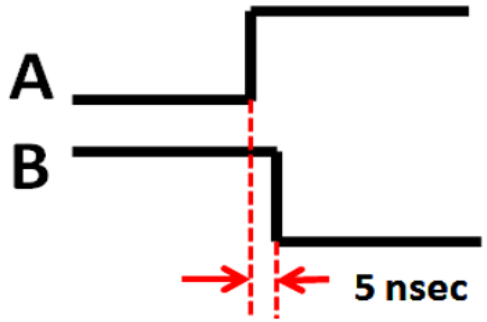
未来の人間社会には人工知能パートナーシステム(AIPS)とも言える人間にやさしい支援システムが出現すると期待している。AIPS搭載の自動走行車や老人介護システム、人間型歩行ロボットやロボット・ハウスなどである。そこで本書では、そのAIPSを支える「デジタル回路の世界」と題し、ハードとソフトの両面で、人とコンピュータをつなぐデジタル技術について紹介している。図や絵をたくさん用意して、基礎からやさしく解説している。

図 4-5-1





Inverterの信号遅延時間(Delay Time)は ～5nsec.



Clock 周波数

1 Hz ←→ 1 sec (3×10^{10} cm)

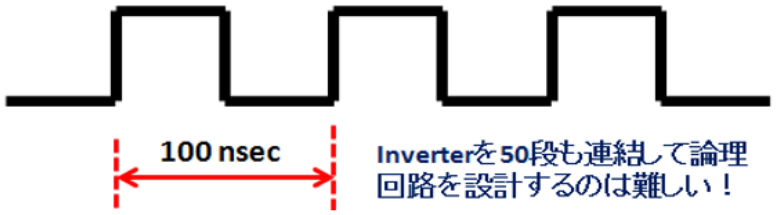
1KHz ←→ 1 msec (3×10^{7} cm)

1MHz ←→ 1 μsec (3×10^{4} cm)

1GHz ←→ 1 nsec (30 cm)

（光は1秒間に 30万Km 進む）

Clock 周波数 が 10 MHz なら Clock 幅は 100nsec



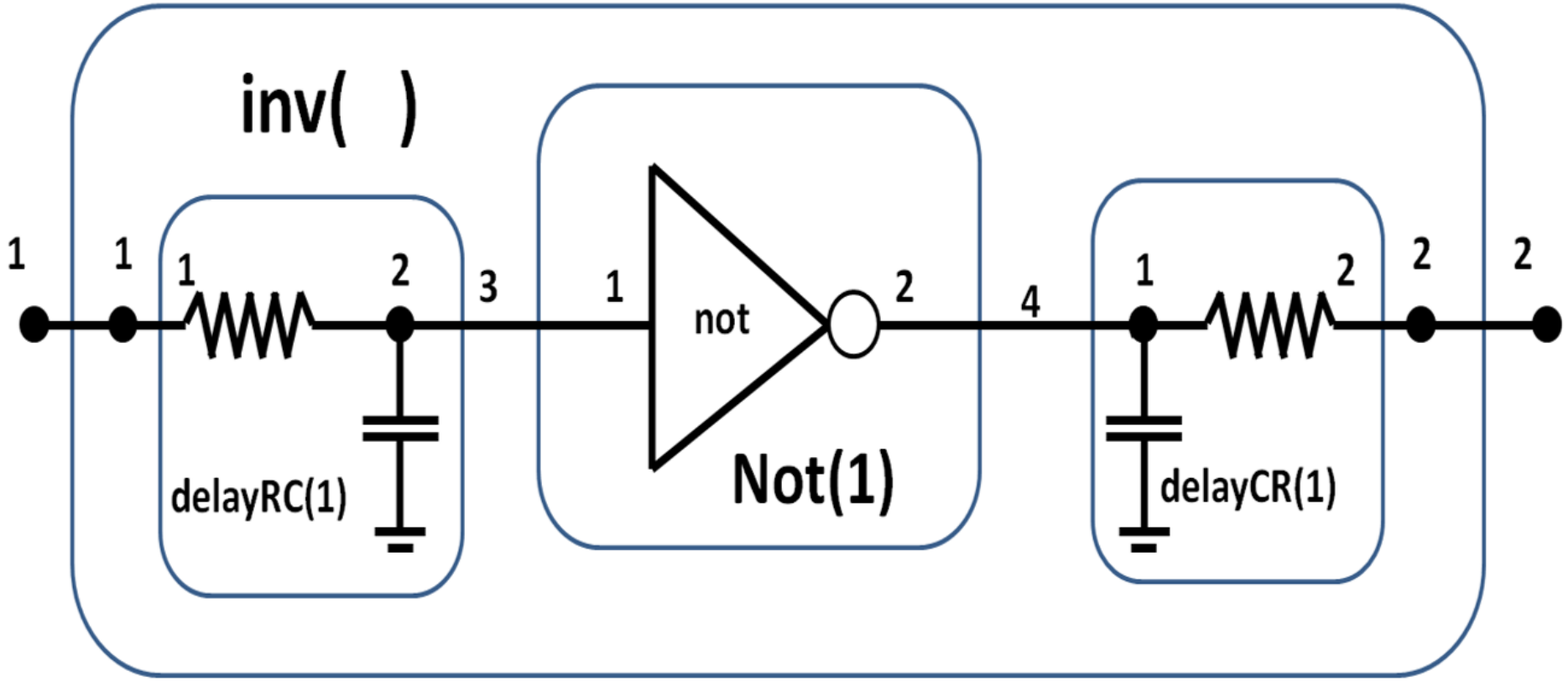
Inverterを50段も連結して論理回路を設計するのは難しい！

CMOS Inverter 回路 inv( )とその遅延時間

図 4-5-2

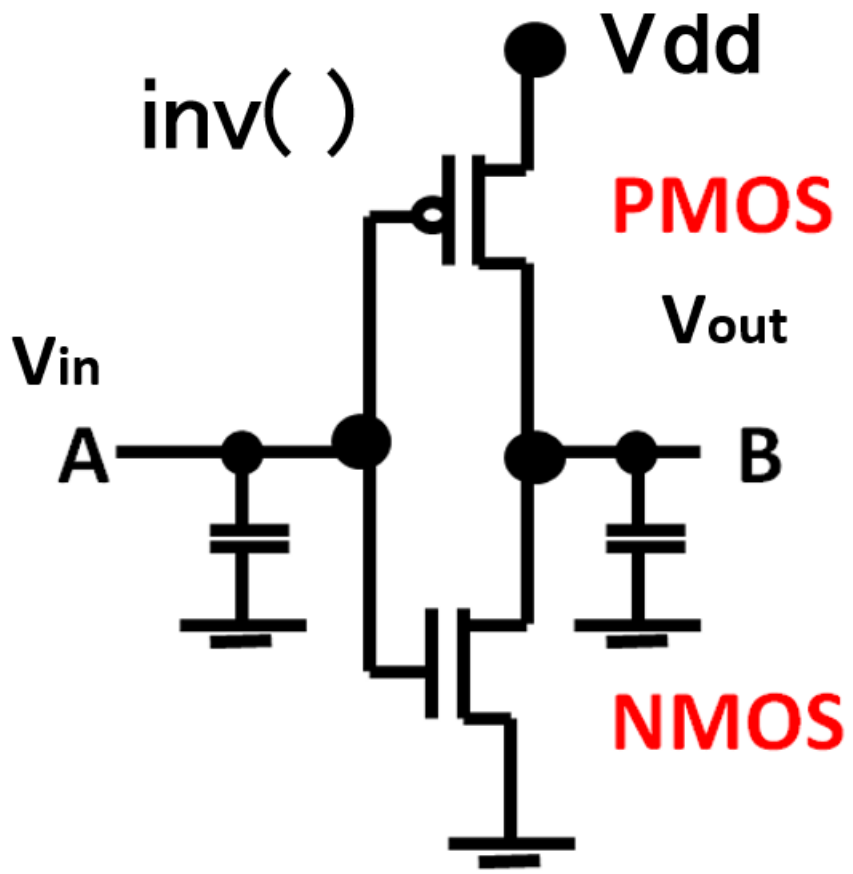
DCDL（digital circuit description language）のよる coding 例

```
define   inv( )  { input   [1];   output   [2];
          [3]=delayRC(1) [1] ; [4]=not(1)[3];   [2]=delayCR(1)[4];  }
```



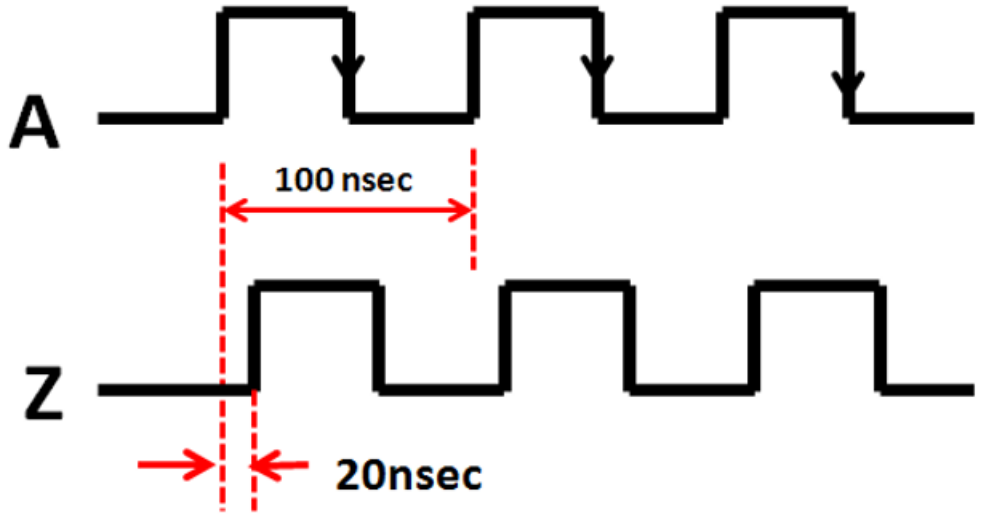
RC遅延を考慮した inv( ) 回路図とその coding 例

図 4-5-3



Inverterの信号遅延時間(Delay Time)は ～5nsec.

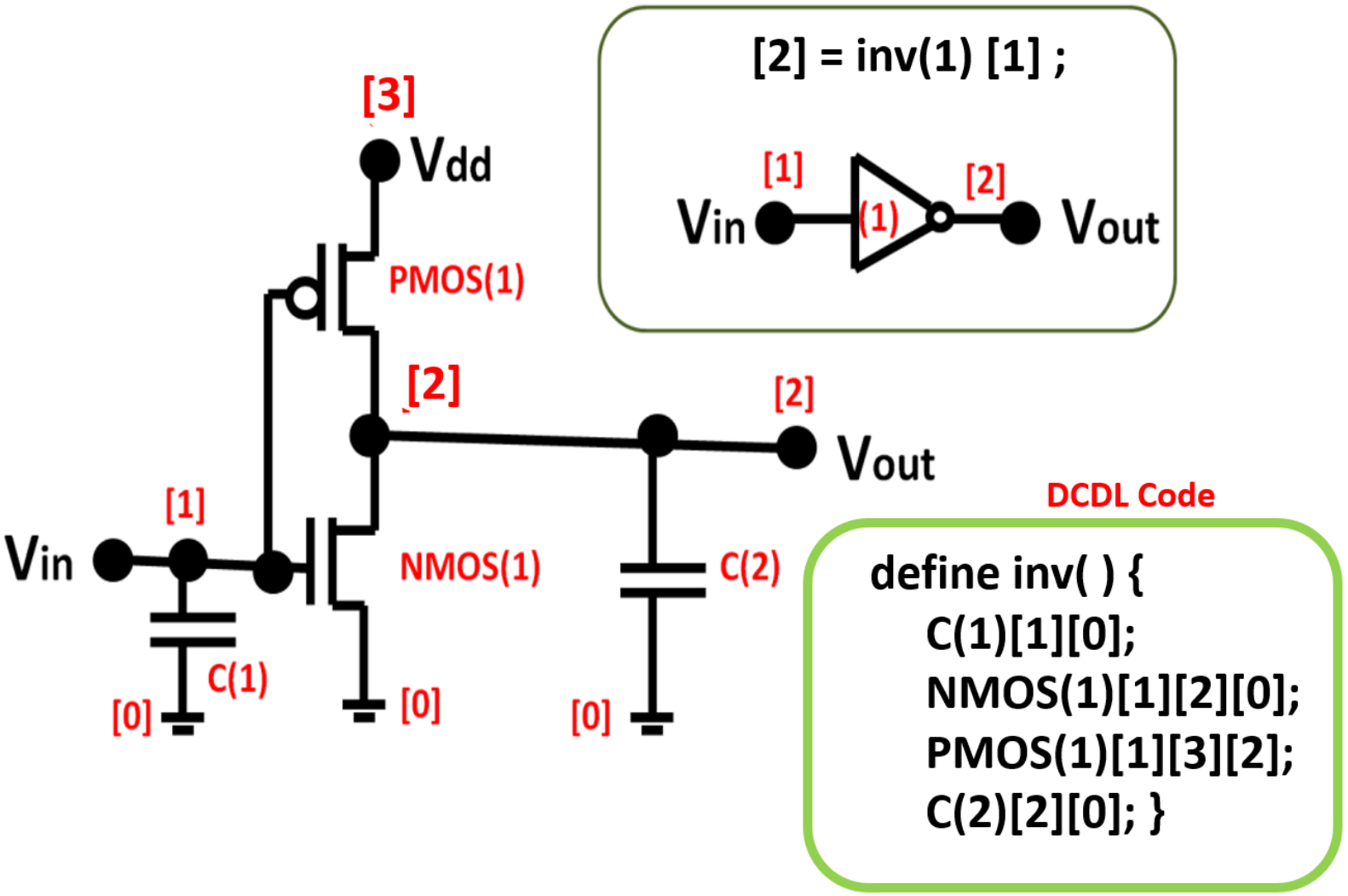
Clock 周波数が 10 MHz なら Clock 幅は 100nsec



CMOS inverter を複数個（偶数個）連結した遅延回路

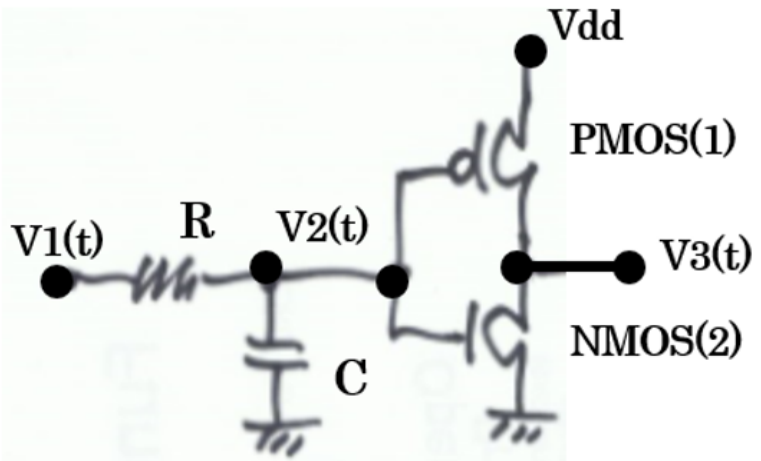
図 4-5-4

DCDL (digital circuit description language) のよる coding 例



入出力容量を考慮したCMOS inverter回路 inv( ) 回路の coding例

図 4-5-5



Case (1) when t1 < t < t3,

V2(t) = Vdd { 1 - exp(- (t –t1) /RC) }

V2(t2) = Vdd/2 = Vdd { 1 - exp (- Δt1/RC) }

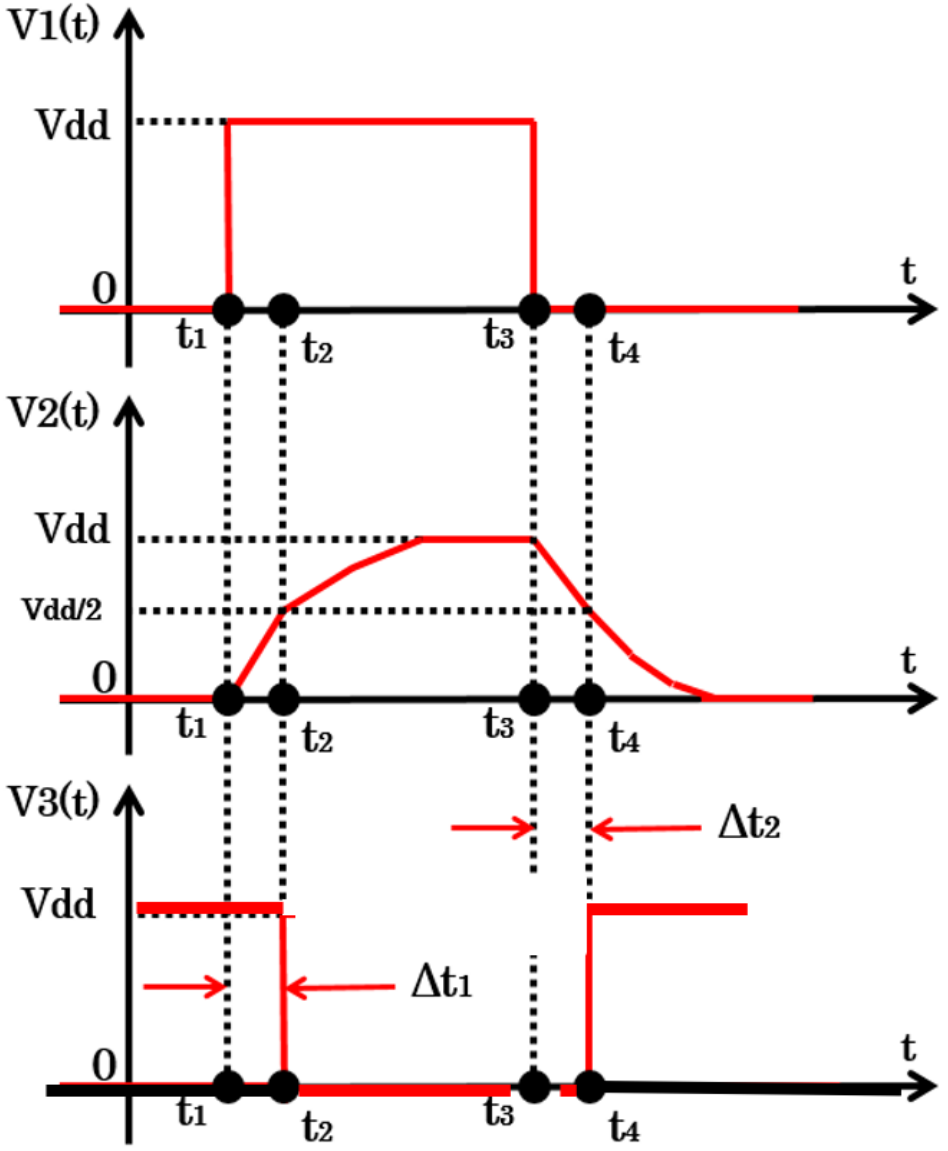
Δt1 = (ln 2) RC ～ 0.69 RC ;

Case (2) when t3< t ,

V2(t) = Vdd exp(- (t –t3) /RC)

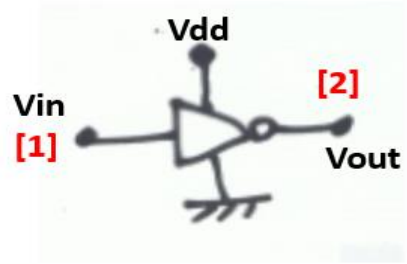
V2(t4) = Vdd/2 = Vdd exp (- Δt2/RC)

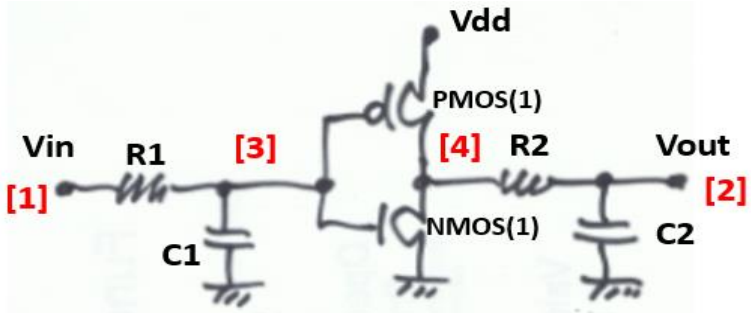
Δt2= (ln 2) RC ～ 0.69 RC ;



入力信号側にRC回路がある inverter 回路 inv( ) の入出力特性

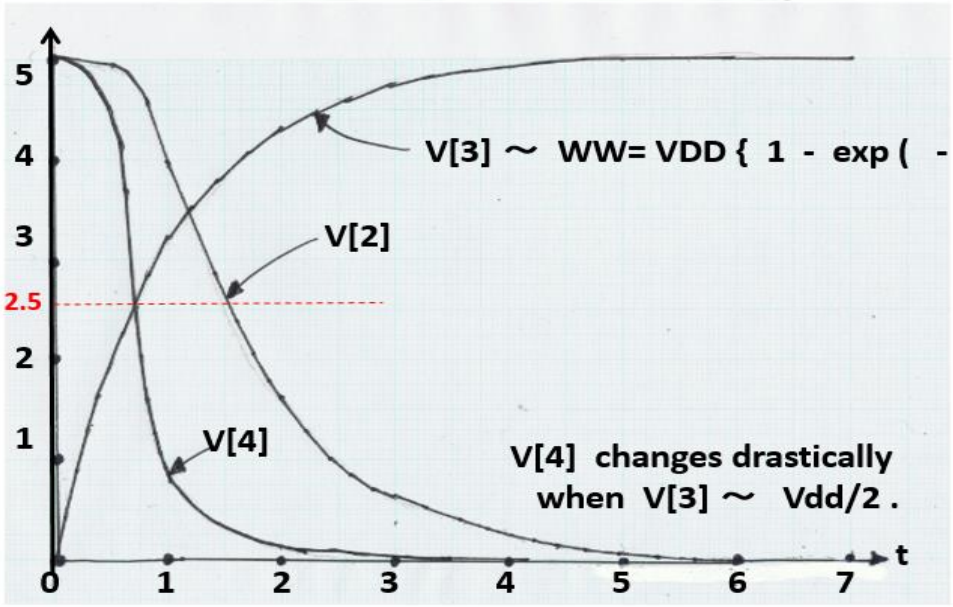
図 4-5-6





Vdd=5 volt, Vss= 0 volt, R1=C1=1 ; R2=C2=1 ; として計算している。

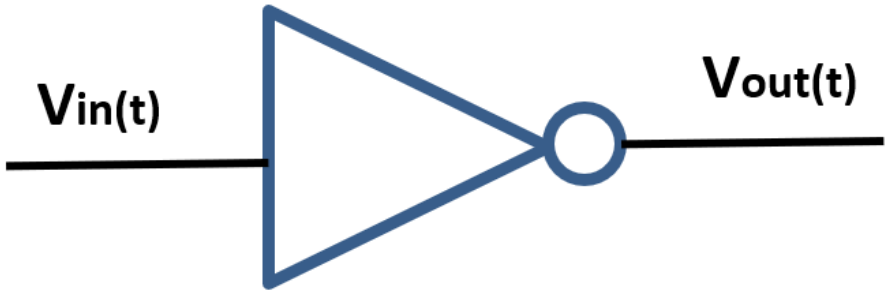
```
define   inv ( )

{   input 1; output 2;

    R1(1)[1][3];
    C1(1)[3][Vss];

PMOS(1)[3][Vdd][4];

NMOS(1)[3][4][Vss];
    R2(1)[4][2];
    C2(1)[2][Vss];  }
```

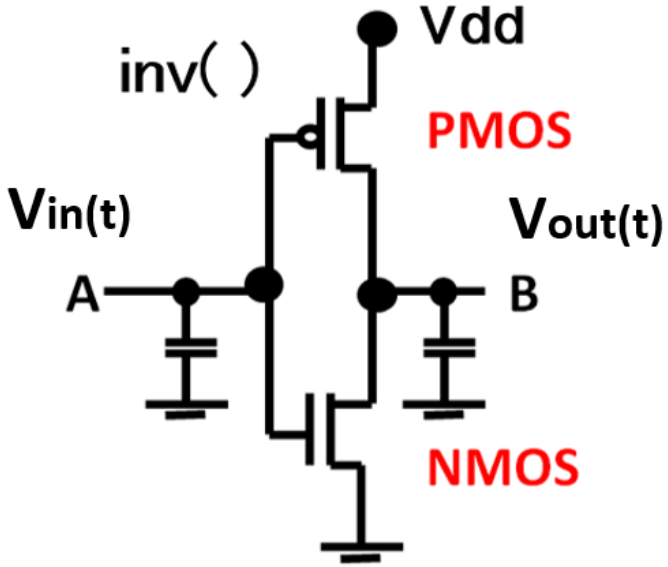


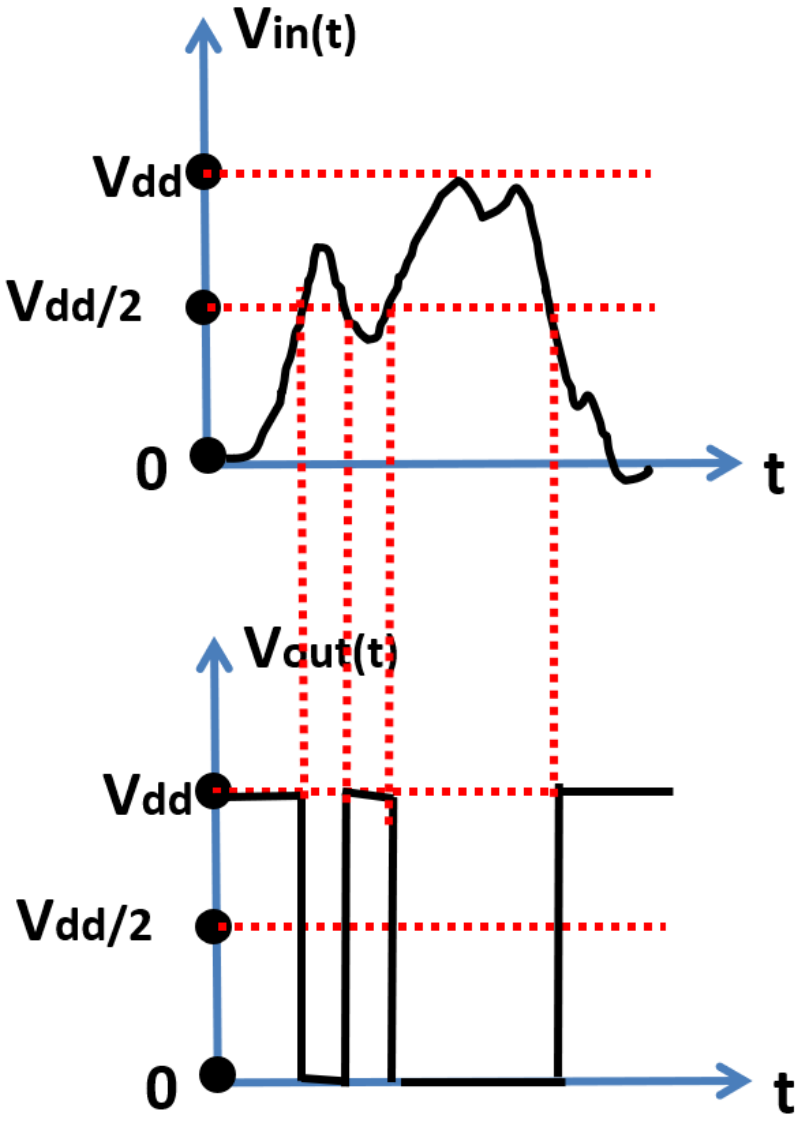
t	WW	V[3]	V[4]	Vout= V[2]
t=0.000000	WW=0.000000	W3=0.000000	W4=5.000000	W5=5.000000
t=0.010000	WW=0.049751	W3=0.049503	W4=5.000000	W5=5.000000 KK=6
t=0.020000	WW=0.099007	W3=0.098762	W4=5.000000	W5=5.000000 KK=6
t=0.030000	WW=0.147772	W3=0.147530	W4=5.000000	W5=5.000000 KK=6
t=0.040000	WW=0.196053	W3=0.195813	W4=5.000000	W5=5.000000 KK=6
t=0.050000	WW=0.243853	W3=0.243615	W4=5.000000	W5=5.000000 KK=6
t=0.060000	WW=0.291177	W3=0.290942	W4=5.000000	W5=5.000000 KK=6
t=0.070000	WW=0.338031	W3=0.337798	W4=4.999845	W5=5.000000 KK=6
t=0.080000	WW=0.384418	W3=0.384187	W4=4.999224	W5=4.999995 KK=6
t=0.090000	WW=0.430344	W3=0.430116	W4=4.998126	W5=4.999983 KK=6
t=0.100000	WW=0.475813	W3=0.475587	W4=4.996551	W5=4.999957 KK=6
t=1.000000	WW=3.160603	W3=3.160511	W4=0.799869	W5=3.932332 KK=6
t=2.000000	WW=4.323324	W3=4.323290	W4=0.112828	W5=1.619269 KK=6
t=3.000000	WW=4.751065	W3=4.751052	W4=0.033705	W5=0.631494 KK=6
t=4.000000	WW=4.908422	W3=4.908417	W4=0.012613	W5=0.244784 KK=5
t=5.000000	WW=4.966310	W3=4.966309	W4=0.004822	W5=0.094776 KK=5
t=6.000000	WW=4.987606	W3=4.987606	W4=0.001858	W5=0.036681 KK=5
t=7.000000	WW=4.995441	W3=4.995440	W4=0.000718	W5=0.014194 KK=5
t=8.000000	WW=4.998323	W3=4.998323	W4=0.000278	W5=0.005493 KK=4
t=9.000000	WW=4.999383	W3=4.999383	W4=0.000107	W5=0.002125 KK=4
t=10.00000	WW=4.999773	W3=4.999773	W4=0.000042	W5=0.000822 KK=4

入力端子の容量と出力端子の容量の両方を考慮したinverter回路の特性

図 4-5-7(1)

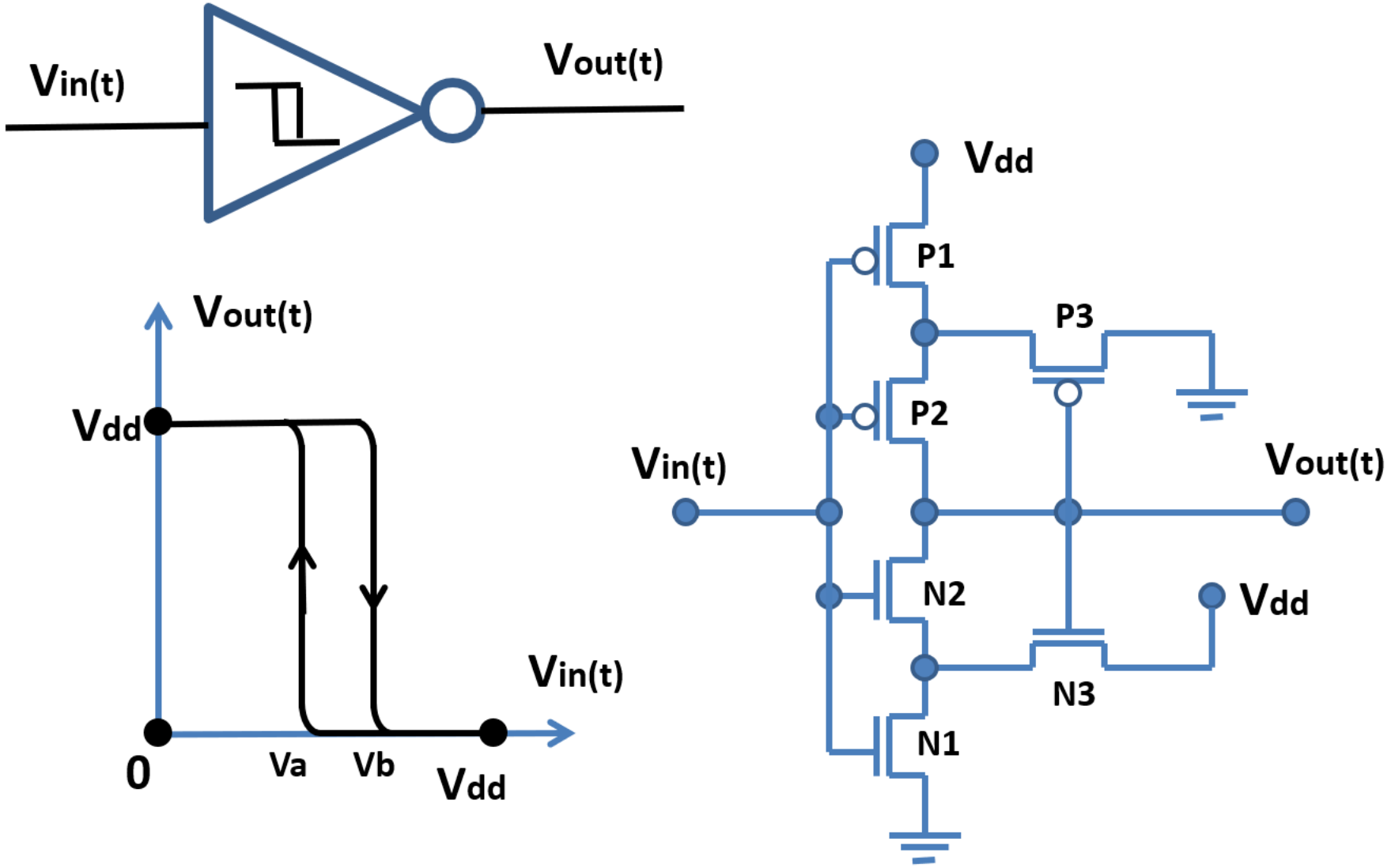






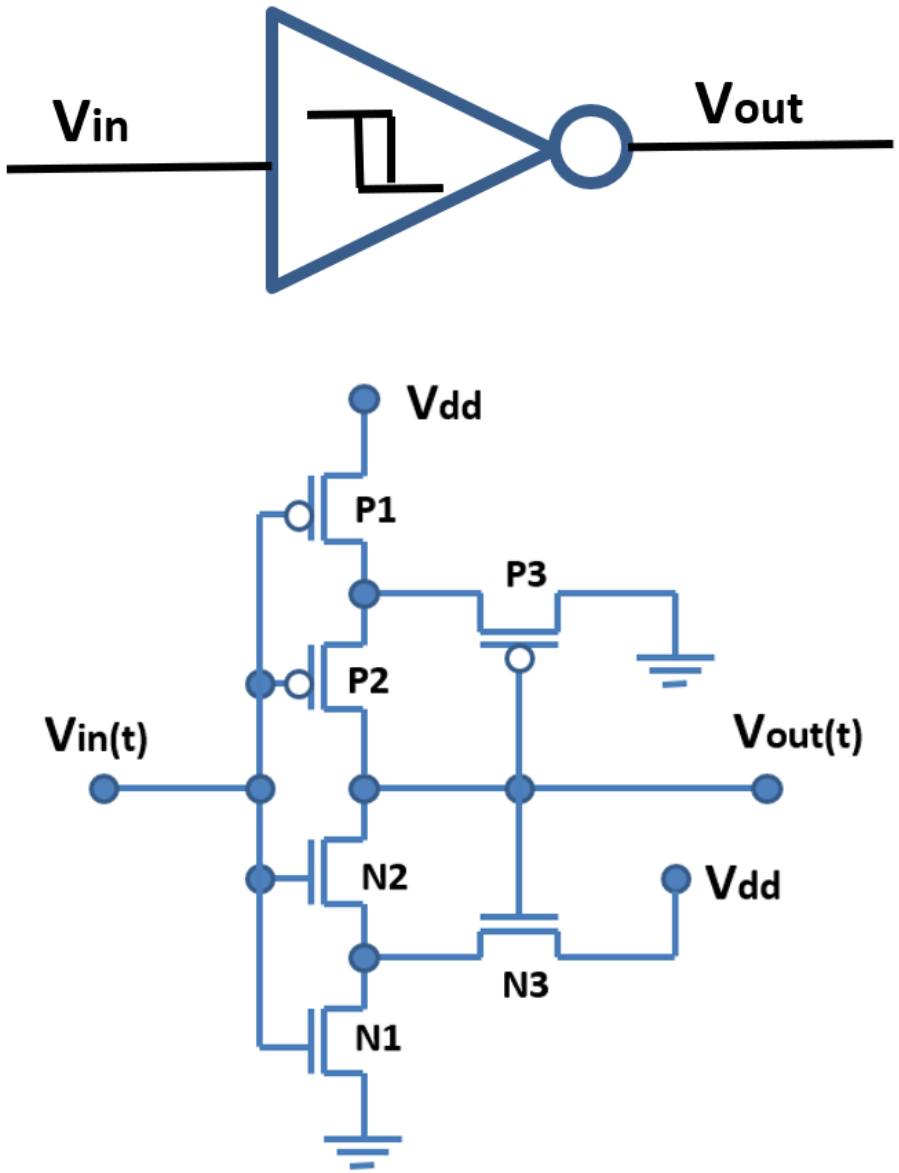
雑音による通常の CMOS inverter 回路 inv( )での誤動作

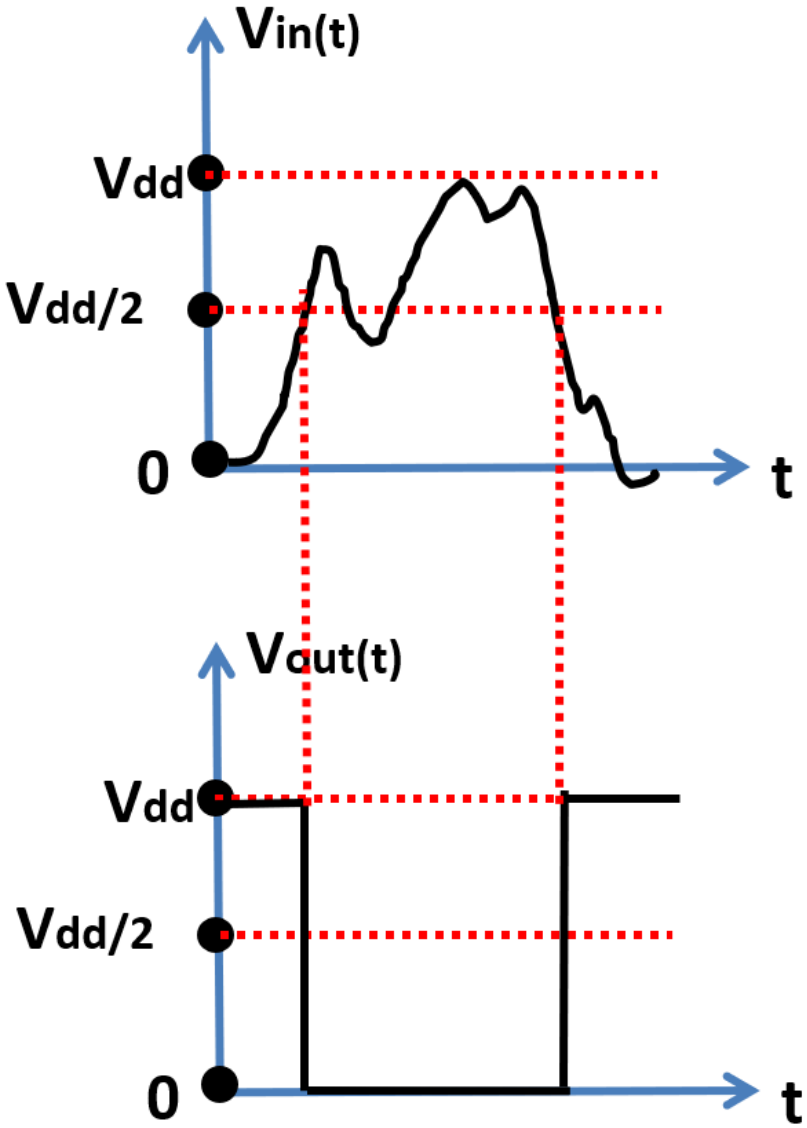
図 4-5-7(2)



CMOS Schmitt Trigger inverter 回路 invSmt( )

図 4-5-7(3)





CMOS Schmitt Trigger inverter 回路 invSmt( )の入出力波形

図 4-5-8

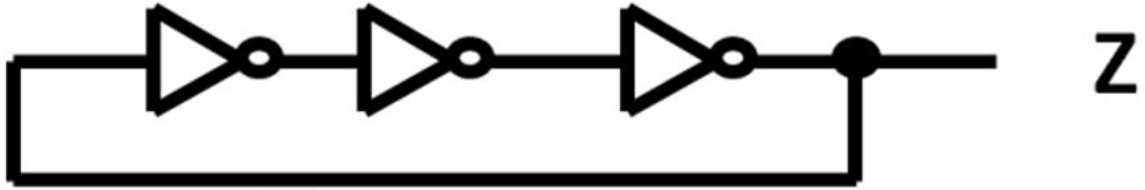
Inverterの信号遅延時間(Delay Time)は ～5nsec.

inv( ) 回路を単純につなげたもの

単純な遅延回路

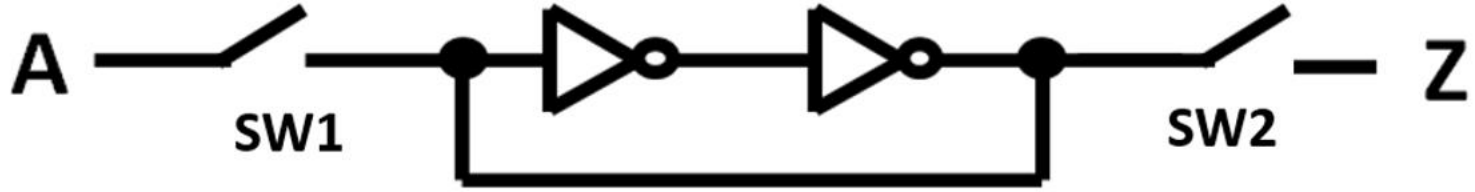
inv( ) 回路を奇数個つなげてFeedbackしたもの。

発振回路



inv( ) 回路を偶数個つなげてFeedbackしたもの。

Memory 回路



CMOS inverter chainを使った応用回路の例

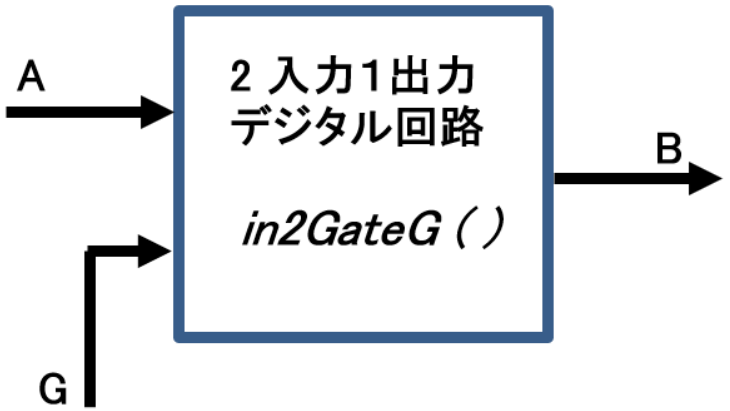
図 4-6-1

DCDL (digital circuit description language) のよる coding 例

in2GateG ( ) 回路の出力Bの値　　for G = 0 ～F

input (G,A)	G =0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
G =0 A= 0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
G= 0 A=1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
G=1 A=0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
G=1 A=1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

AND( )　*EXOR( )*　*OR( )*　*NOR( )*　*EXNOR( )*　*NAND( )*

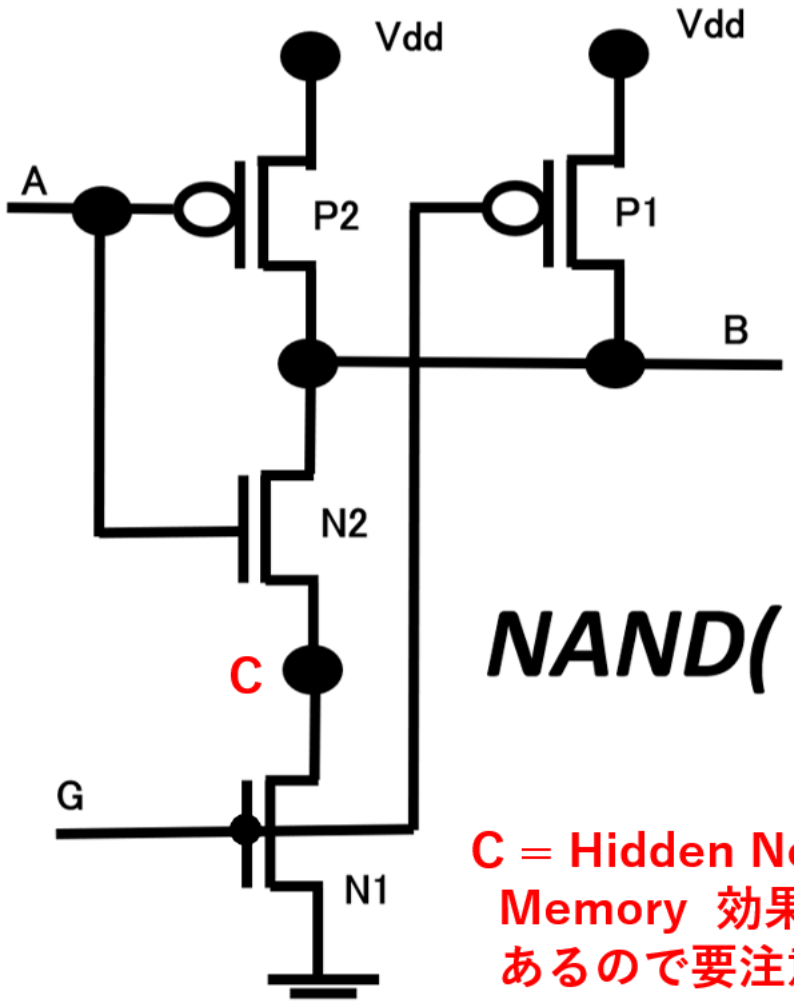


in2Gate1( )=AND( )
in2Gate6( )=EXOR( )
in2Gate7( )=OR( )
in2Gate8( )=NOR( )
in2Gate9( )=EXNOR( )
in2GateE( )=NAND( )

16 種類の 2 入力デジタル回路 in2GateG( ) 回路の DCDL Code定義

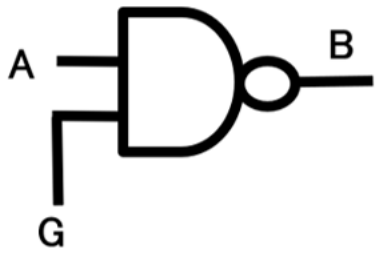
図 4-6-2

DCDL (digital circuit description language) のよる coding 例



NAND( )

C = Hidden Node
Memory 効果が
あるので要注意




```
in2Gate1( )=AND( )
in2Gate6( )=EXOR( )
in2Gate7( )=OR( )
in2Gate8( )=NOR( )
in2Gate9( )=EXNOR( )
in2GateE( )=NAND( )
```

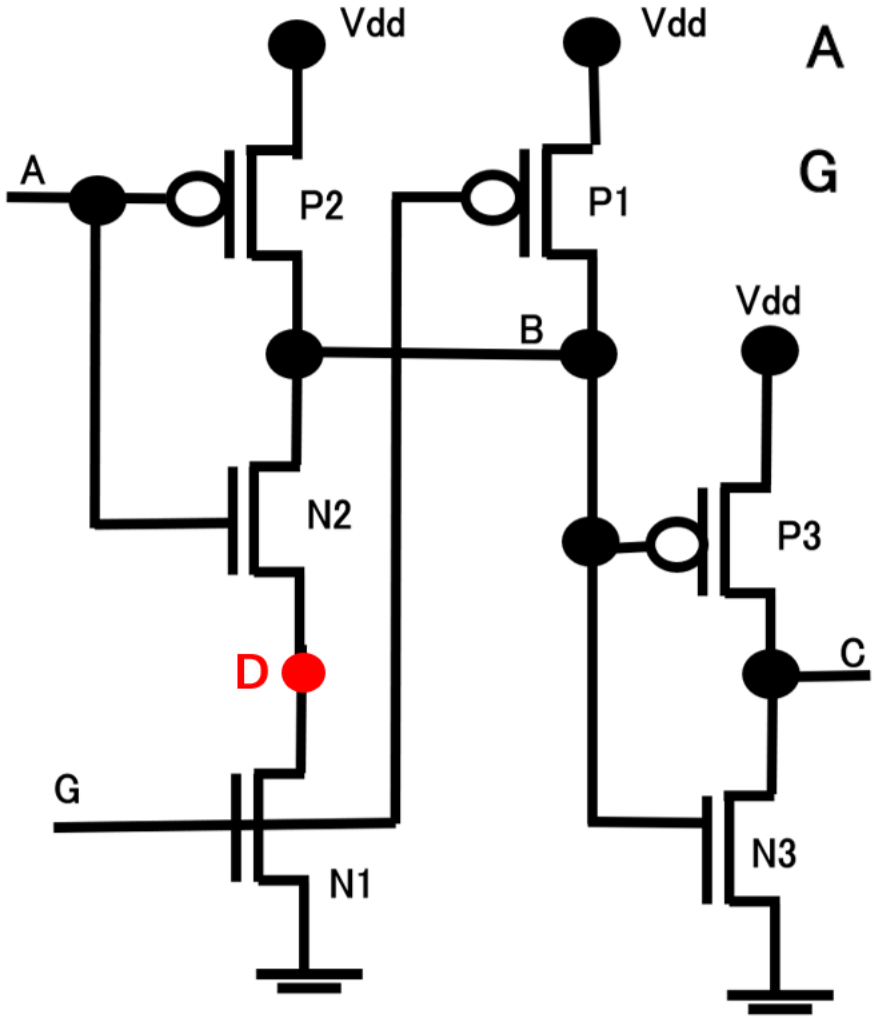
G	A	B
0	0	1
0	1	1
1	0	1
1	1	0

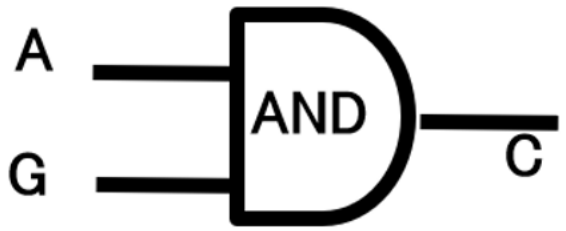
if G = 0 , B = 1;
If G = 1, B =inv(A);

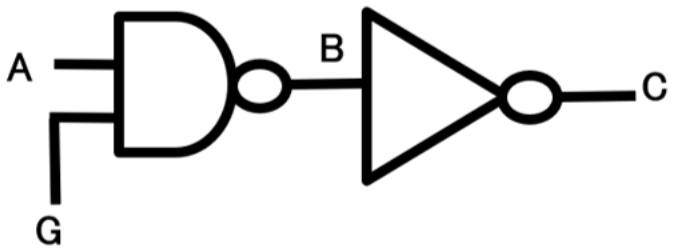
2 入力 CMOS NAND Gate 回路 NAND( )の DCDL Code 定義

図 4-6-3(1)

DCDL (digital circuit description language) のよる coding 例







*NAND( )*inv( )→AND( )*

in2Gate1( )=AND( )
in2Gate6( )=EXOR( )
in2Gate7( )=OR( )
in2Gate8( )=NOR( )
in2Gate9( )=EXNOR( )
in2GateE( )=NAND( )

G	A	B	C
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

if G = 0 , C = 0 ;
If G = 1, C =A ;

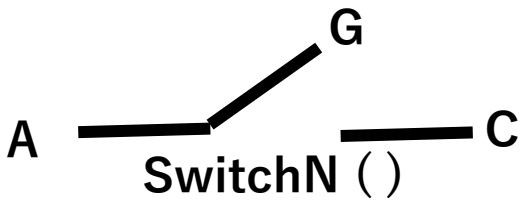
2 入力 CMOS NAND Gate 回路 NAND( )の DCDL Code 定義

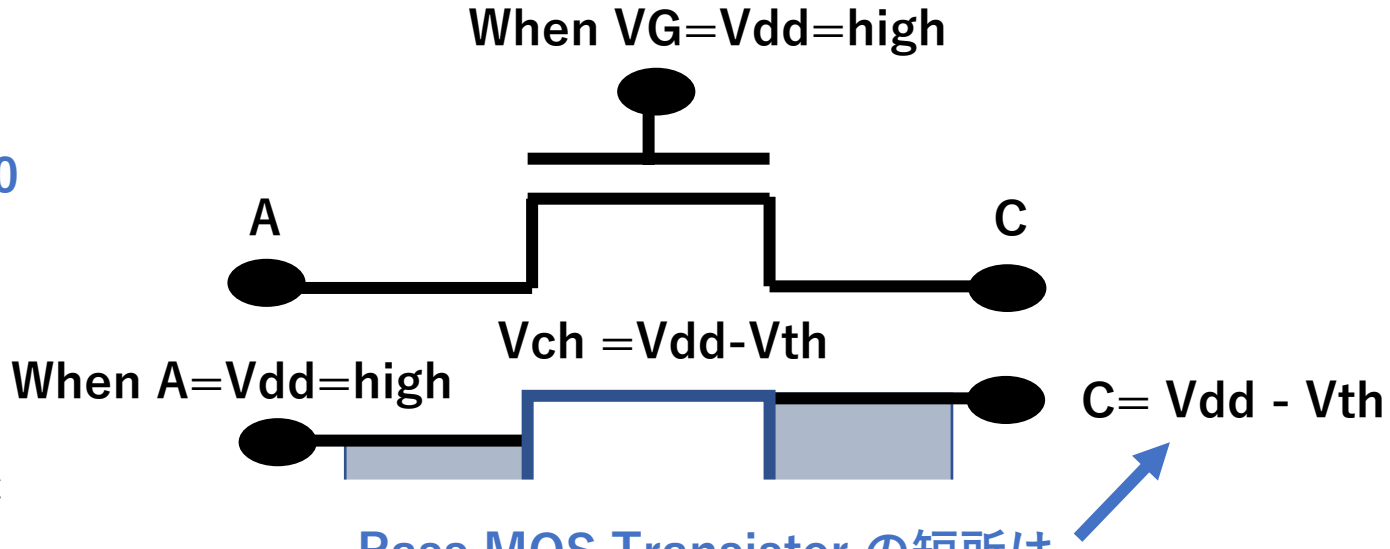
図 4-6-3(2)

SwitchN( ) 回路の定義

High=1 Low=0

VG	A	C
0	0	?
0	1	?
1	0	0
1	1	1





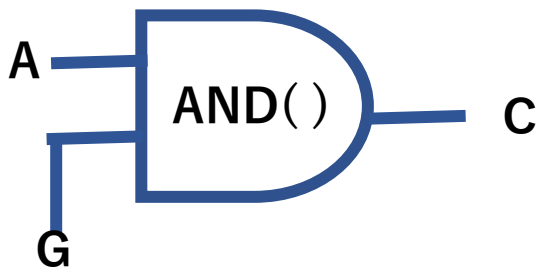
Pass MOS Transistor の短所は、
出力端子 C が 1 になりきらない。

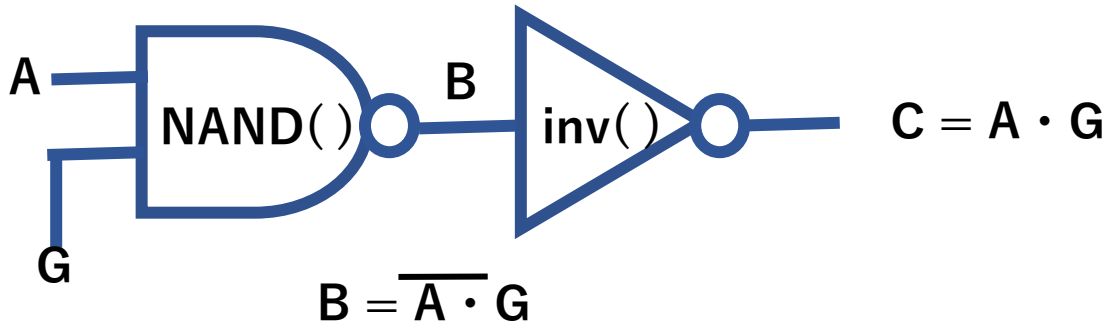
CMOS回路の長所は出力電圧が接地GNDと電源Vddの値まではっきり定まる事

AND( ) 回路の定義

G	A	C
0	0	0
0	1	0
1	0	0
1	1	1

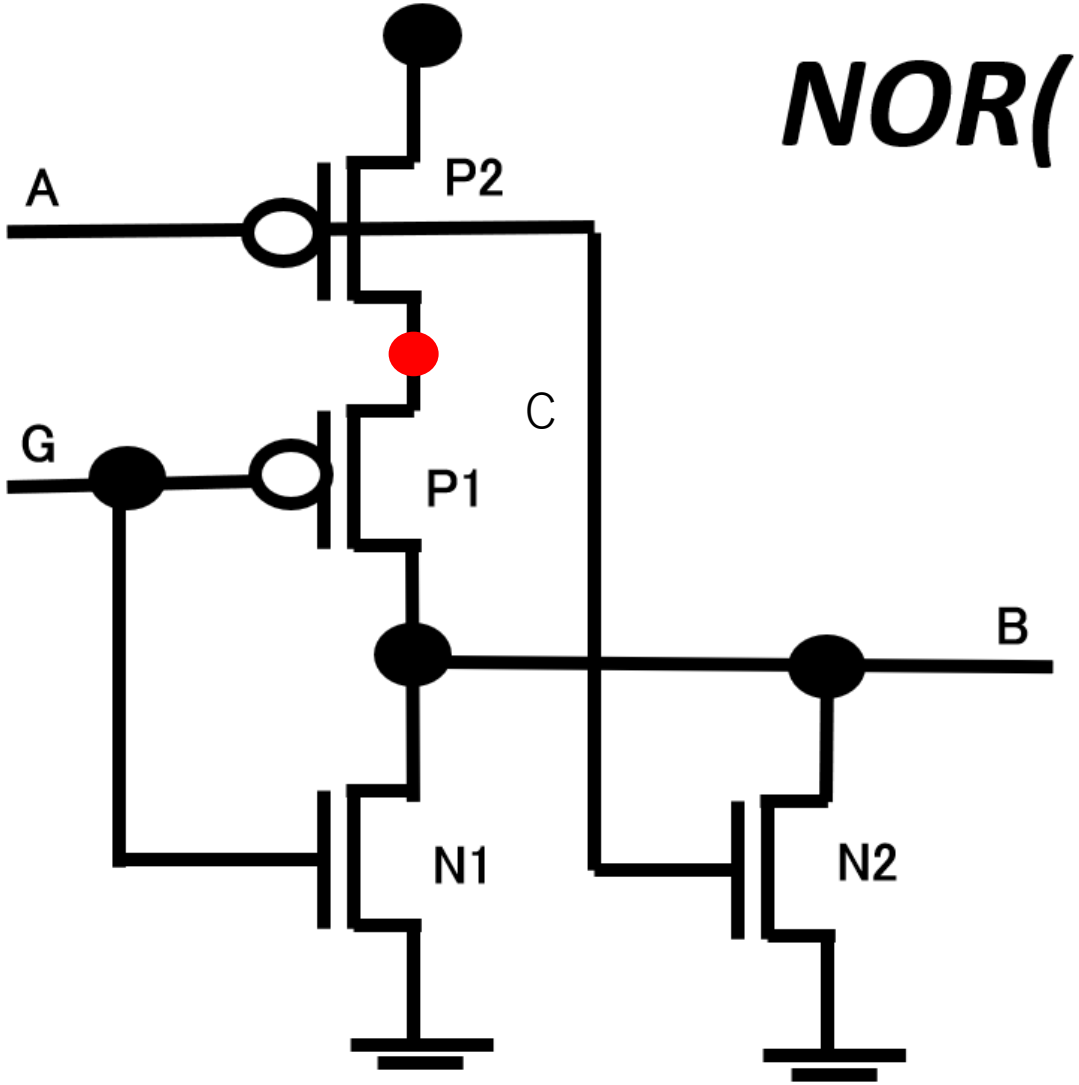
NAND( )*inv( )→AND( )



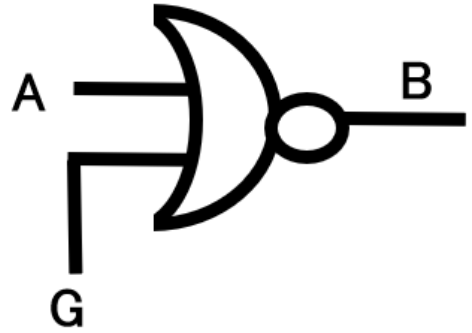


AND( )回路とSwitchN( )回路の比較

図 4-6-4



NOR( )

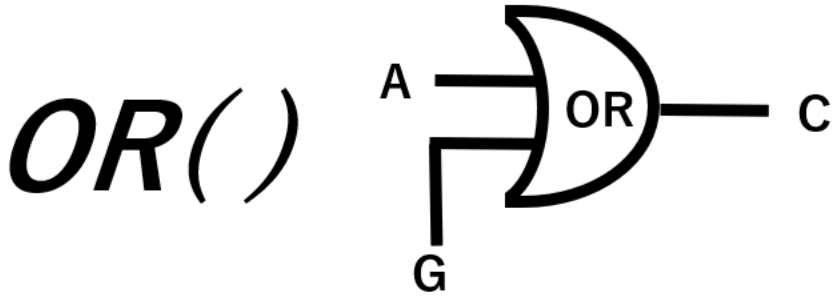


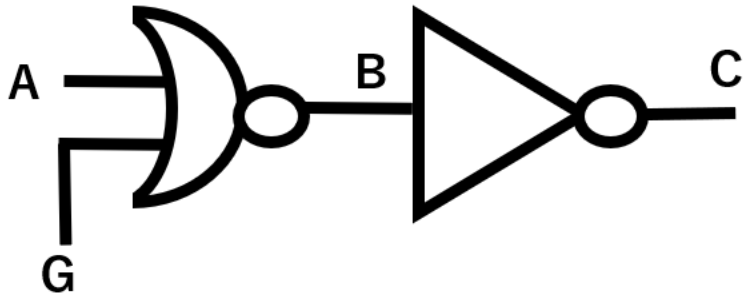
G	A	B
0	0	1
0	1	0
1	0	0
1	1	0

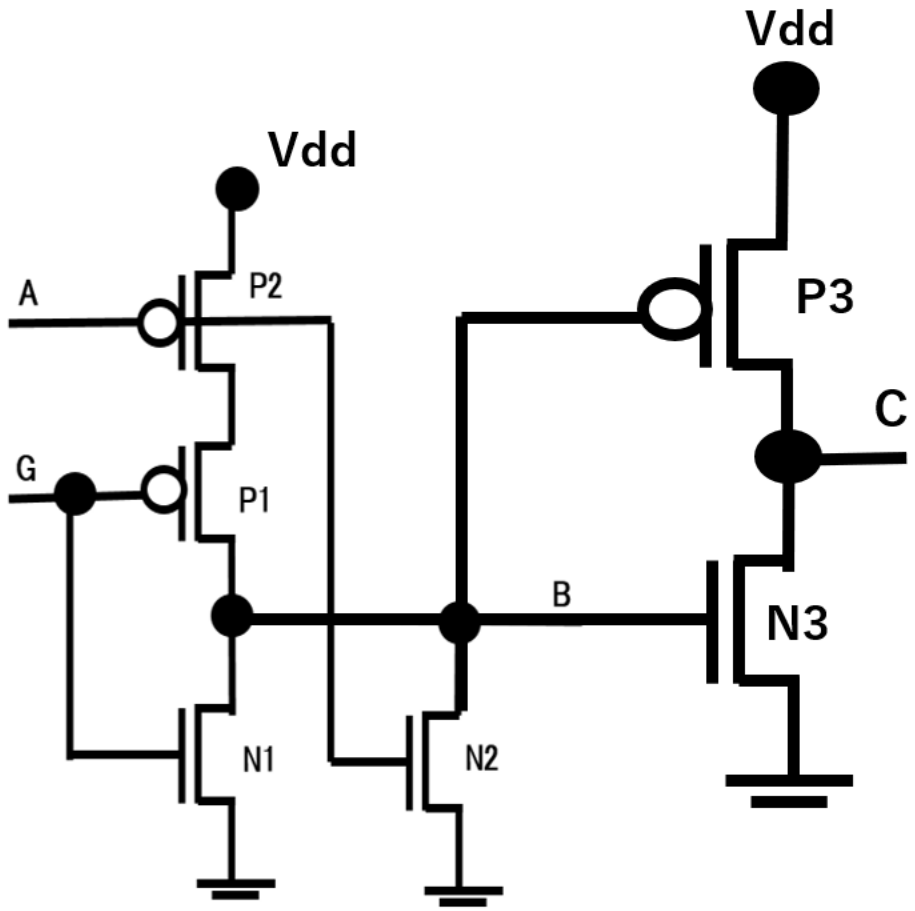
if G = 0 , B = inv ( ) [A] ;
If G = 1, B = 0 ;

CMOS NOR Gate 回路 **NOR( )**の定義

図 4-6-5







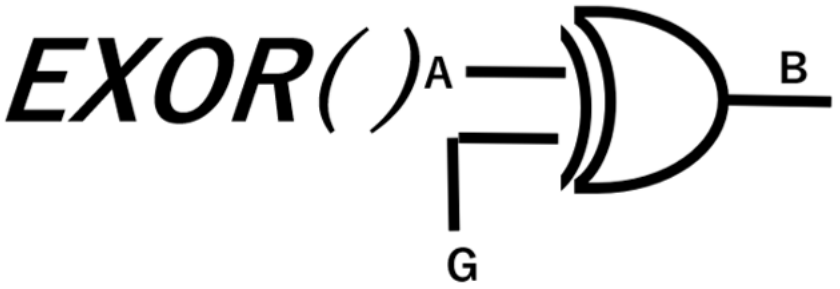
NOR( ) inv( ) → OR( )

G	A	B	C
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

if G = 0 , C = A ;
If G = 1, C = 1 ;

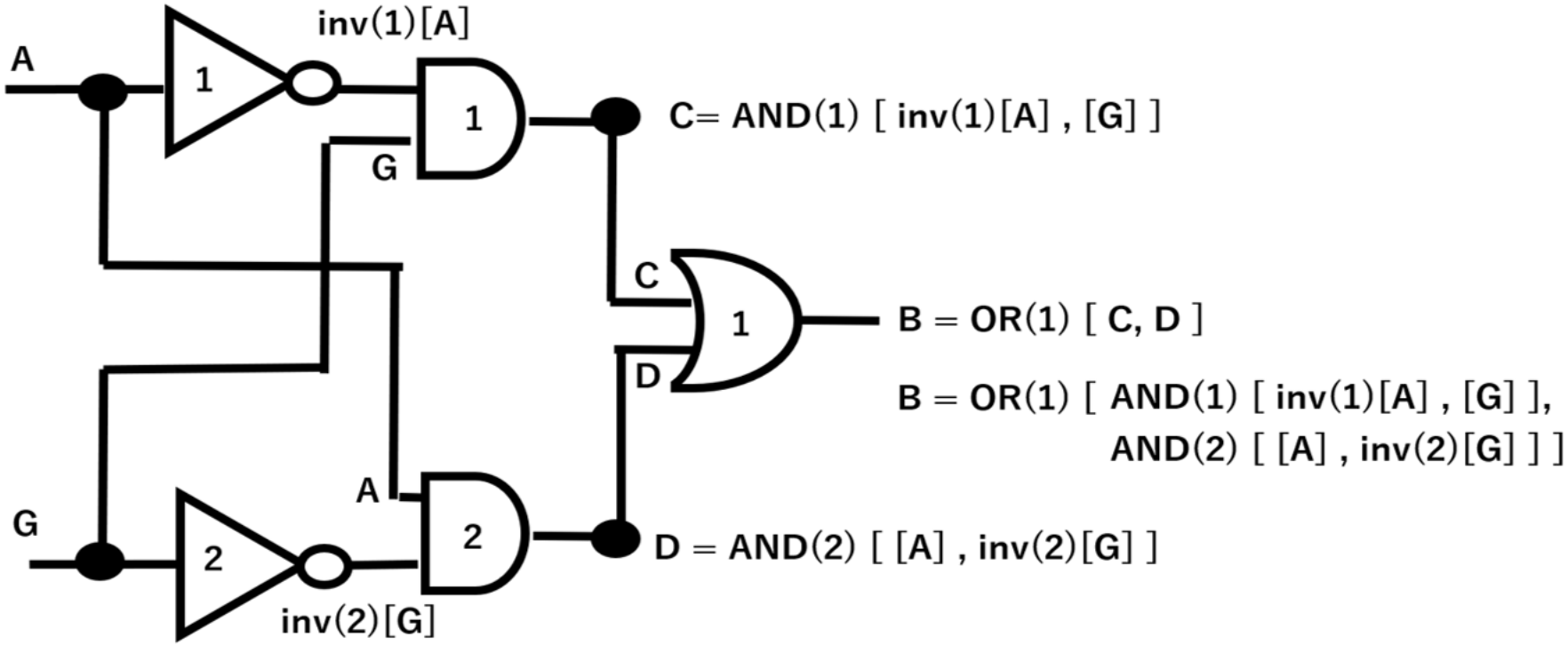
CMOS OR Gate 回路 **OR( )**の定義

図 4-6-6



G	A	B
0	0	0
0	1	1
1	0	1
1	1	0

DCDL (digital circuit description language) のよる coding 例

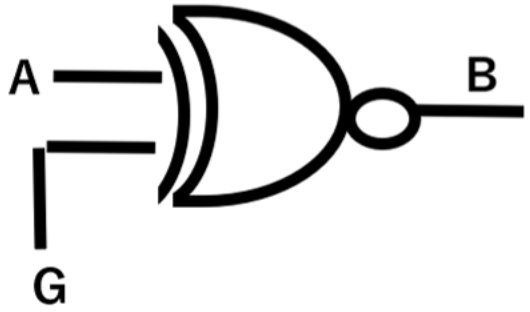


CMOS Exclusive OR Gate回路 **EXOR( )**の定義

図 4-6-7

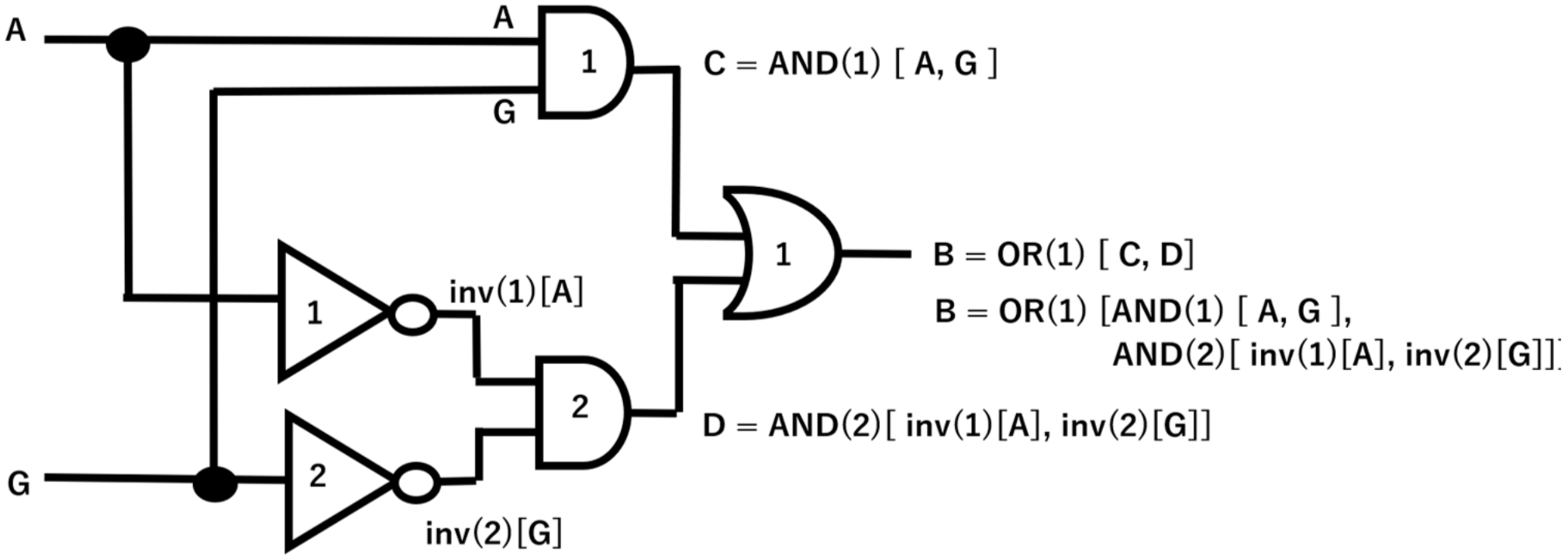
EXNOR( )

1 bit Data の一致回路



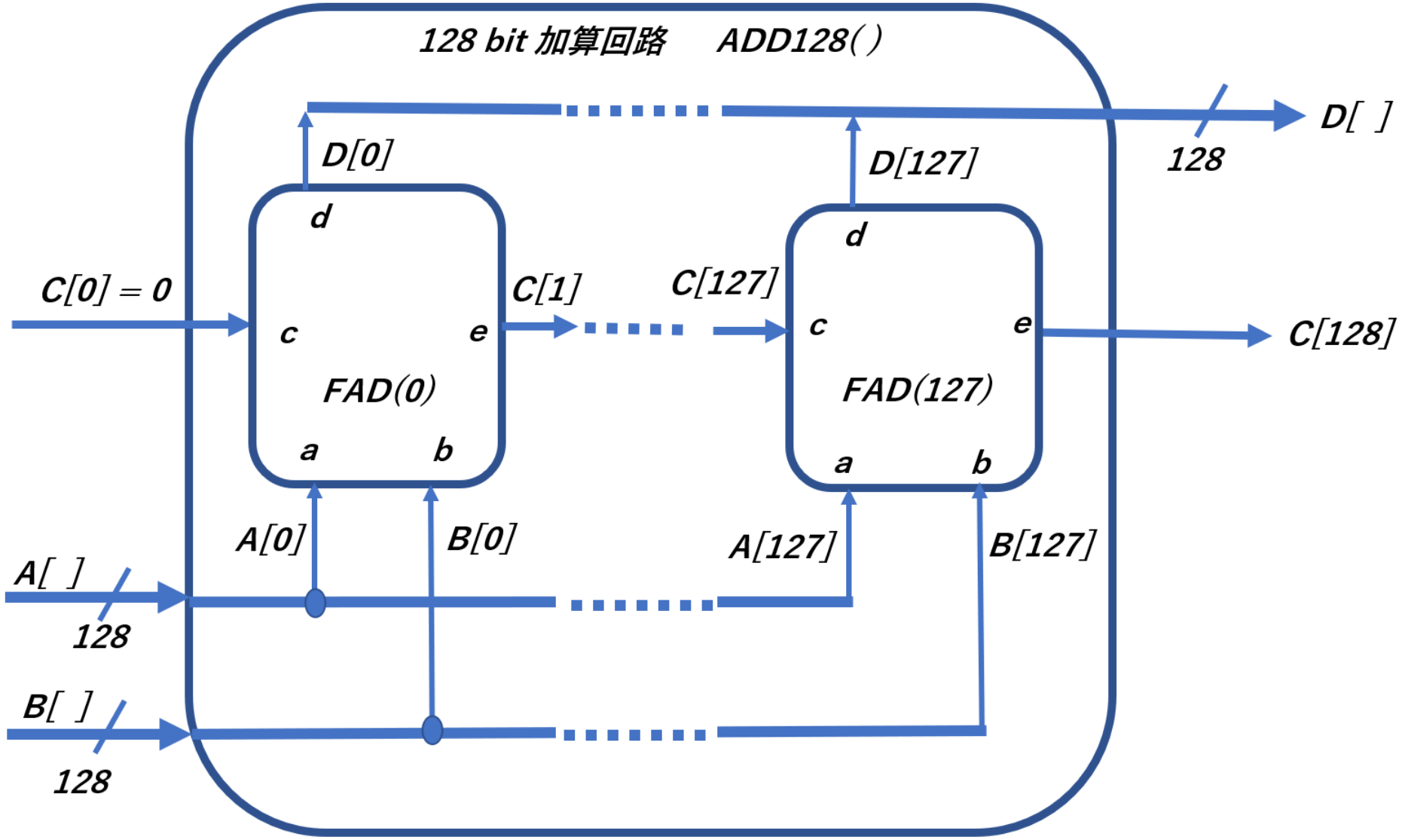
G	A	B
0	0	1
0	1	0
1	0	0
1	1	1

DCDL (digital circuit description language) のよる coding 例



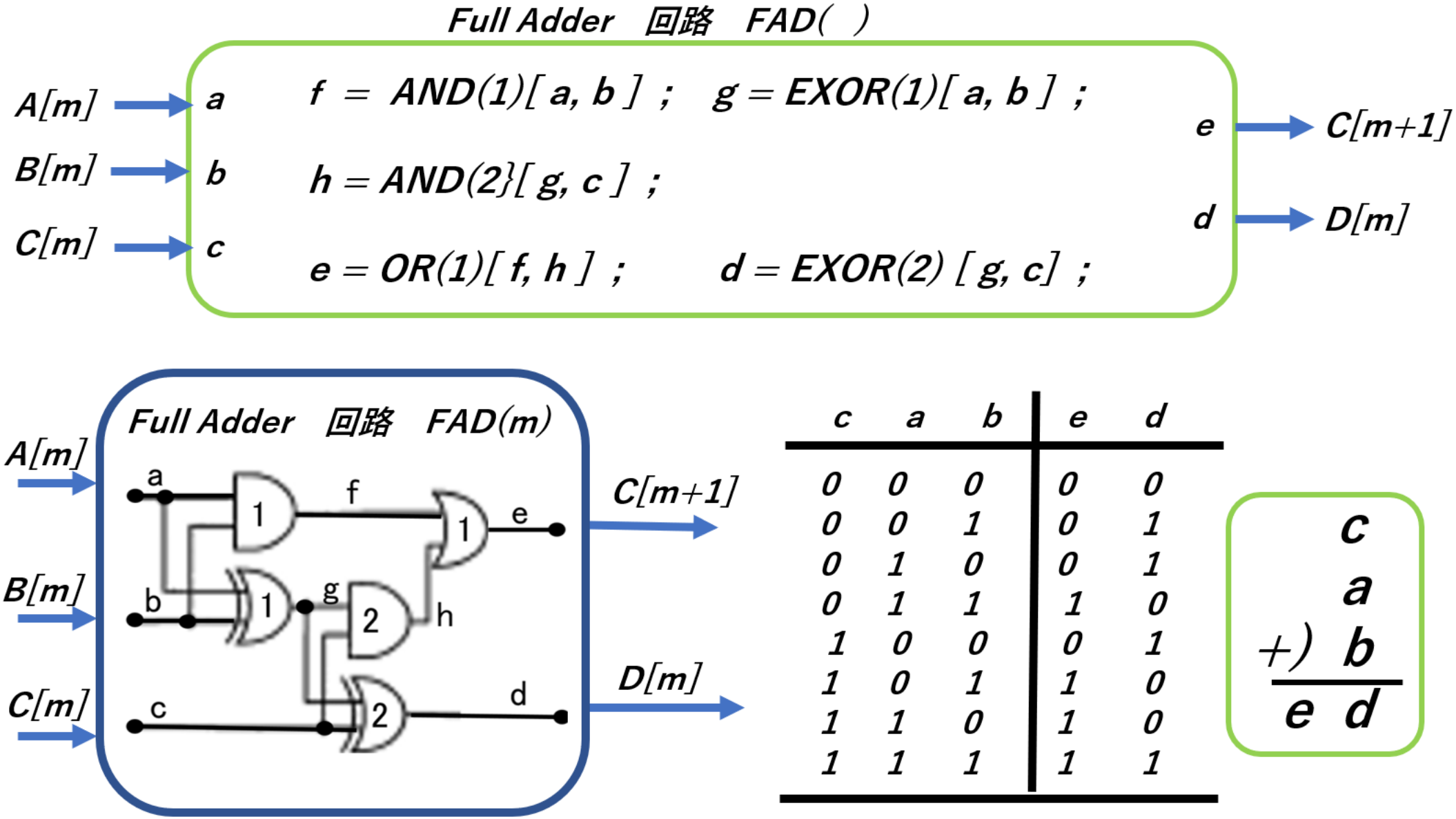
CMOS Exclusive NOR Gate回路 **EXNOR( )**の定義

図 4-7-1



128 bit 加算回路　ADD128 ( ) のイメージ図

図 4-7-2

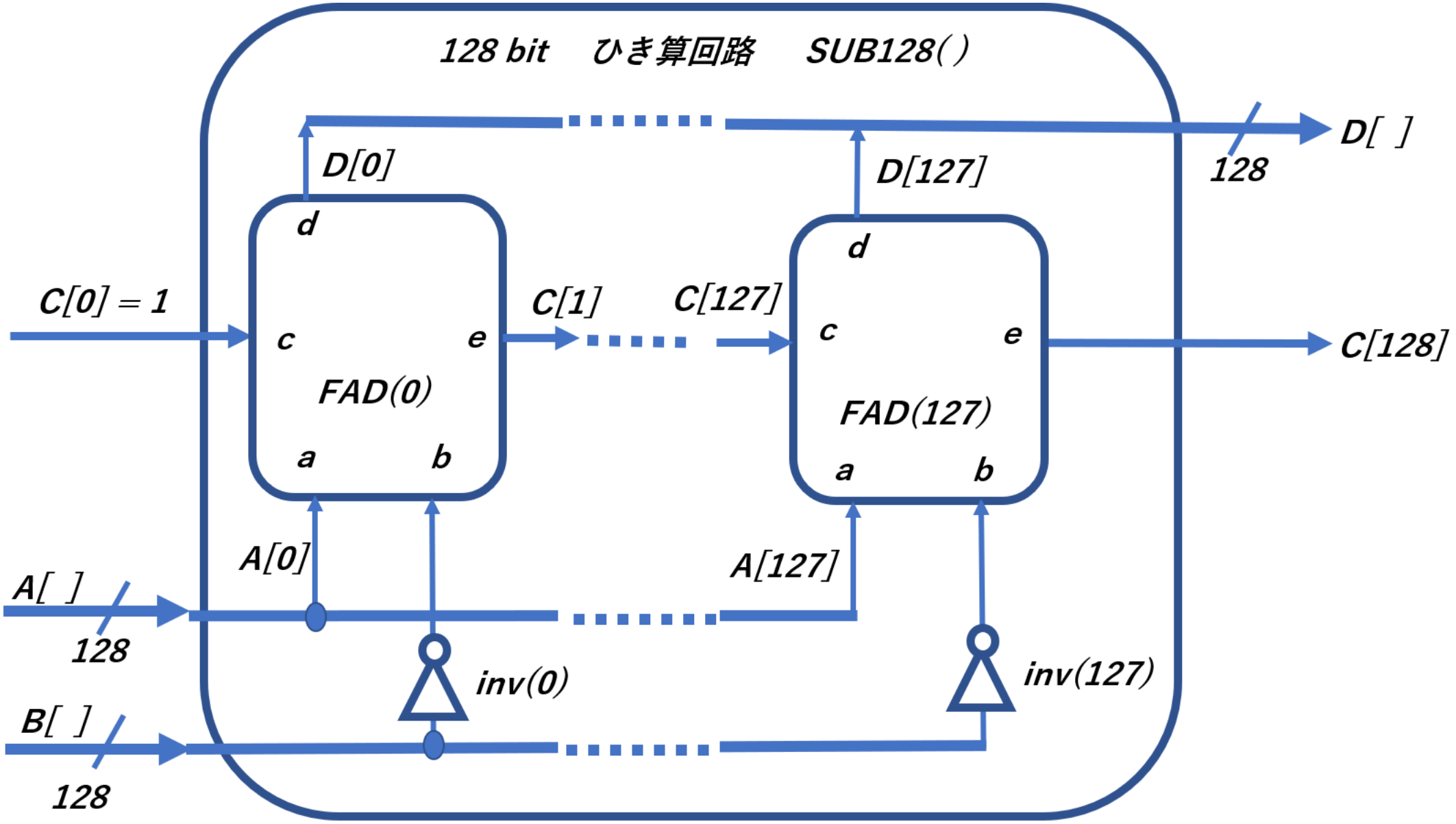


c	a	b	e	d
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$\begin{array}{rr} & c \\ & a \\ +) & b \\ \hline & e\ d \end{array}$$

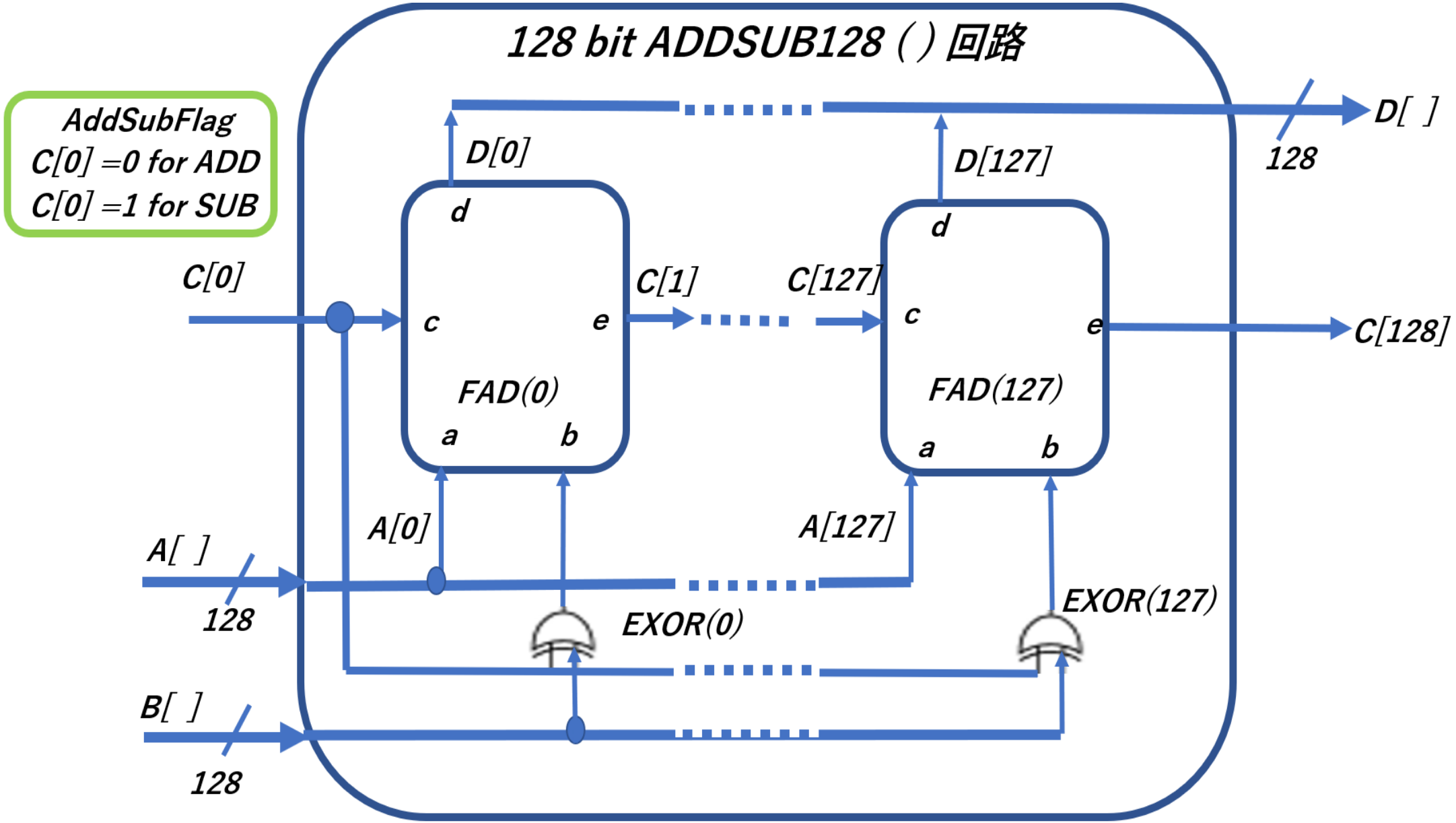
Full Adder 回路　FAD( ) の定義

図 4-7-3



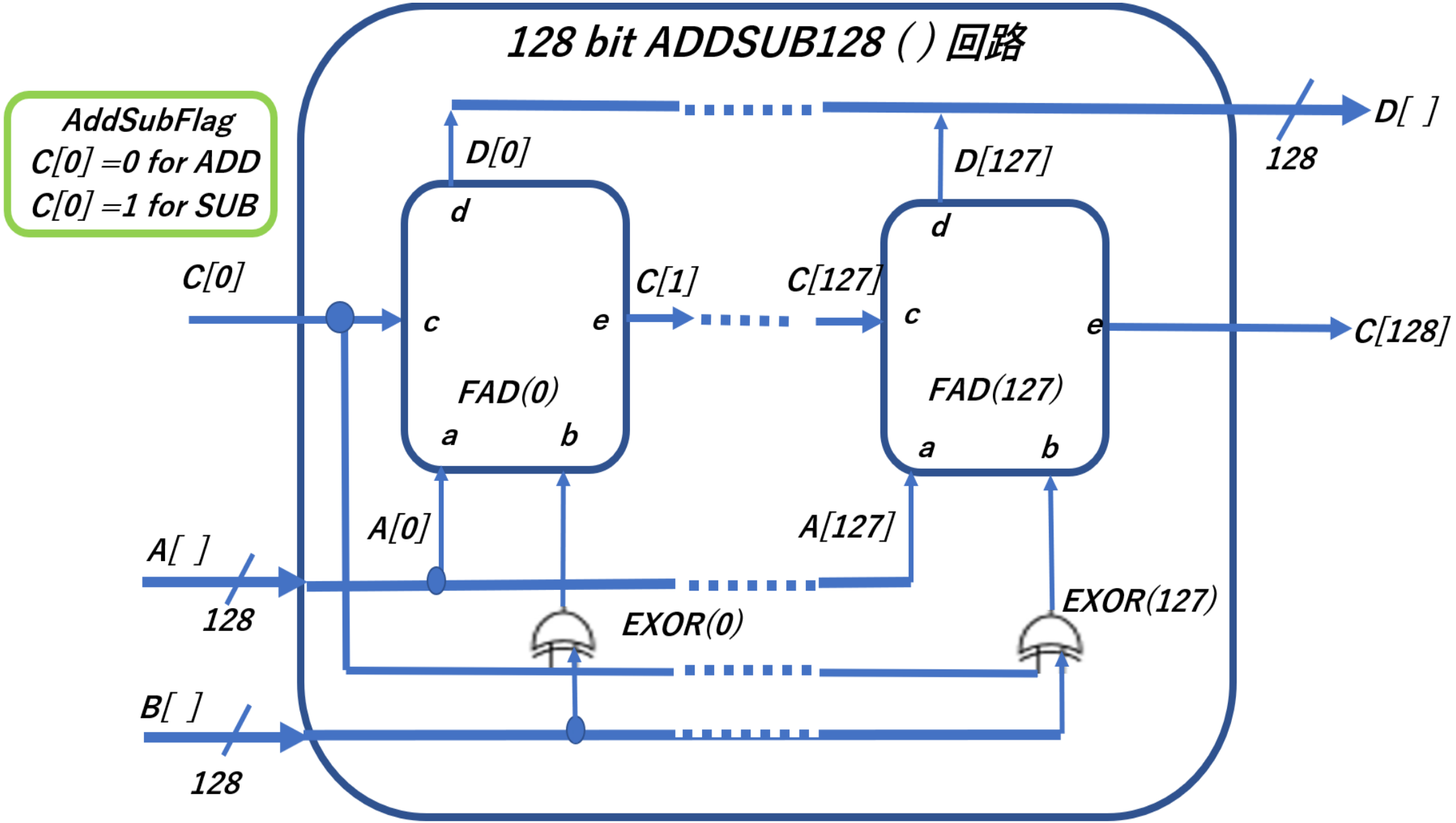
128 bitひき算回路　SUB128 ( ) のイメージ図

図 4-7-4



128 bit加減算回路　ADDSUB128 ( ) のイメージ図

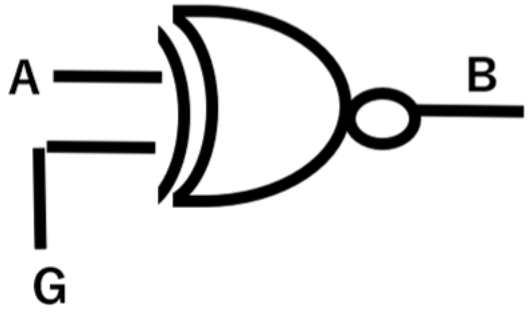
図 4-7-4



128 bit 比較回路　Compare128 ( ) のイメージ図

図 4-6-7

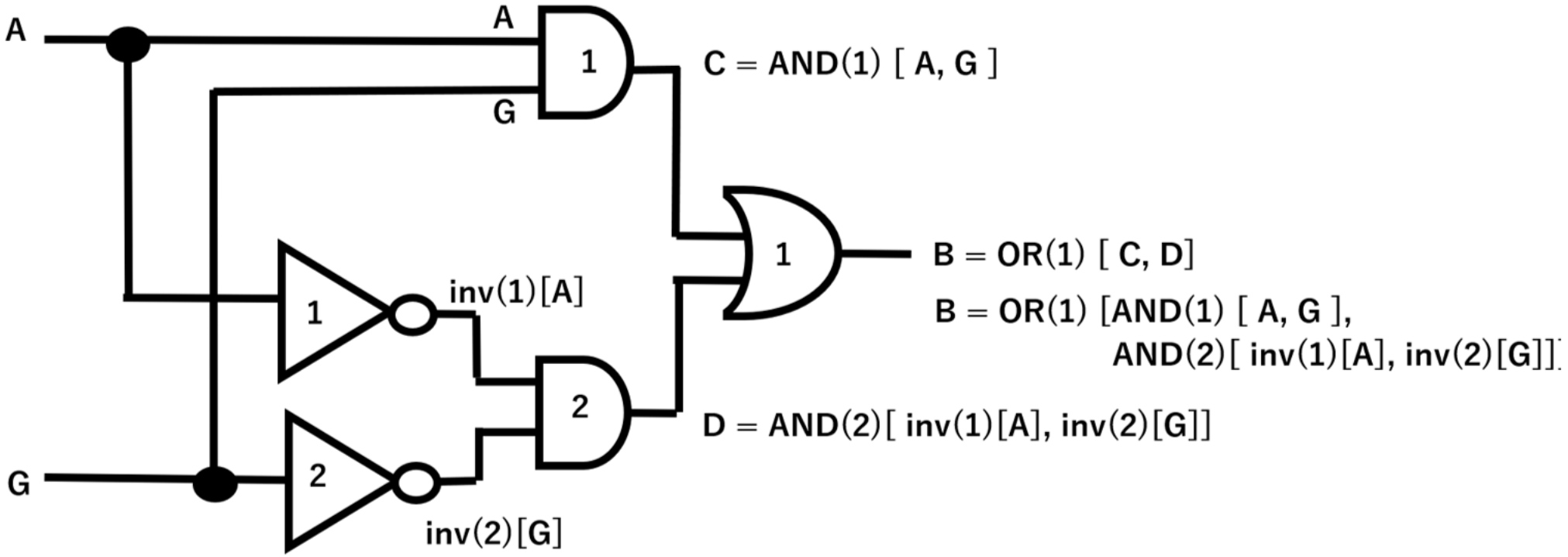
EXNOR( )



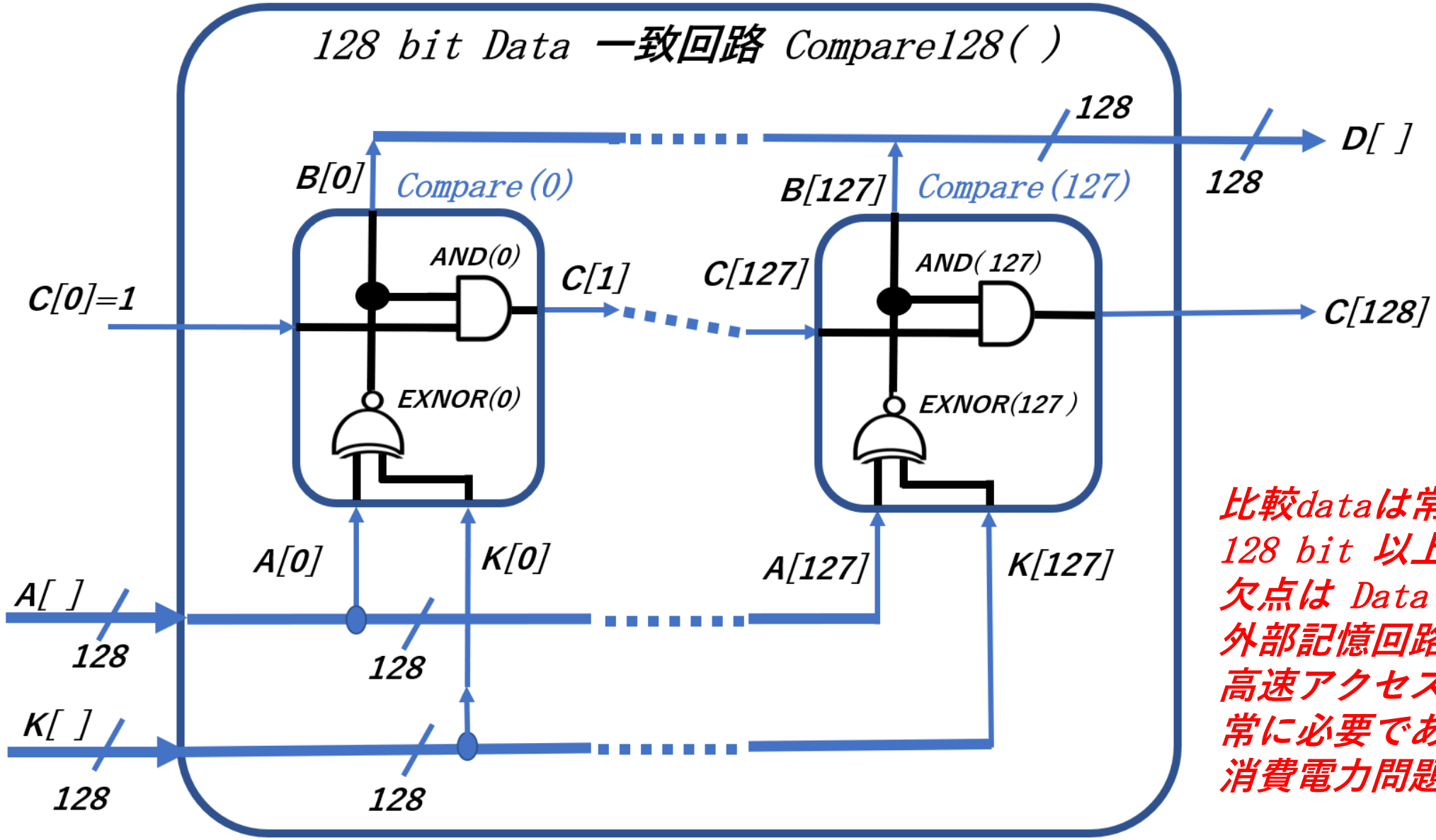
G	A	B
0	0	1
0	1	0
1	0	0
1	1	1

1 bit Data の一致回路

DCDL (digital circuit description language) のよる coding 例



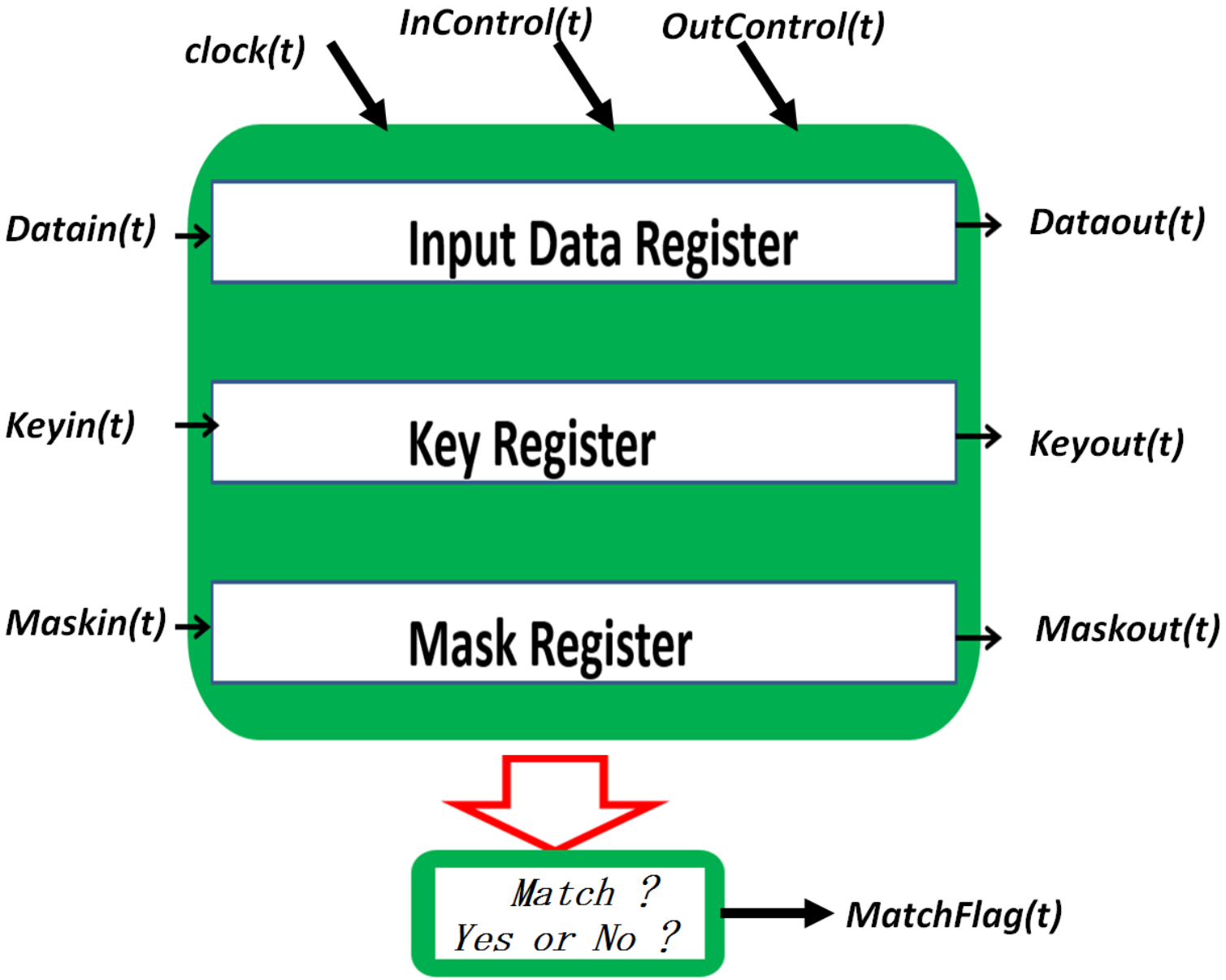
CMOS Exclusive NOR Gate回路 **EXNOR( )**の定義



比較dataは常に
128 bit 以上。
欠点は Data を
外部記憶回路から
高速アクセスが
常に必要である。
消費電力問題。

Data A[ ] と Key Data K[ ]の 一致照合を高速実行する回路

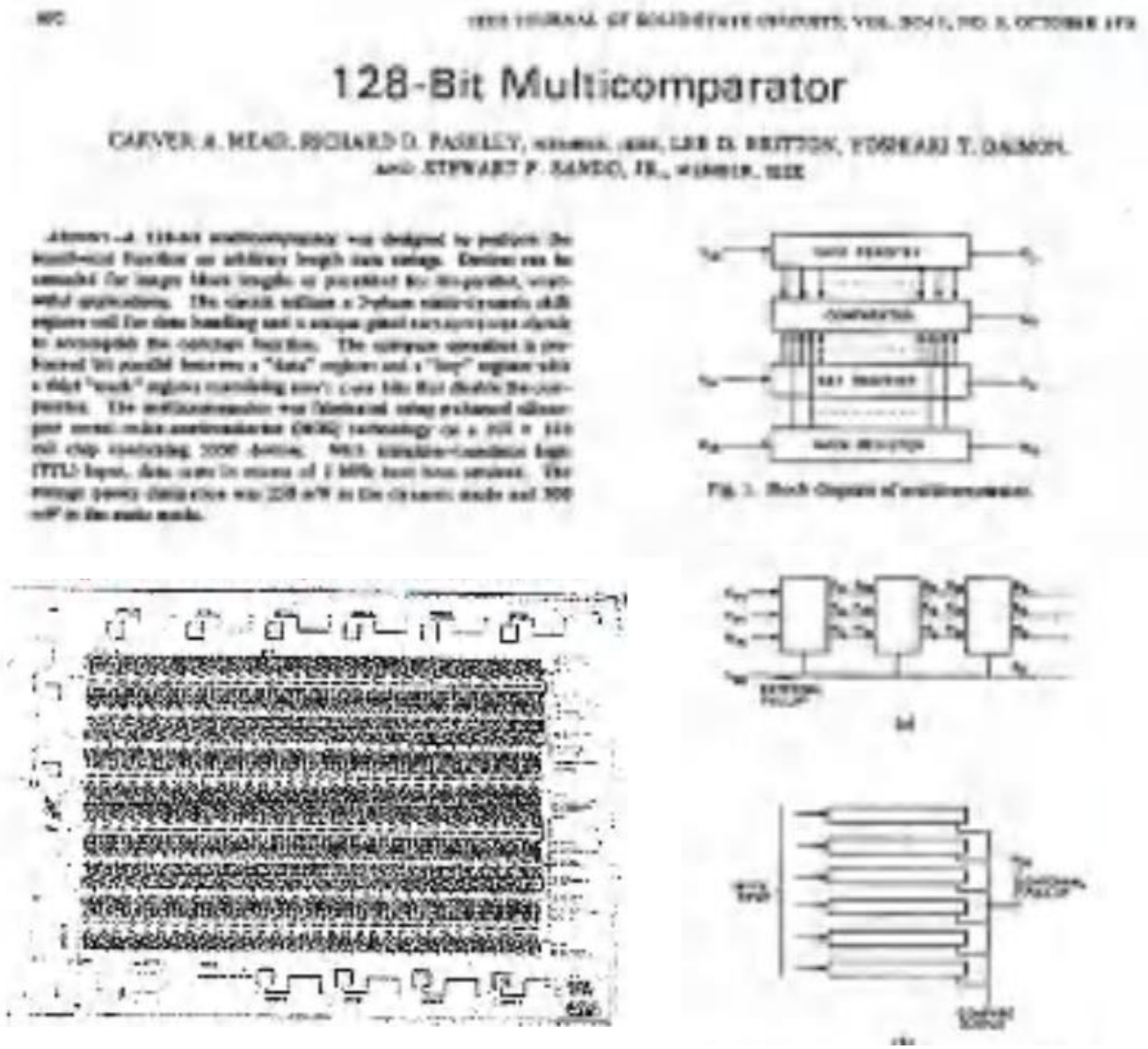
図 1-6-2(1)



128 bit 比較回路の単純機能の定義

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976



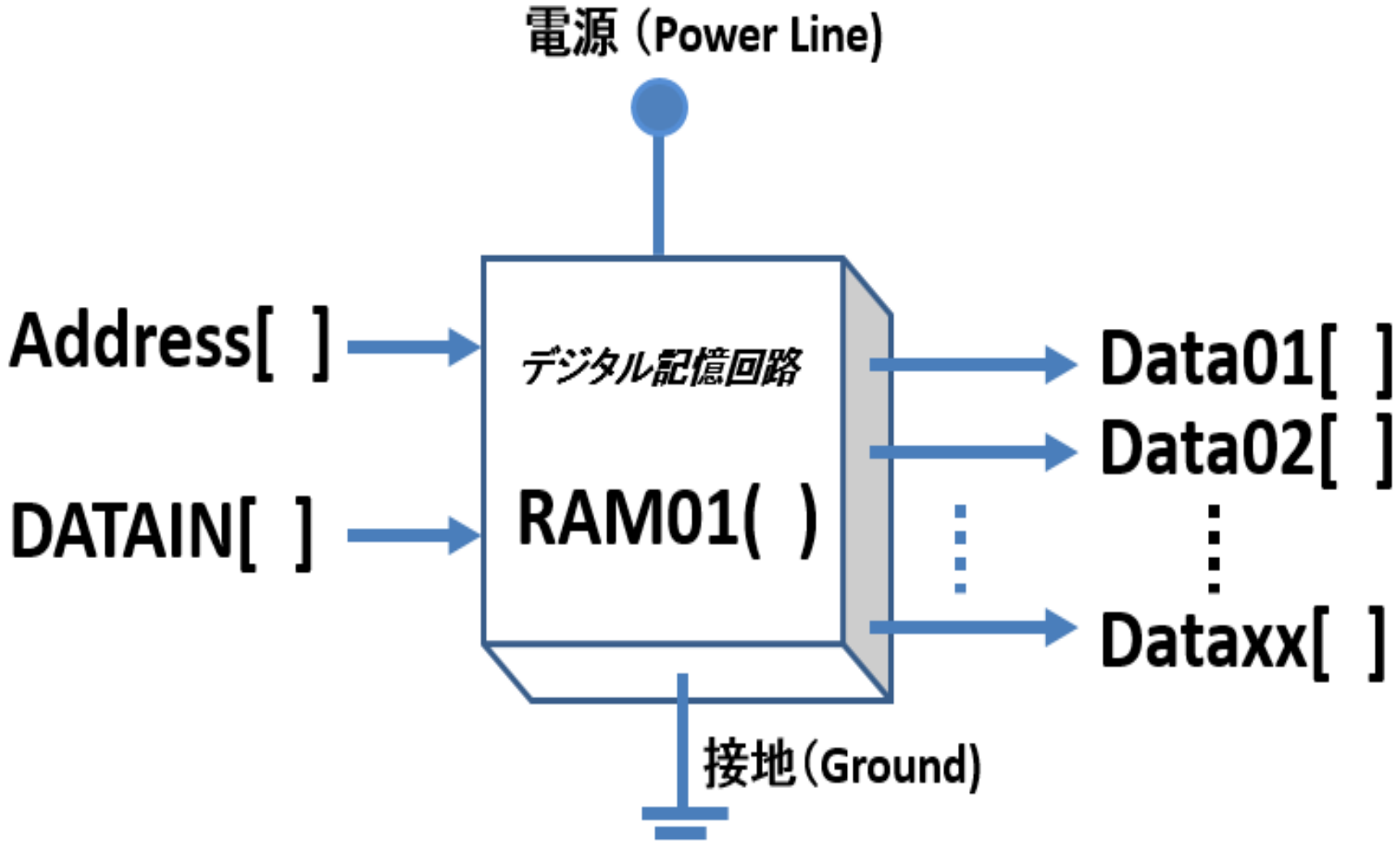
128-Bit Multicomparator

CARVER A. MEAD, RICHARD D. PASLEY, [illegible], LEE D. BRITTON, YOSHIAKI T. DAIMON, AND STEWART F. SANDO, III, [illegible]

Prof. C. A. Mead and Yoshiaki Daimon Hagiwara working on the silicon chip design at Caltech in 1972

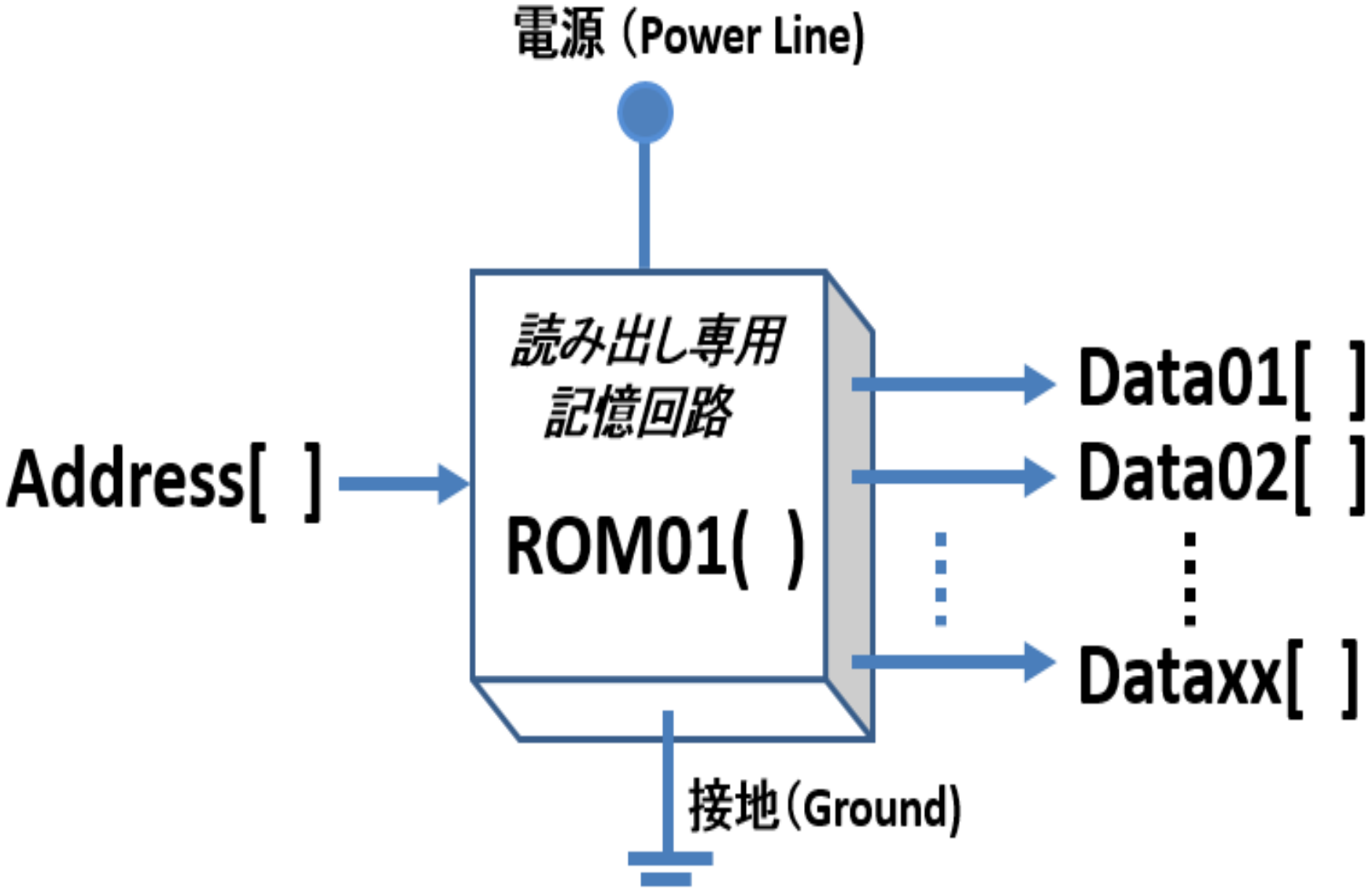
128-bit Multicomparator chip, designed by Hagiwara in 1972-1973 and fabricated by Intel PMOS process.

図 1-5-18



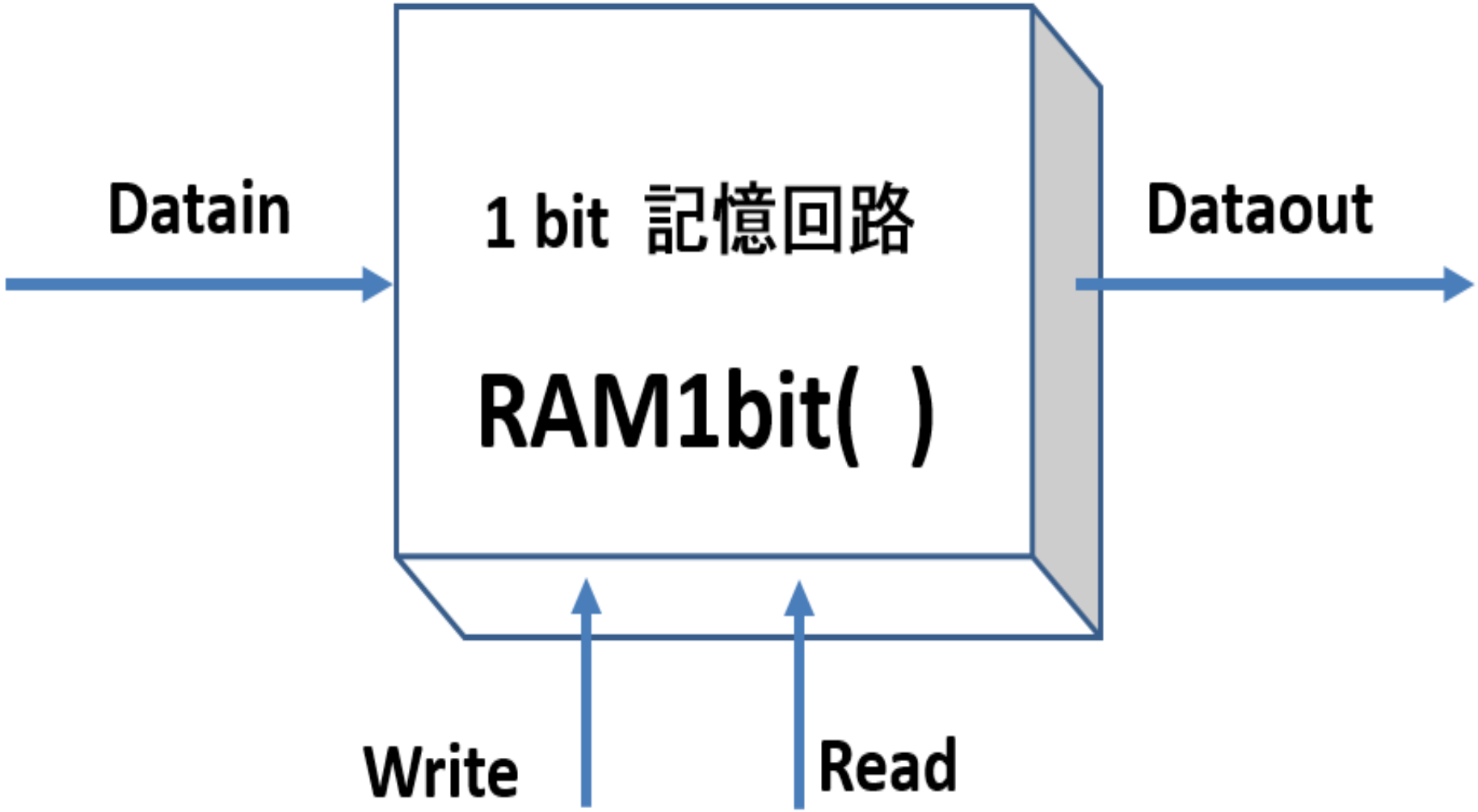
複数個のdataを記憶保存してくれる記憶回路

図 1-5-19



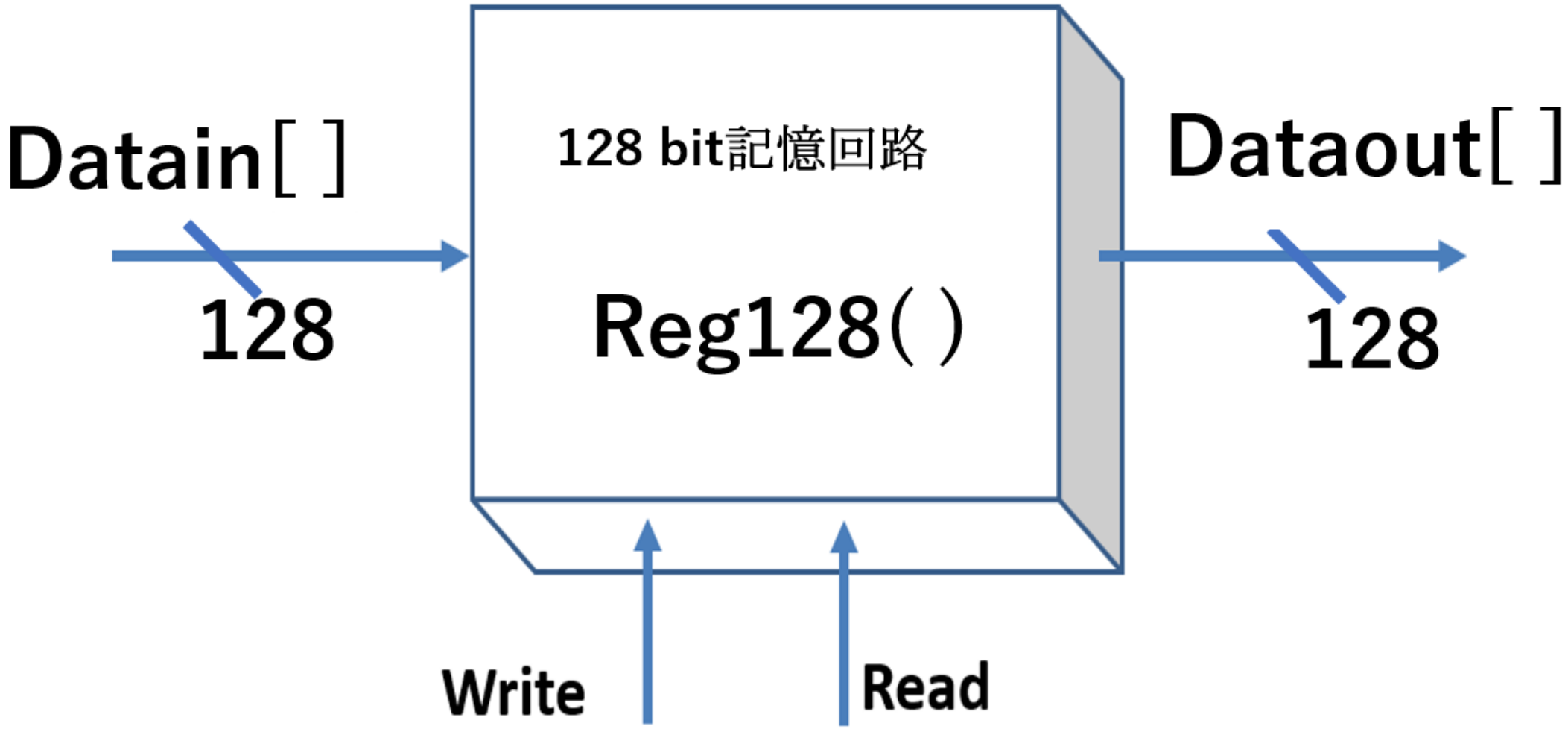
読み出し専用記憶回路　ROM01( )

図 1-5-20



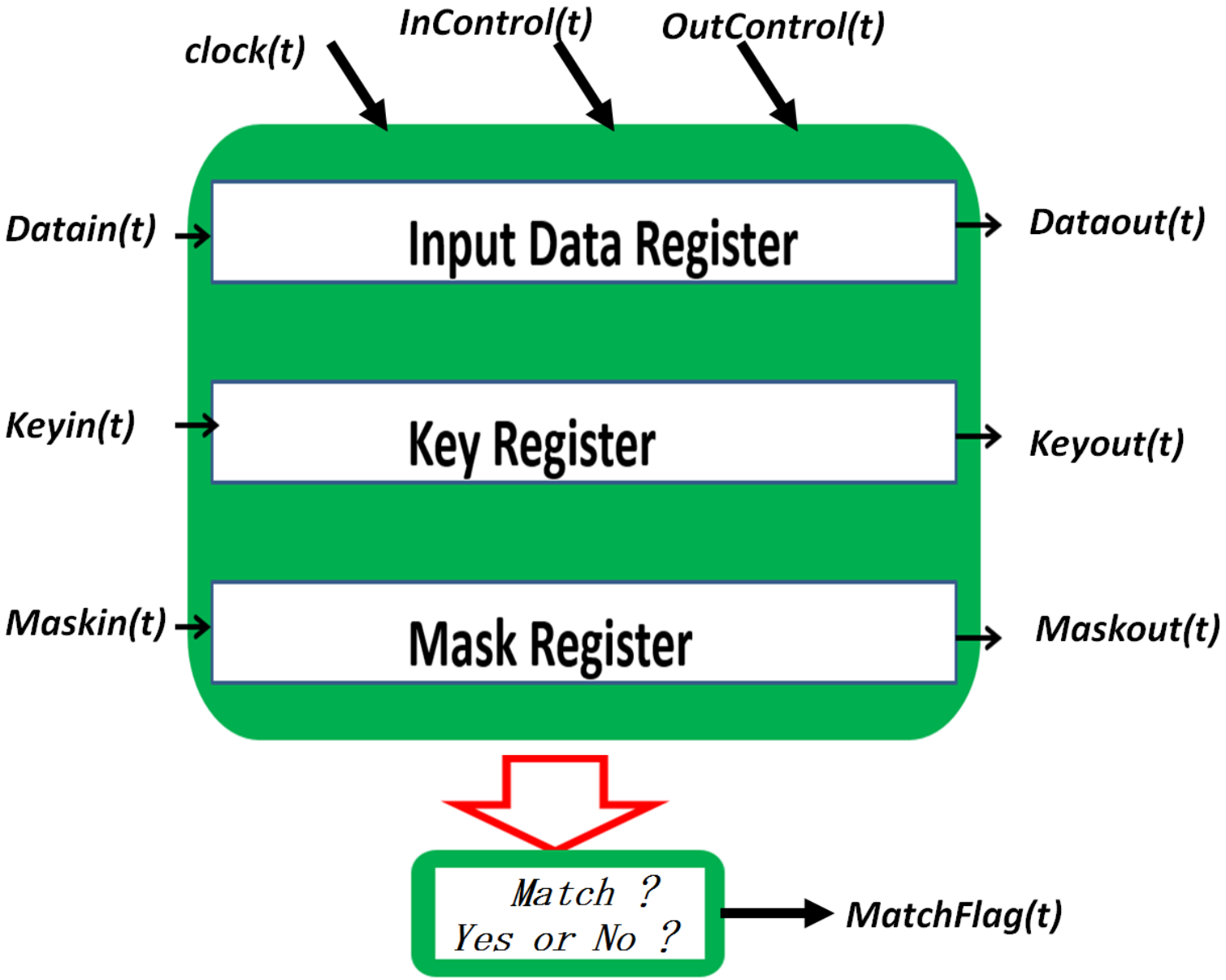
1 bit 記憶する回路　RAM1bit( ) 回路

図 1-5-21



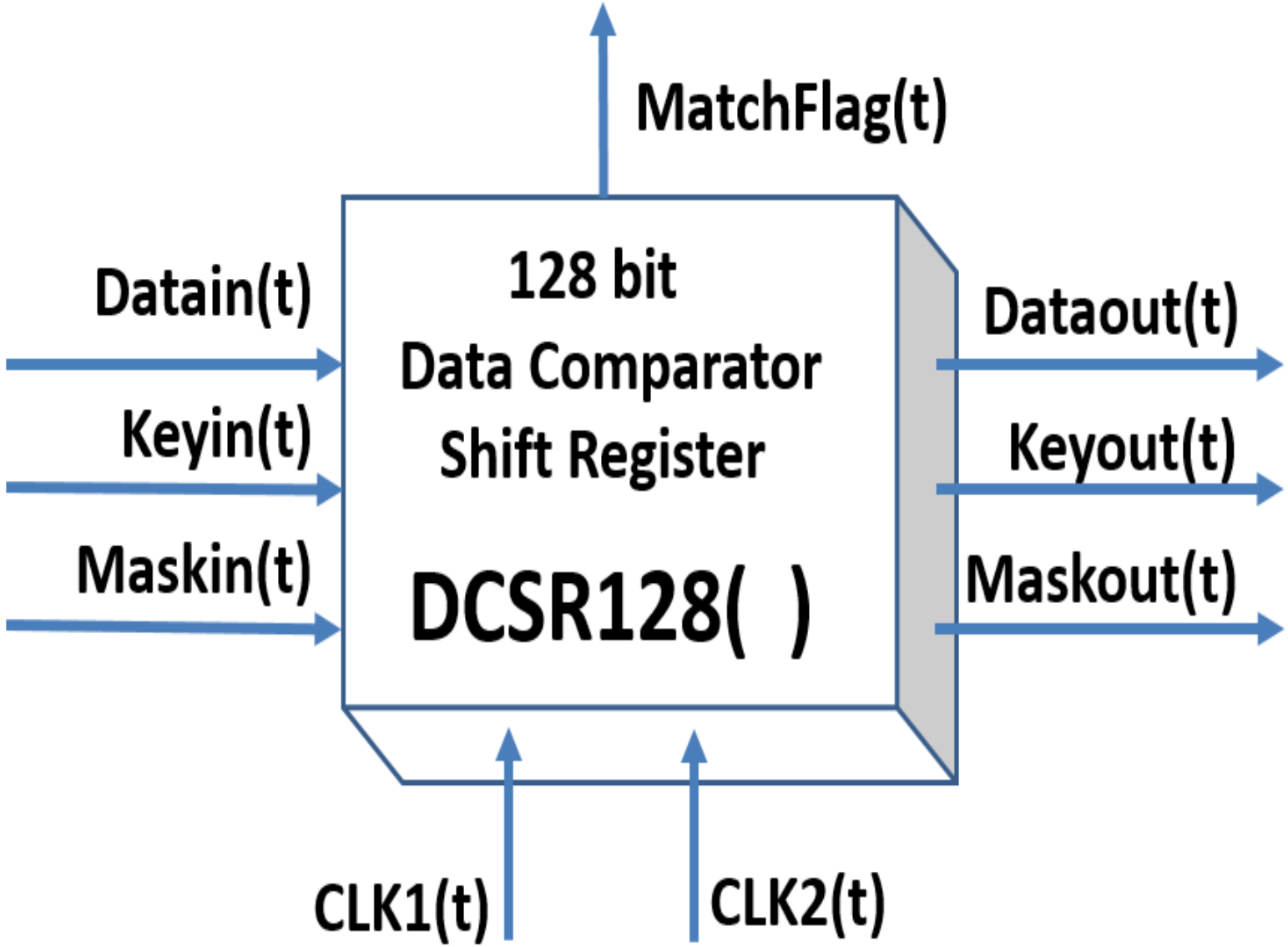
一時的に128　bit 記憶登録する回路　Reg128 ( ) 回路

図 1-6-2(1)



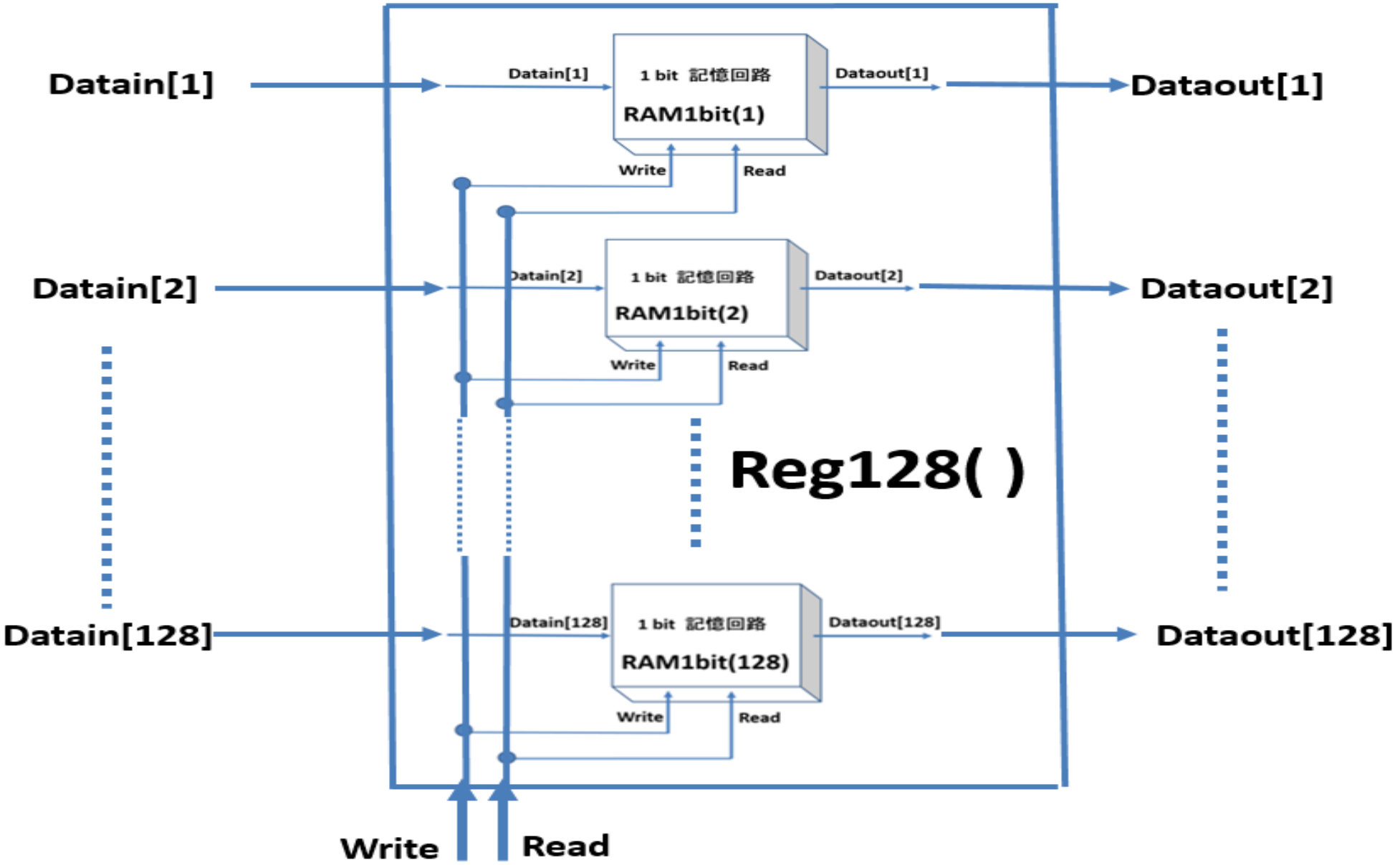
128 bit 比較回路の単純機能の定義

図 1-6-2(2)



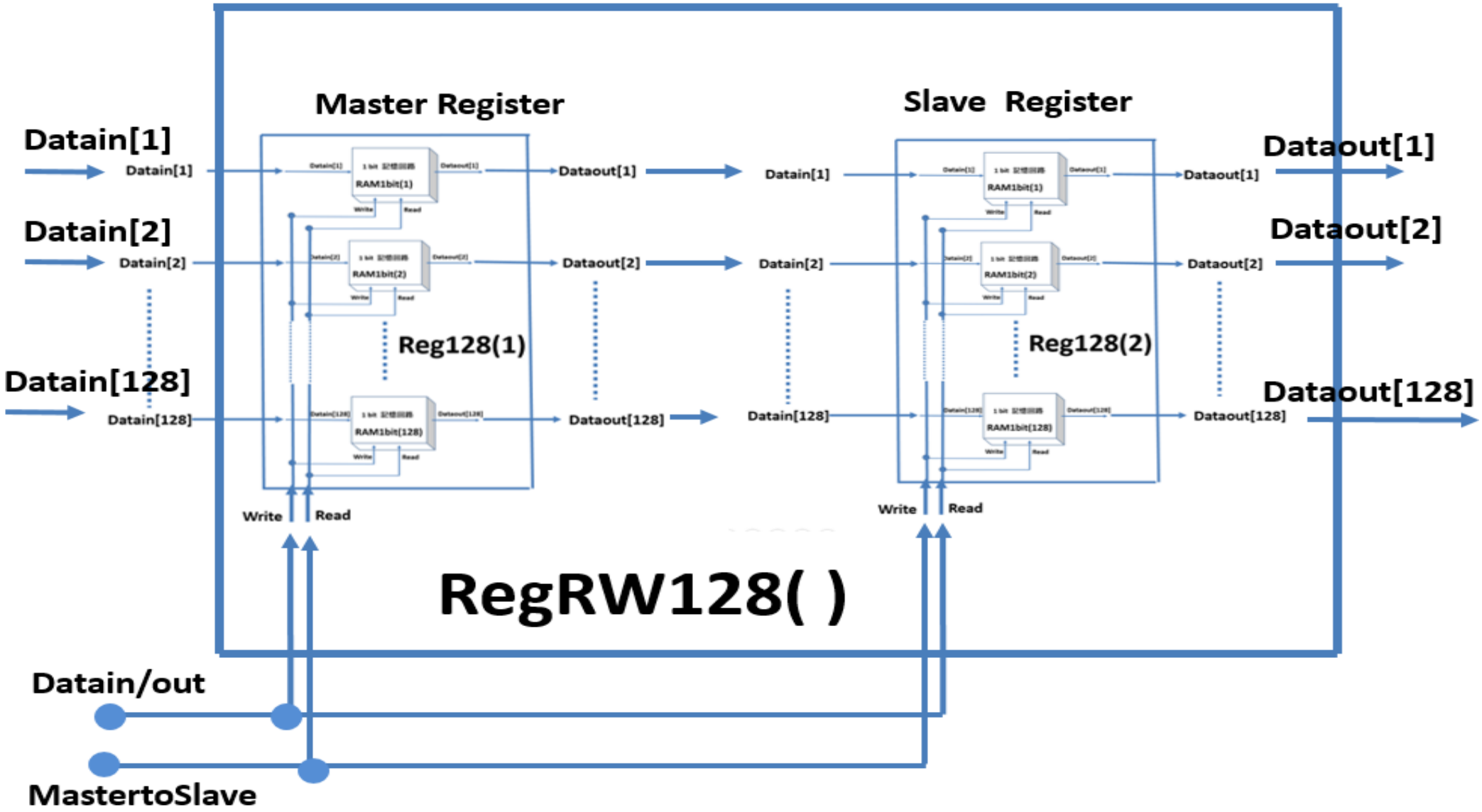
128 bit data 比較回路

図 1-6-3



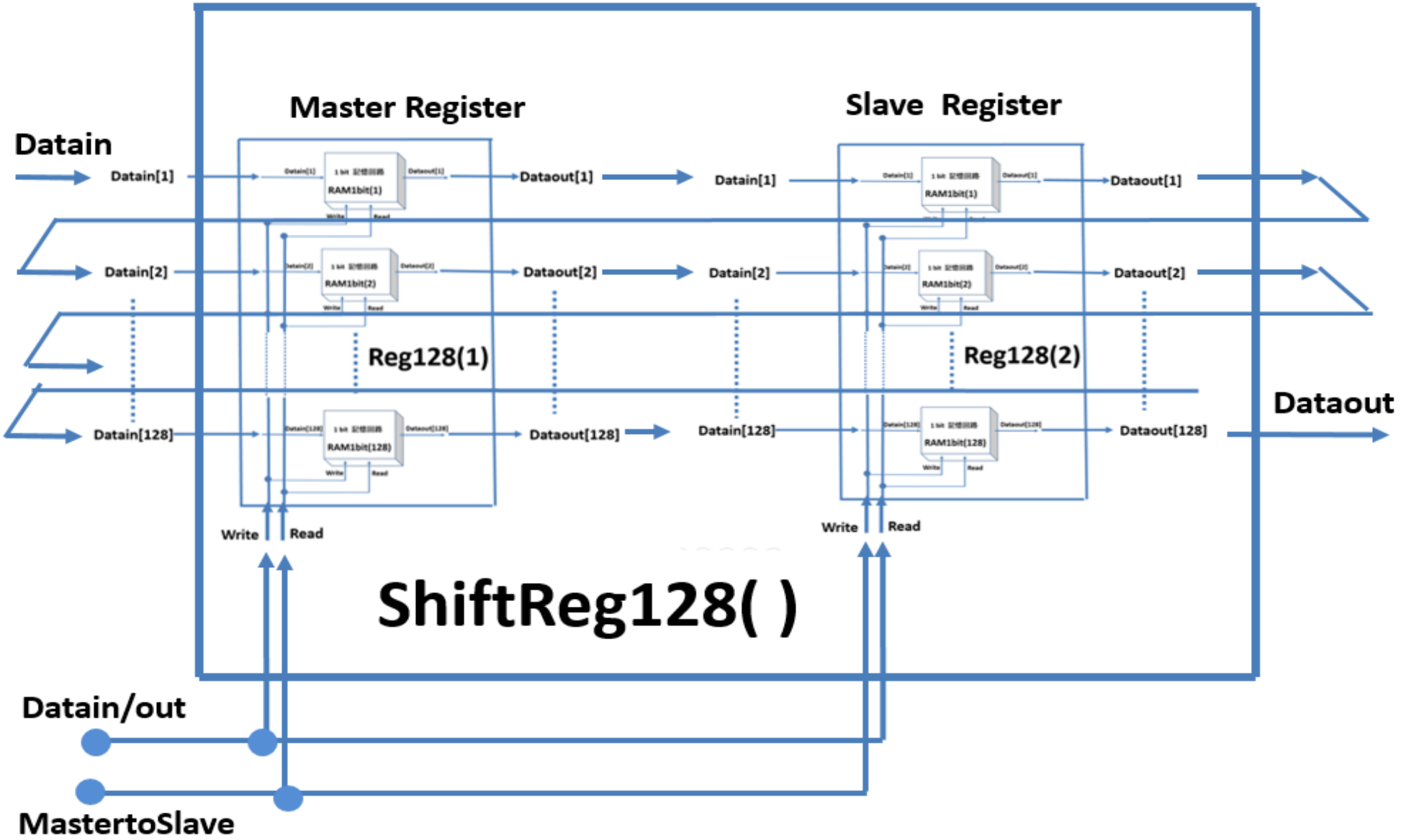
Latch 型 128 bit Register回路　Reg128( )回路の全体図

図 1-6-4



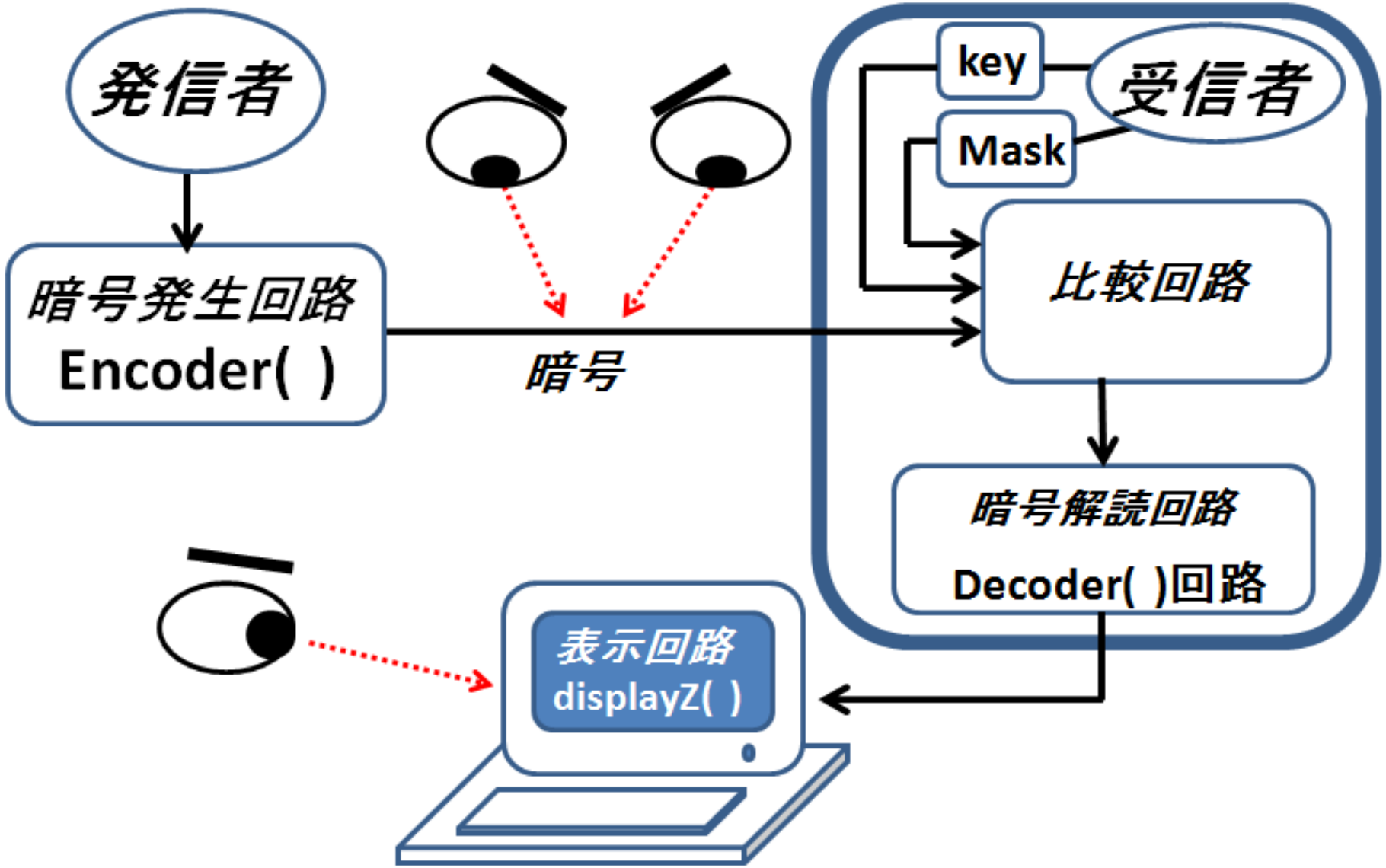
同時読み書き可能な　RegRW128（）回路

図 1-6-5



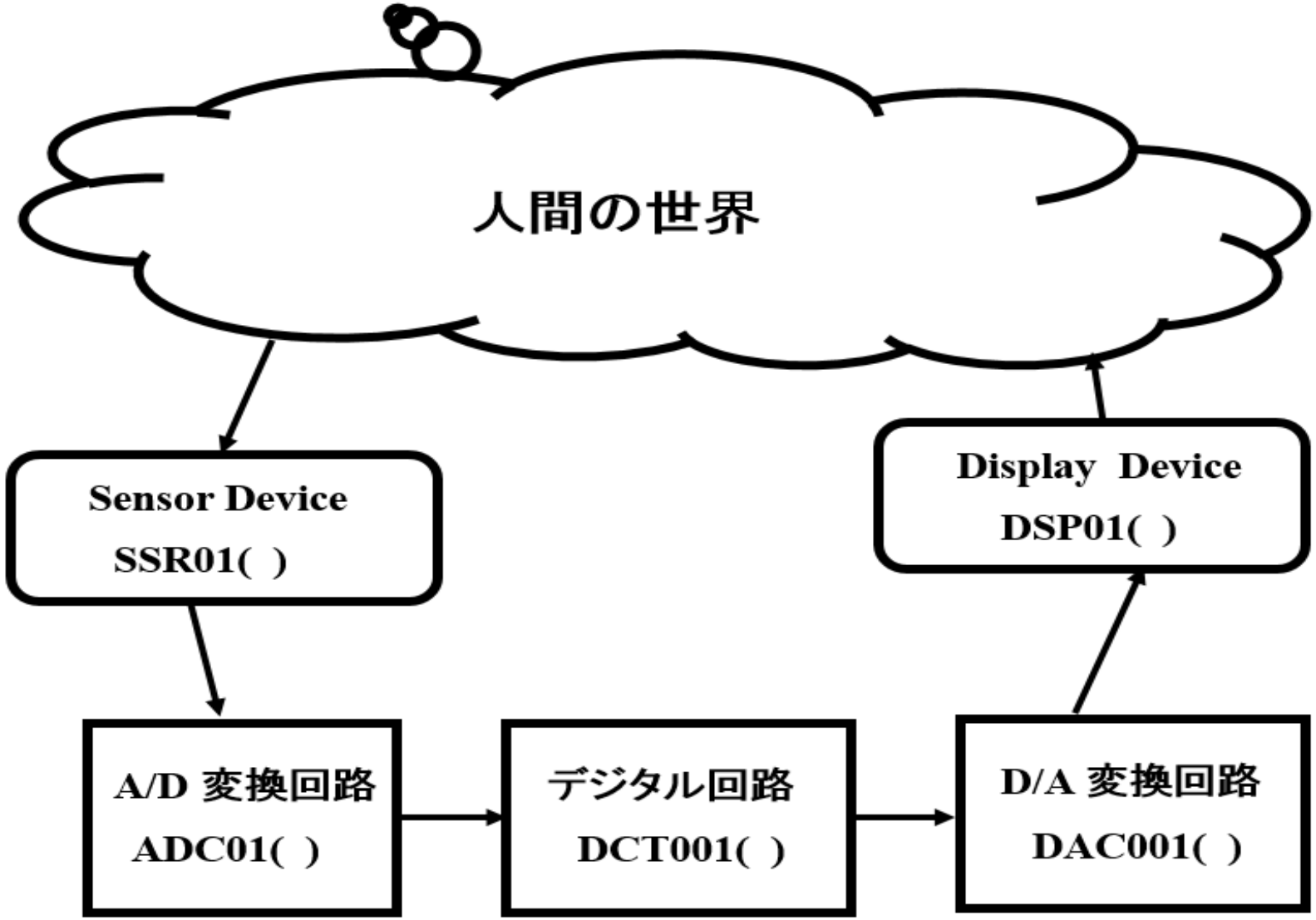
Latch型記憶回路で構成した128 bit Shift Register

図 1-6-6



暗号の自動解読装置のイメージ図

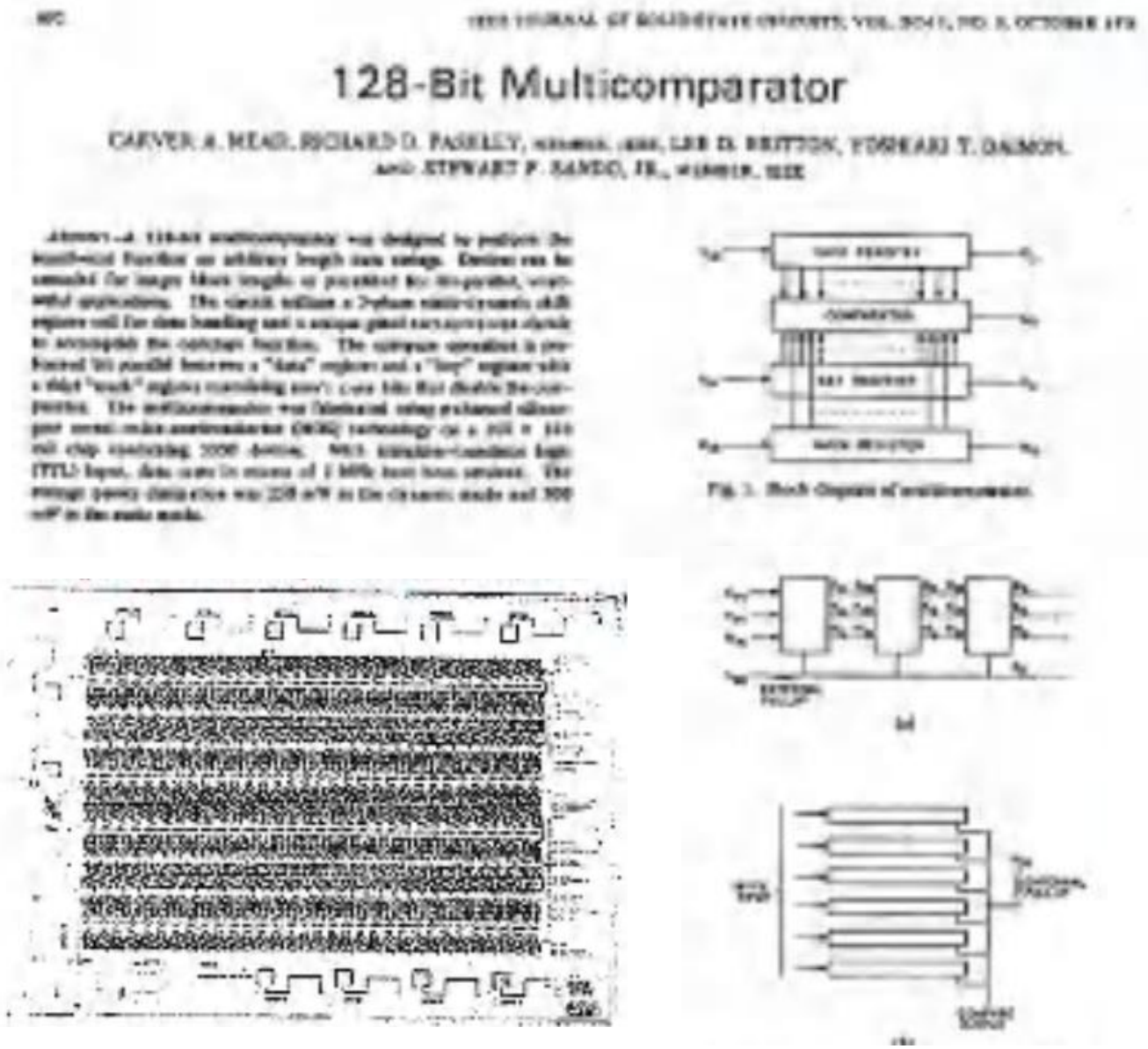
図 1-6-7



デジタル回路が持つ情報伝達の使命

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976



128-Bit Multicomparator

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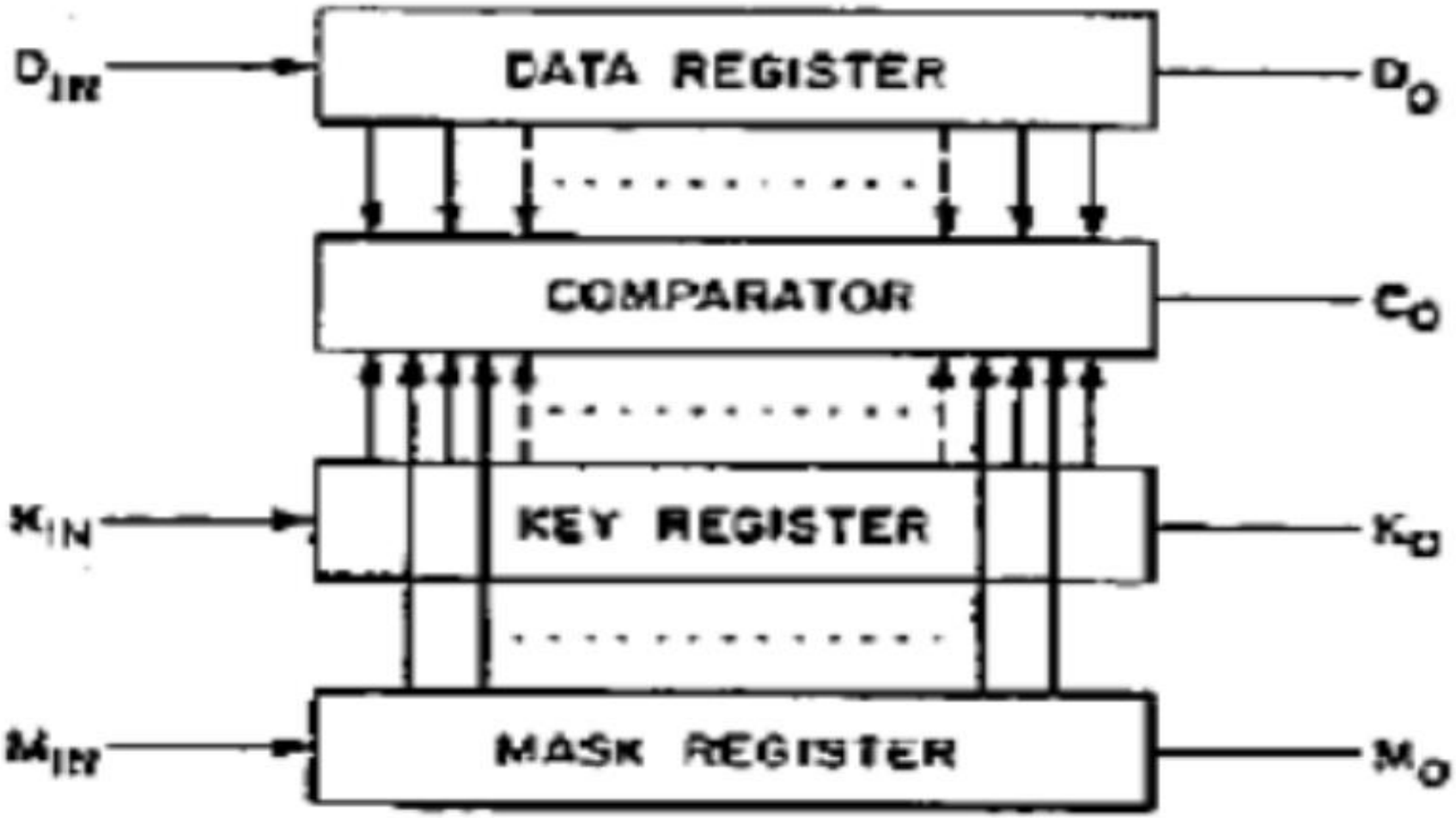
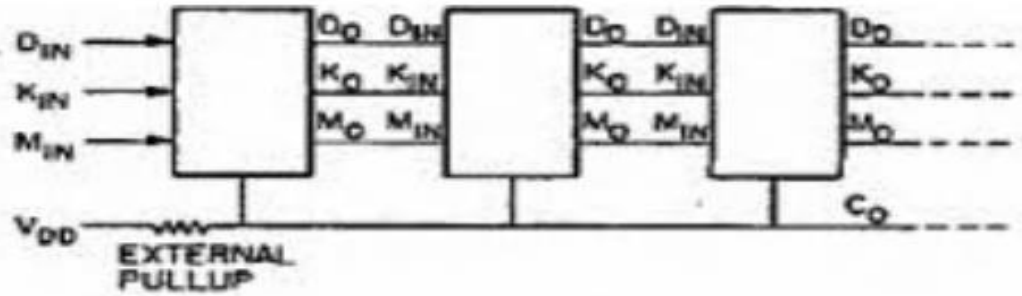


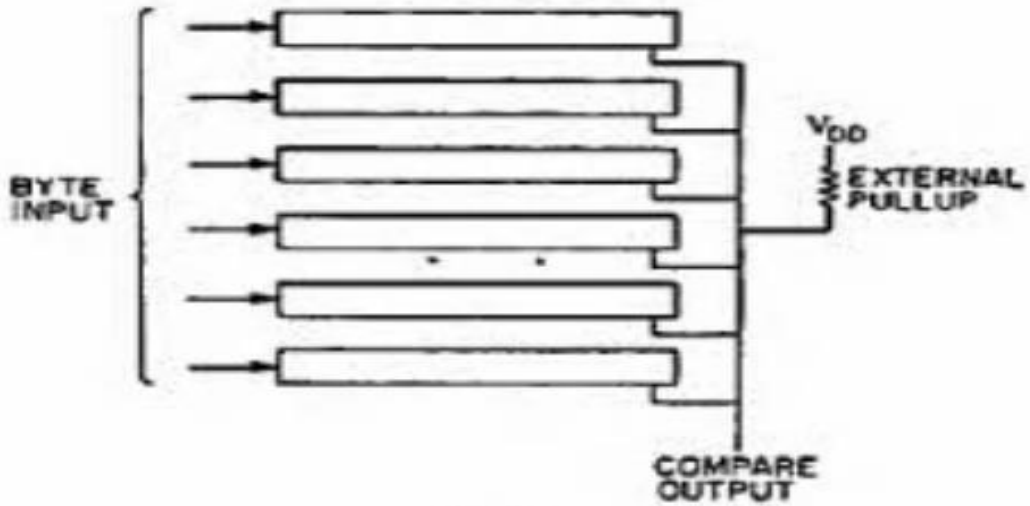
Fig. 1. Block diagram of multicomparator.

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976



(a)



(b)

Fig. 2. Possible connections of multicomparator. (a) Cascaded. (b) Bit-parallel, word-serial.

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976

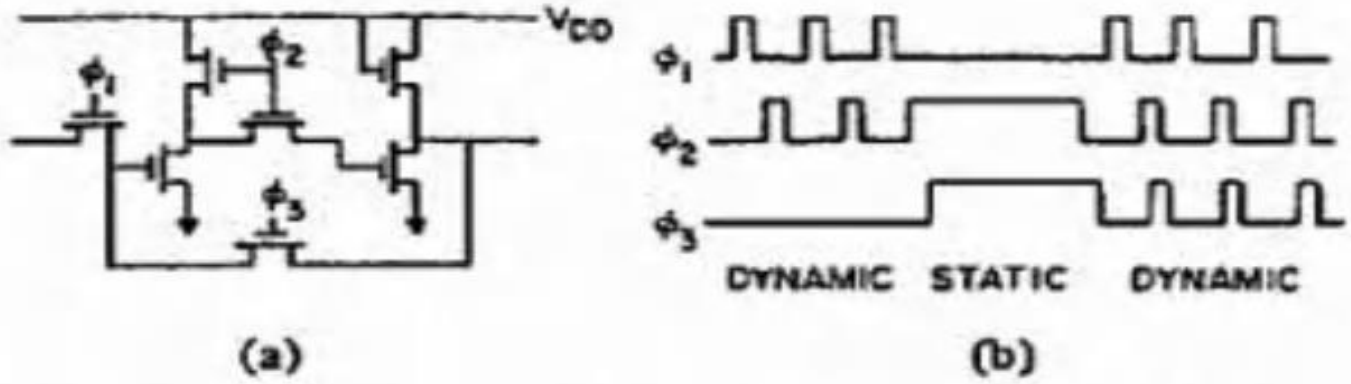


Fig. 3. Basic shift register cell. (a) Schematic. (b) Clock timing.

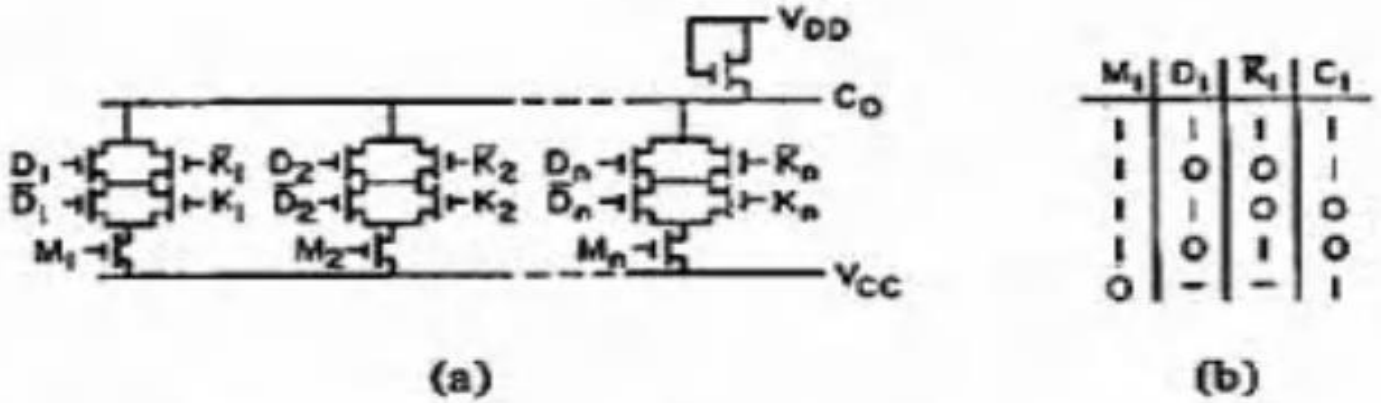


Fig. 4. Gated EXCLUSIVE-NOR gate. (a) Schematic. (b) Truth table.

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976

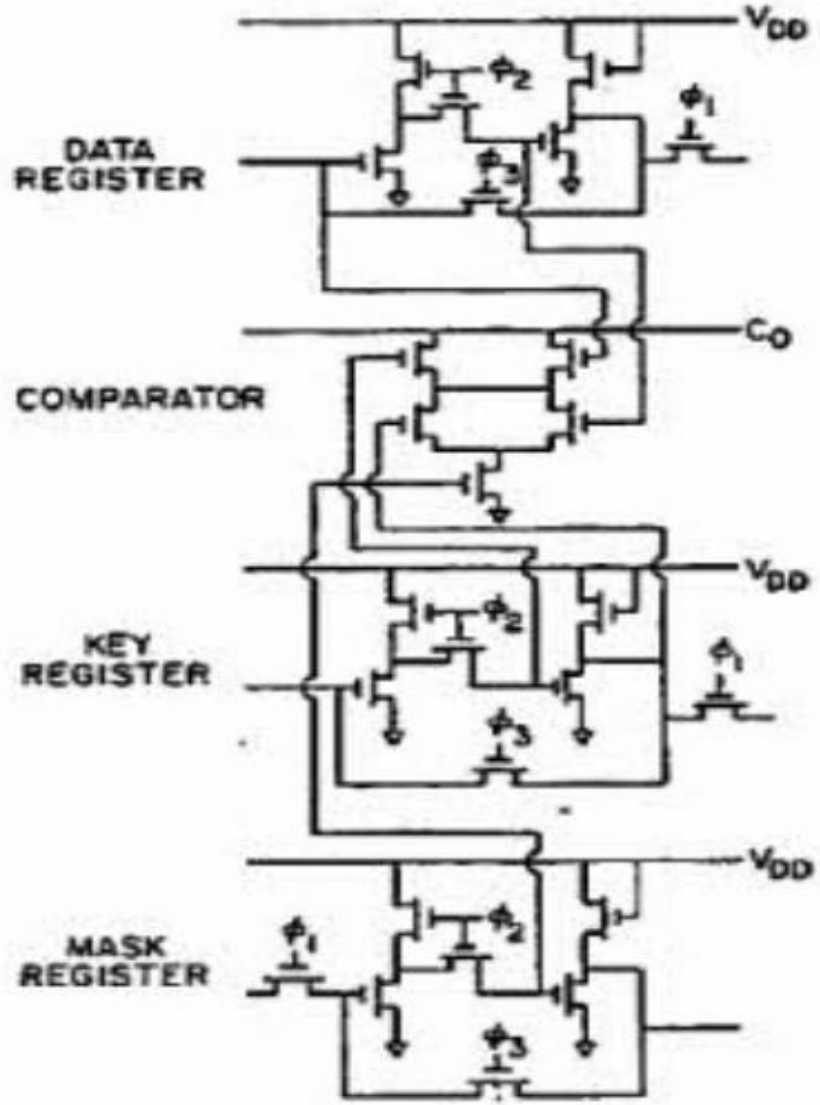


Fig. 5. Full schematic of one bit slice of the multicomparator.

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976

serial-in/serial-out fast 128 bit parallel data comparator chip
fabricated by Intel corporation p-channel E/D MOS fabrication line

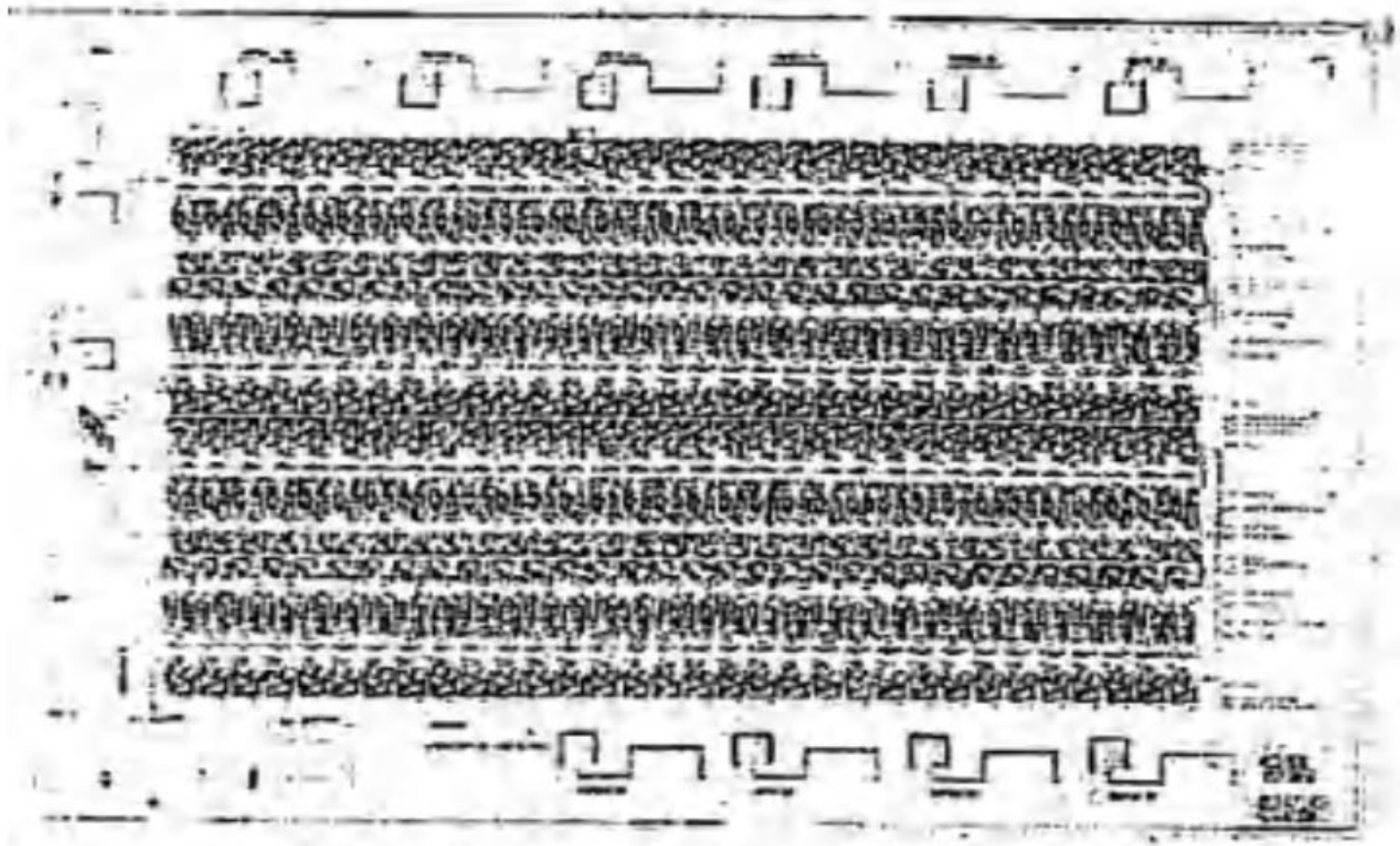


Fig. 6. Photomicrograph of multicomparator chip.

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976

TABLE I

Parameter	Performance[a]
Clock rate	0.0001–2 MHz
Dynamic supply current	25 mA
Static supply current	30 mA
Clock leakage current (ϕ_1)	120 nA
Clock leakage current (ϕ_2)	300 nA
Clock capacitance (ϕ_1)	40 pF
Clock capacitance (ϕ_2)	60 pF
Clock capacitance (ϕ_3)	40 pF
Interclock capacitance	7 pF
Input capacitance	10 pF
Output capacitance	10 pF

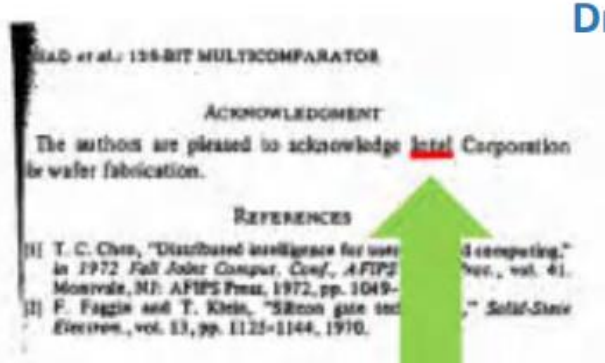
[a] *Test Conditions:*

$$T = 23^{\circ}\text{C}, V_{cc} = 5\text{ V}, V_{DD} = -5\text{ V},$$

$$V_{\phi L} = +5\text{ V}, V_{\phi H} = -5\text{ V}, V_{\text{input}} = 0.5\text{ V}.$$

128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976



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The authors are pleased to acknowledge Intel Corporation for wafer fabrication.

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Dr. Lee Barton at Hewlett-Packard
Caltech Graduate, 1973

Lee D. Brinton received the B.S.E.E. degree from the California Institute of Technology, Pasadena, in 1973.

He then invented and marketed a computer-aided memory for theater lighting control, and now works for Hewlett-Packard Laboratories, Cupertino, CA, designing and testing LSI integrated circuits for mini-computers.

Dr. Yoshiaki Hagiwara at Sony
Caltech Graduate, 1975

Yoshiaki Hagiwara was born in Kyoto, Japan, on July 4, 1948. He received the B.S., M.S., and Ph.D. degrees from the California Institute of Technology, Pasadena, in 1971, 1972, and 1975, respectively.

Since 1967, he has served several research groups in the Institute. He worked as a Data Processor in hydraulics from 1967 to 1969, engaging in the analysis of the pressure distribution of solitary waves, the influence of the geological features of a harbor upon the induced standing-wave amplitude in the harbor, and the diffusion mechanism of polluted objects in moving fluids. From 1969 to 1971, he worked as an Experimentalist in the Material Science Department and studied the switching and other electronic properties of newly developed amorphous alloys from the low temperature of 4 K to room temperature. From 1971 to 1975 he was a Research and Teaching Assistant both in the Electrical Engineering and Physics Departments at the California Institute of Technology. In the summer of 1971 and 1973, he visited Sony Corporation, Tokyo, Japan, as a Product-Appraisal Engineer at the Atsugi plant and engaged in developments and applications of bipolar technologies in video and power integrated circuits. He is presently with the Sony Corporation, Tokyo, Japan. His interests lie in the areas of digital and linear integrated circuit designs, the physics of microelectronics, and artificial intelligence.

Prof. C.A.Mead at Caltech

Carver A. Mead received S., M.S., and Ph.D. degrees from the a Institute of Technology, Pasadena, , 1957, and 1959, respectively.

He has been a member Faculty of the California Institute of D., Pasadena, CA, since 1957. His re as contributed to the understanding o ing in solids, current flow mechanis his dielectric films, metal-semiconduct rs, band energies in semiconductors, a onic processes in insulators. He has proposed and demonstr peration of a number of new solid-state electronic devices s several U.S. patents.

Dr. Mead is a Fellow of the American Physical and a member of Sigma Xi.

Dr. Richard Pashley at Intel
Caltech Graduate, 1974

Richard D. Pashley (M born in Ft. Belvoir, VA, on Septem 1947. He re-

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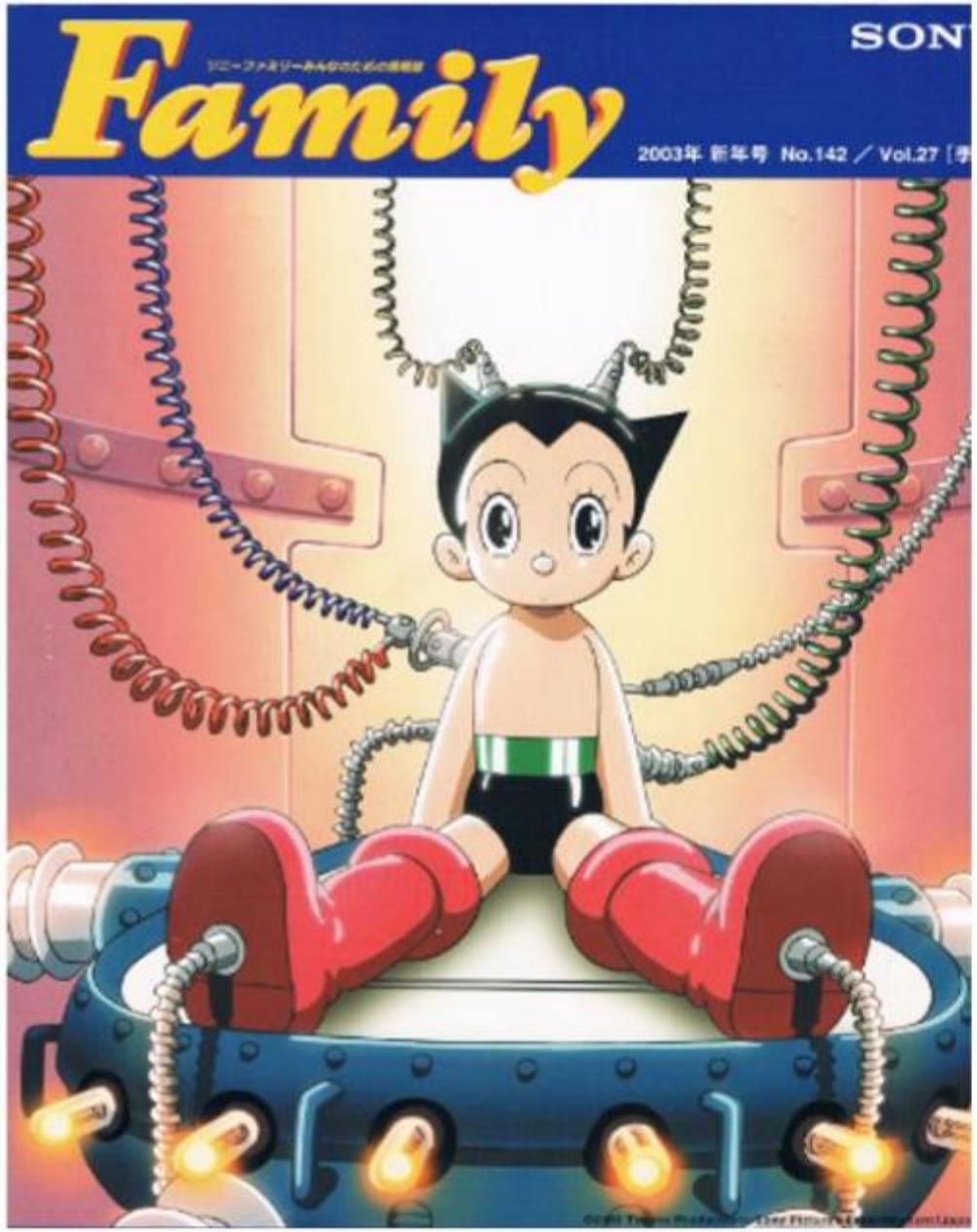

Sony Family Journal 2003 January Issue, No.142/Vol.27

Yoshiaki Hagiwara was born on July 4, 1948 in Kyoto Japan. Graduated from Murasaki-no Elementary School in 1958. Lady Murasaki Shikibu is very famous as the writer of the story of Genji. Graduated from Rakusei Middle High School in 1961. Moved to Riverside-city in California USA in 1965 and graduated from Riverside City Polytechnique High School in 1967. Lived in Pasadena California since 1967 and received BS1971, MS1972 and PhD1975 in Electrical Engineering and Physics from California Institute of Technology (Caltech) . Joined Sony on February 1975 till July 2008. Taught at Sojo University as a professor till 2017. He is now serving for the ssis.or.jp.

Artificial Intelligent Partner System(AIPS) Home Page Top

hagiwara-yoshiaki@aiplab.com

Hello, my name is Yoshiaki Hagiwara. I am also called simply as Yoshi, and as Yoshiaki Daimon and also as Yoshiaki Daimon-Hagihara. I believe that I am the true inventor of the digital camera with the mechanical shutter function capability, which is completely filmless and free from mechanical parts. I worked at Sony from 1975 till 2008. My friends in Sony developed the digital camera in 1987. Sony is now enjoying image sensor business. Image sensors are very important to realize Artificial Intelligent AI robots and self-driving cars.

Evidence that Yoshiaki Hagiwara is the inventor of Pinned Buried Photodiode with in-pixel overflow Drain (VOD) function is given by the three basic Japanese Patent Applications, JPA1975-127646, JPA1975-127647 and JPA1975-134985.

Hagiwara also invented the in in-pixel Overflow Drain (OFD) Punch-thru Clocking Scheme to realize the completely-mechanical-part-free Electrical Shutter for digital cameras, opening a way to realize our modern digital TV world.

Evidence that Yoshiaki Hagiwara is the inventor of Electrical Shutter is given by the basic Japanese Patent Applications, JPA1977-126885.

The first Double Junction Pinned Buried Photodiode was developed by Hagiwara team at Sony in 1978. The first Triple Junction Pinned Buried Photodiode with Electrical Shutter function was developed by Hamazaki team at Sony in 1987.

Yoshiaki Hagiwara joined Sony in Feb 1975 to build Artificial Intelligent Partner System(AIPS), which includes Artificial Intelligent Robot System, Artificial Intelligent Self-Driving Car, and Artificial Intelligent Vision Sensor System. His first work was developing the CCD image sensors. Hagiwara Team at Sony in 1989 developed 4M Cache SRAM for SNAPSHOT picture acquisition which opened a way to build the digital camera system. Hagiwara is also the inventor of the electrical shutter of the digital camera system.

受光表面P＋層と裏面のP+層の両面がピン留め接地された、P+PNPP+接合型新型太陽電池の提案

(7) CMOS型インバータ回路の省エネ特性

詳細は青山社出版の人工知能パートナーシステム(AIPS)を支える「デジタル回路の世界」に記載。

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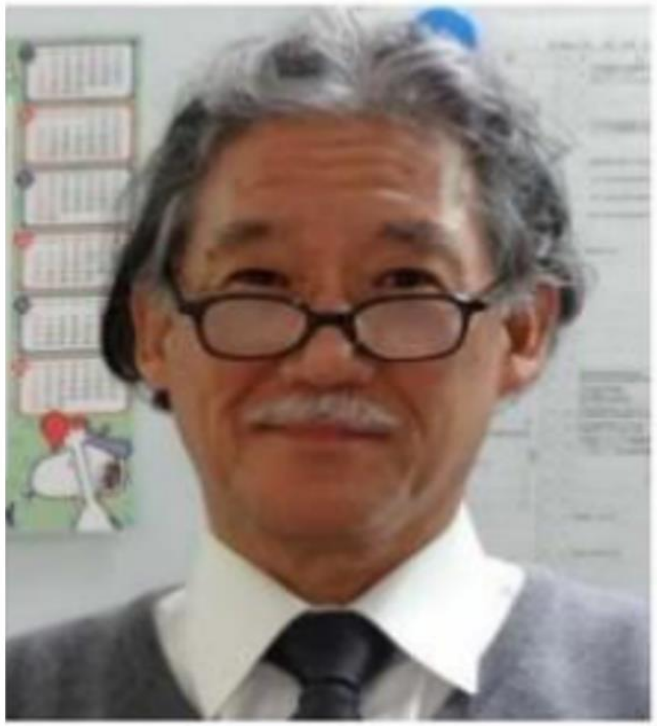

崇城大学 理事長付き 特任教授

IEEE Life Fellow, Ph.D., 工学博士

人工知能パートナーシステム(AIPS)を支える

デジタル回路の世界

IEEE Life Fellow, Ph.D.

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未来の人間社会には人工知能パートナーシステム(AIPS)とも言える人間にやさしい支援システムが出現すると期待している。AIPS搭載の自動走行車や老人介護システム、人間型歩行ロボットやロボット・ハウスなどである。そこで本書では、そのAIPSを支える「デジタル回路の世界」と題し、ハードとソフトの両面で、人とコンピュータをつなぐデジタル技術について紹介している。図や絵をたくさん用意して、基礎からやさしく解説している。

Thank You !