## 受光表面P＋層と裏面のP+層の両面がピン留め接地された、P+PNPP+接合型新型太陽電池の提案

非常に複雑な半導体電子デバイスの物理動作とその構造の説明に挑戦する事になる。できるだけ直観に訴える方法で説明し、数式は極力さけて、基本原理動作を直観的なイメージで理解できる様に工夫をこらして文系の一般社会人の皆様にも親しみを感じる半導体の基礎知識の紹介となればと希望する。

(1)金属と絶縁体の違い

(2)半導体の基本特性

(3) single接合型のダイオードの整流特性

(4) double 接合型バイポーラトランジスタの電流増幅特性

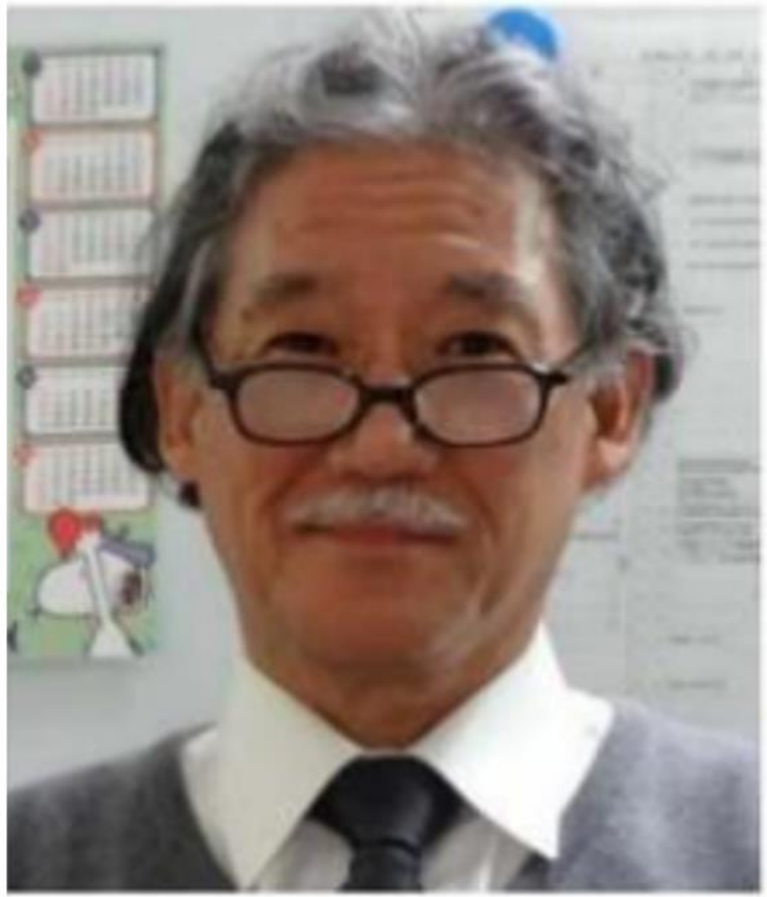
(5) triple 接合型サイリスター型の理想的な高速Switch動作特性

(6) MOS型のトランジスタの電流増幅特性

(7) CMOS型インバータ回路の省エネ特性

(8) 超光感度のCMOS型イメージセンサーの特性

(9) double接合型の新型太陽電池の構造とその動作原理



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# 受光表面P＋層と裏面のP+層の両面がピン留め接地された、P+PNPP+接合型新型太陽電池の提案

## (6) MOS型のトランジスタの電流増幅特性

**詳細は青山社出版の人工知能パートナーシステム(AIPS)を支える「デジタル回路の世界」に記載。**

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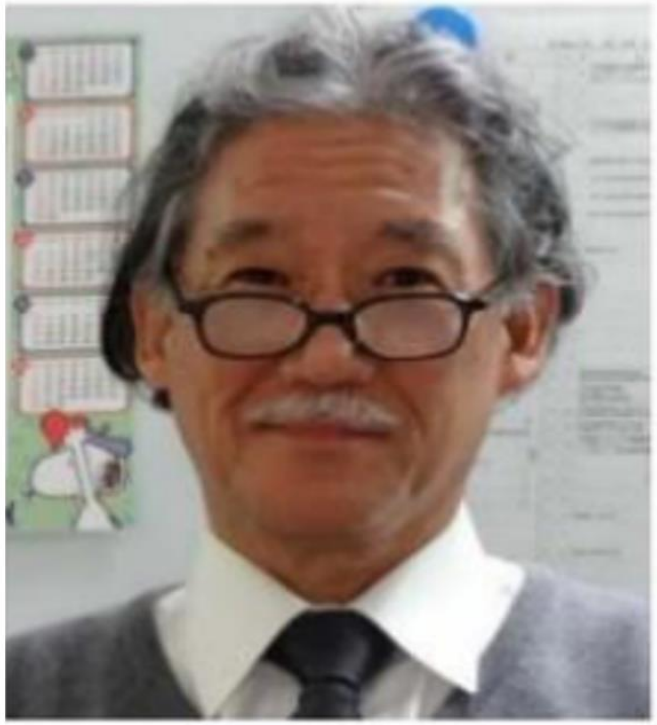


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**IEEE Life Fellow, Ph.D., 工学博士**



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**萩原 良昭 著**

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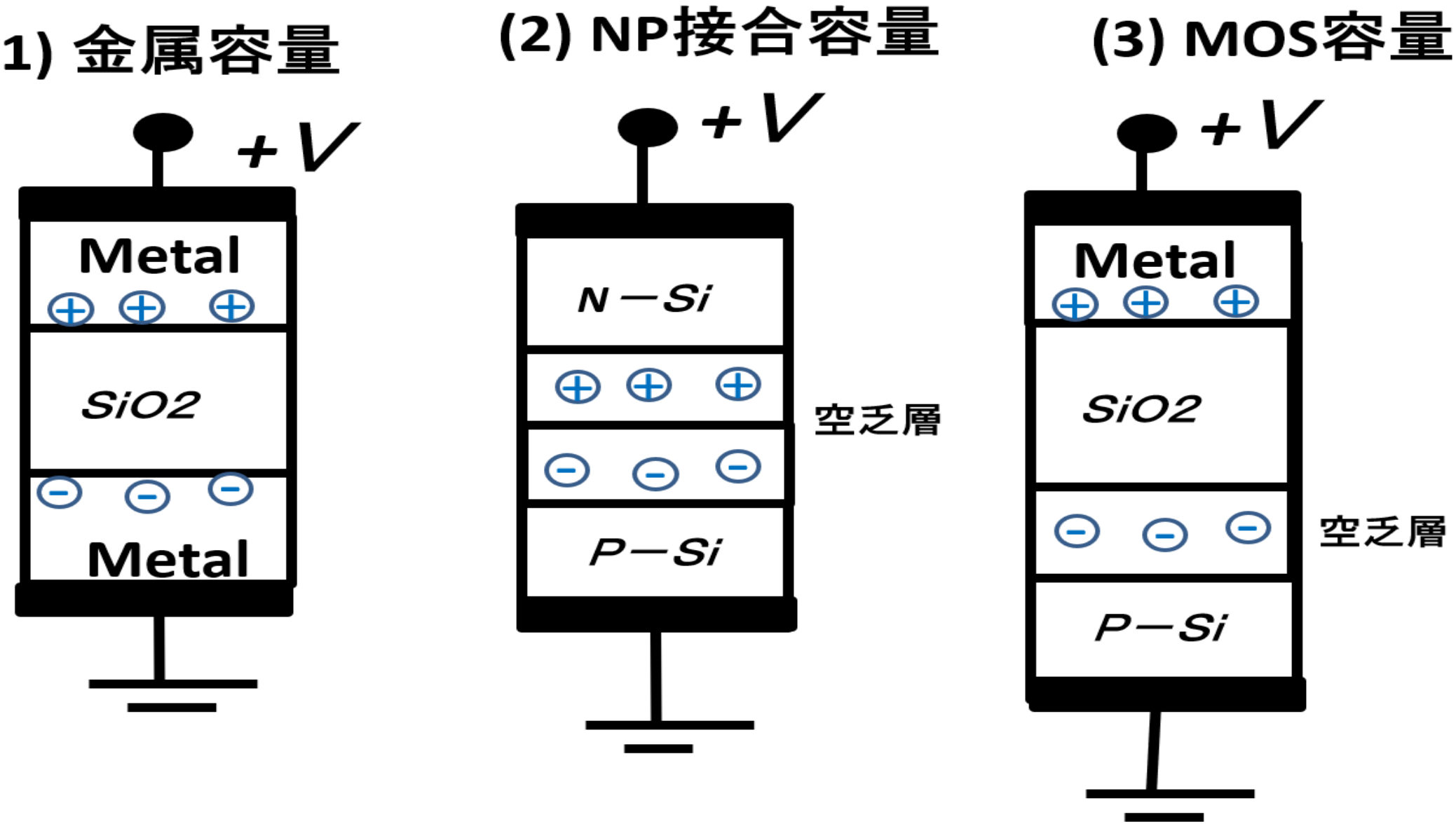
定価(本体9,000円＋税)

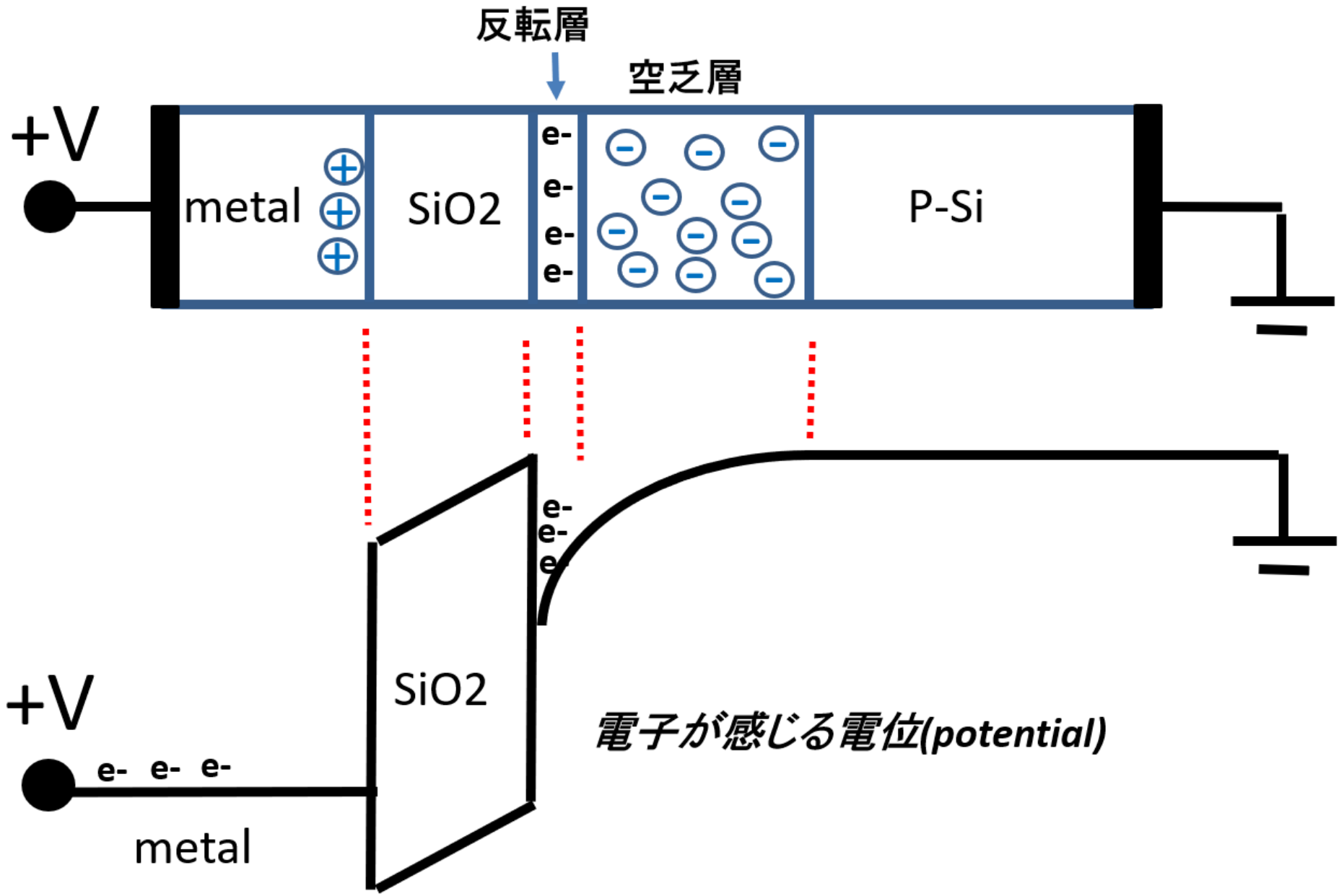
未来の人間社会には人工知能パートナーシステム(AIPS)とも言える人間にやさしい支援システムが出現すると期待している。AIPS搭載の自動走行車や老人介護システム、人間型歩行ロボットやロボット・ハウスなどである。そこで本書では、そのAIPSを支える「デジタル回路の世界」と題し、ハードとソフトの両面で、人とコンピュータをつなぐデジタル技術について紹介している。図や絵をたくさん用意して、基礎からやさしく解説している。

図 4-4-1



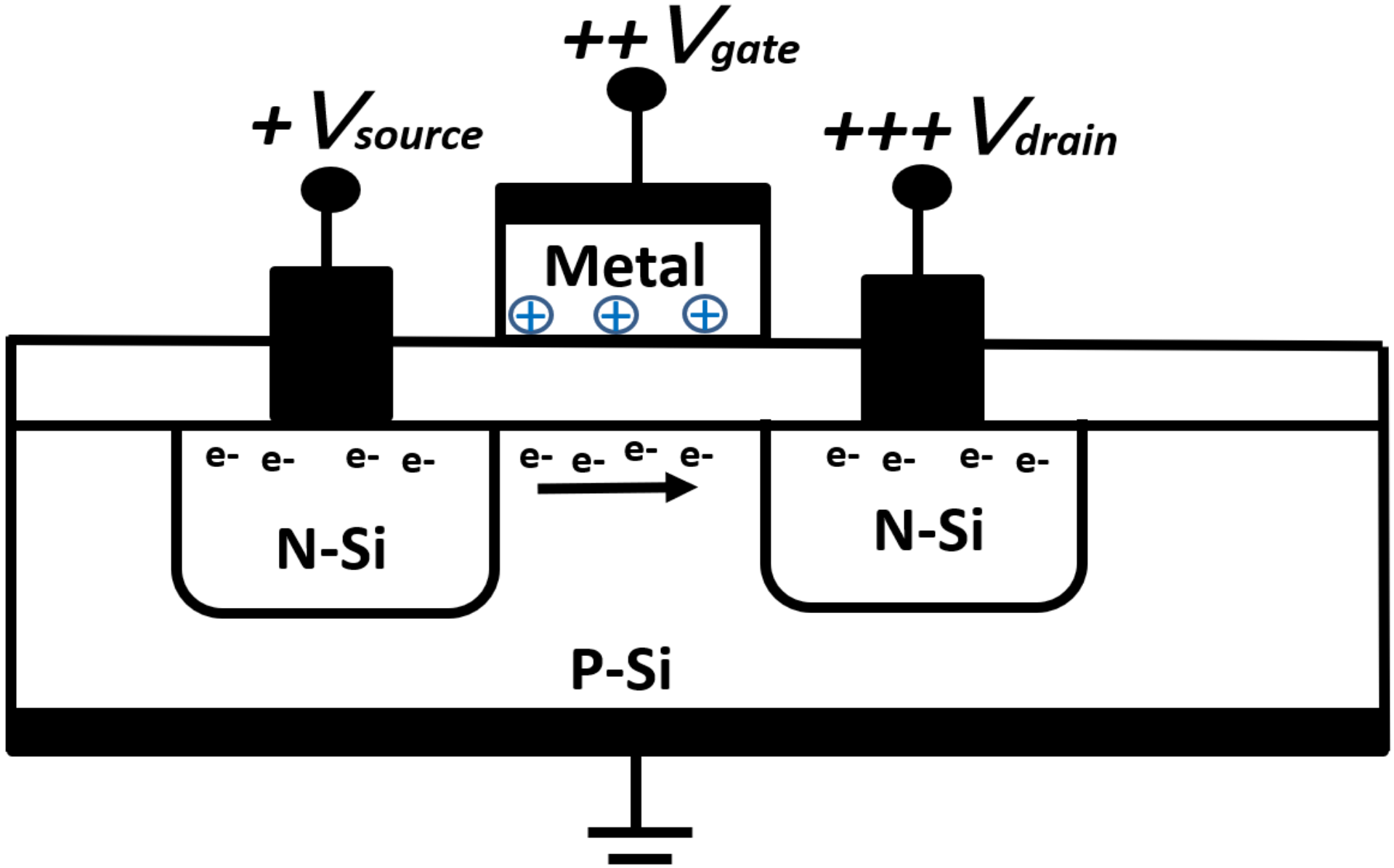

3種類の容量の構造

図 4-4-2



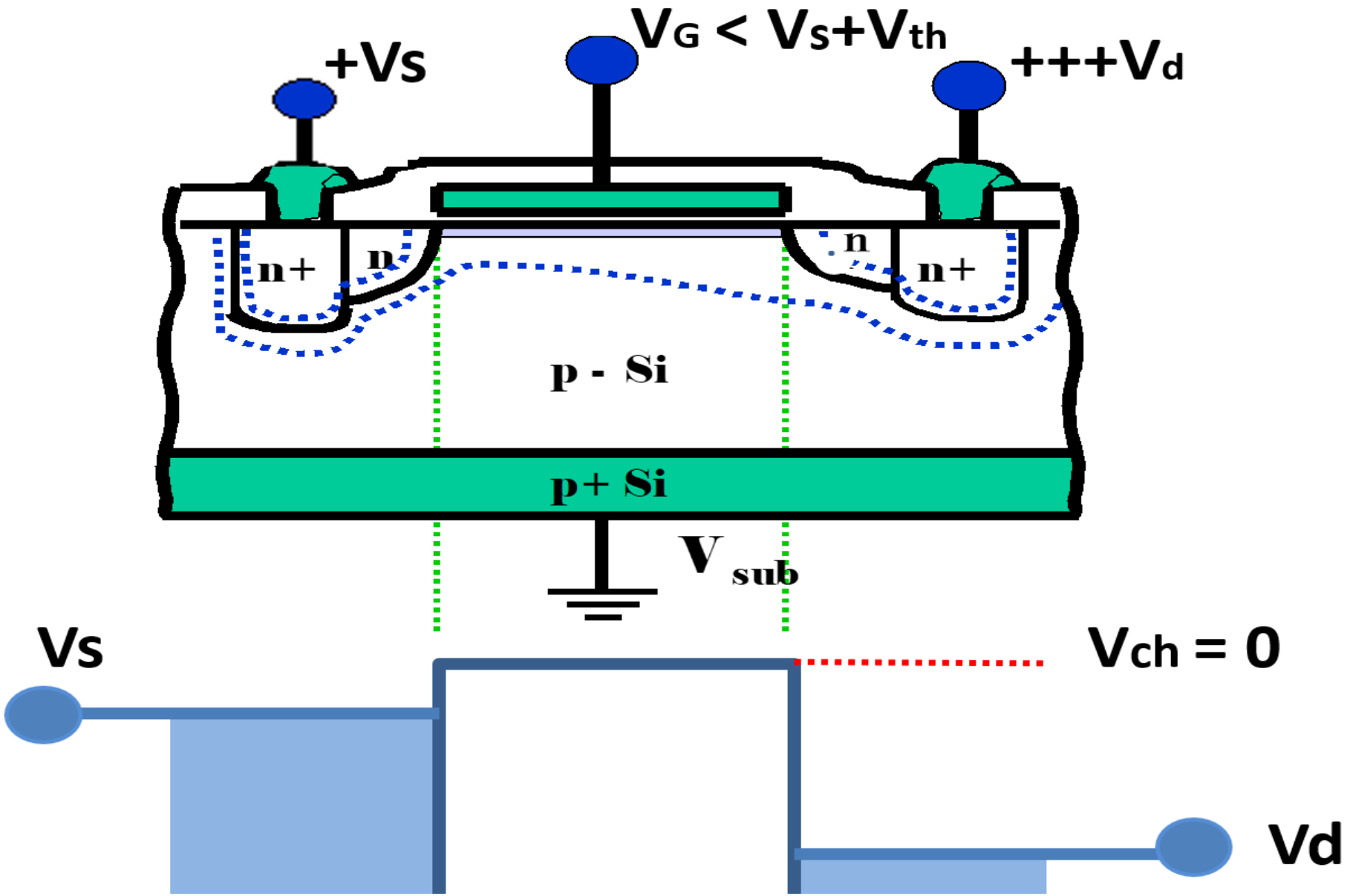

MOS 容量構造に形成される反転層の中の電子

図 4-4-3



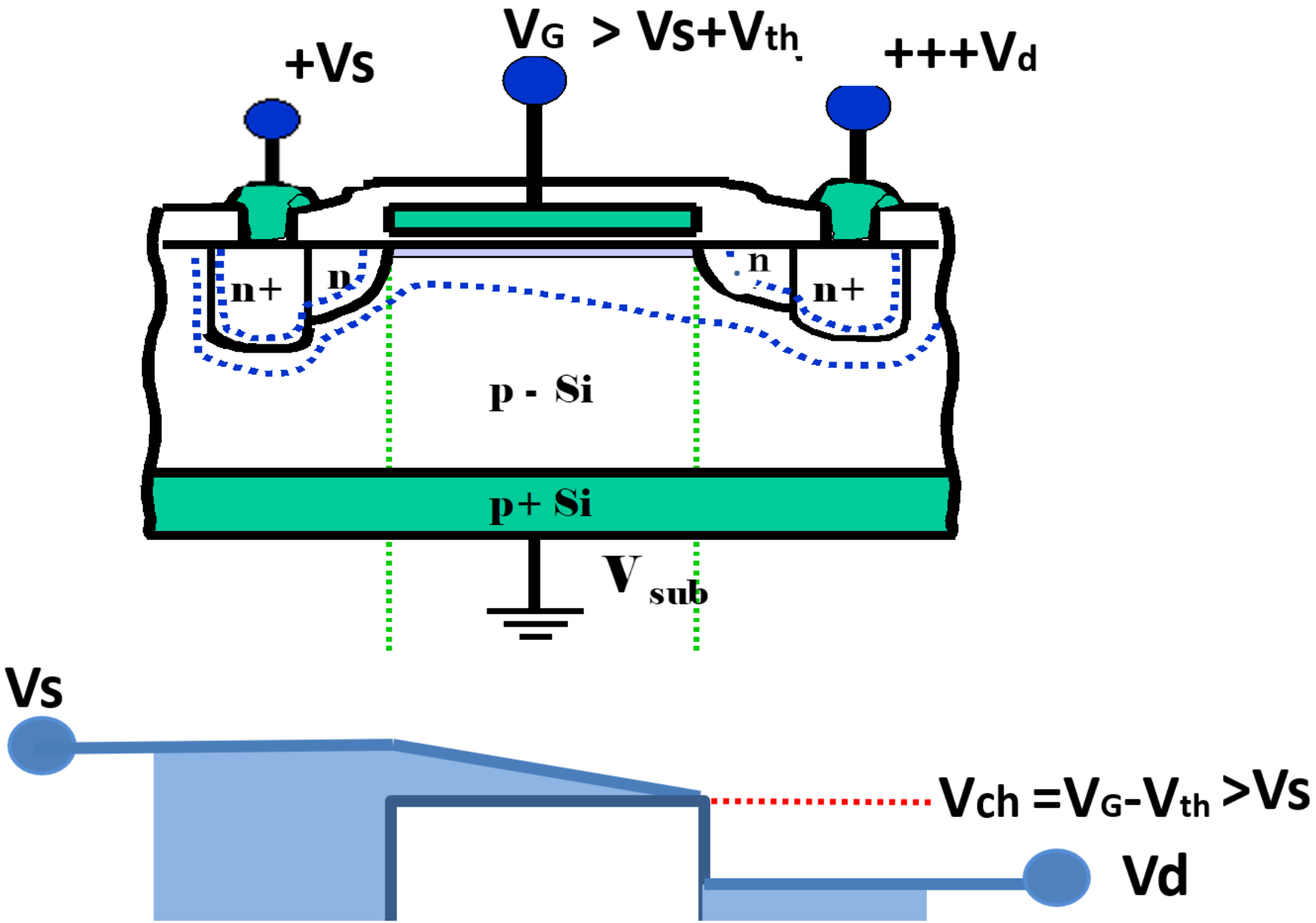

MOS 容量構造に形成される反転層の中の電子

図 4-4-4(1)



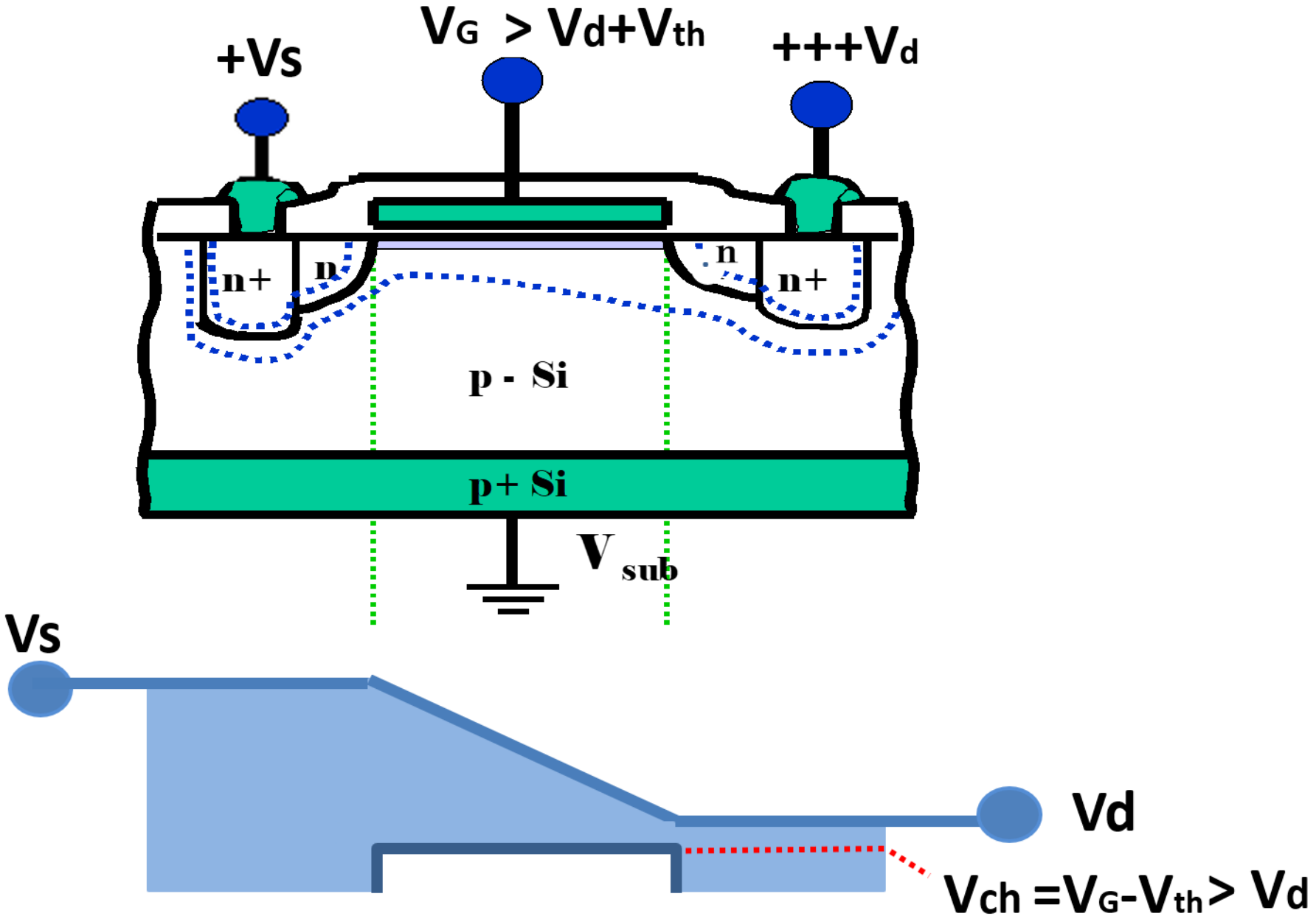

Off mode 動作での MOS transistor の様子

図 4-4-4(2)



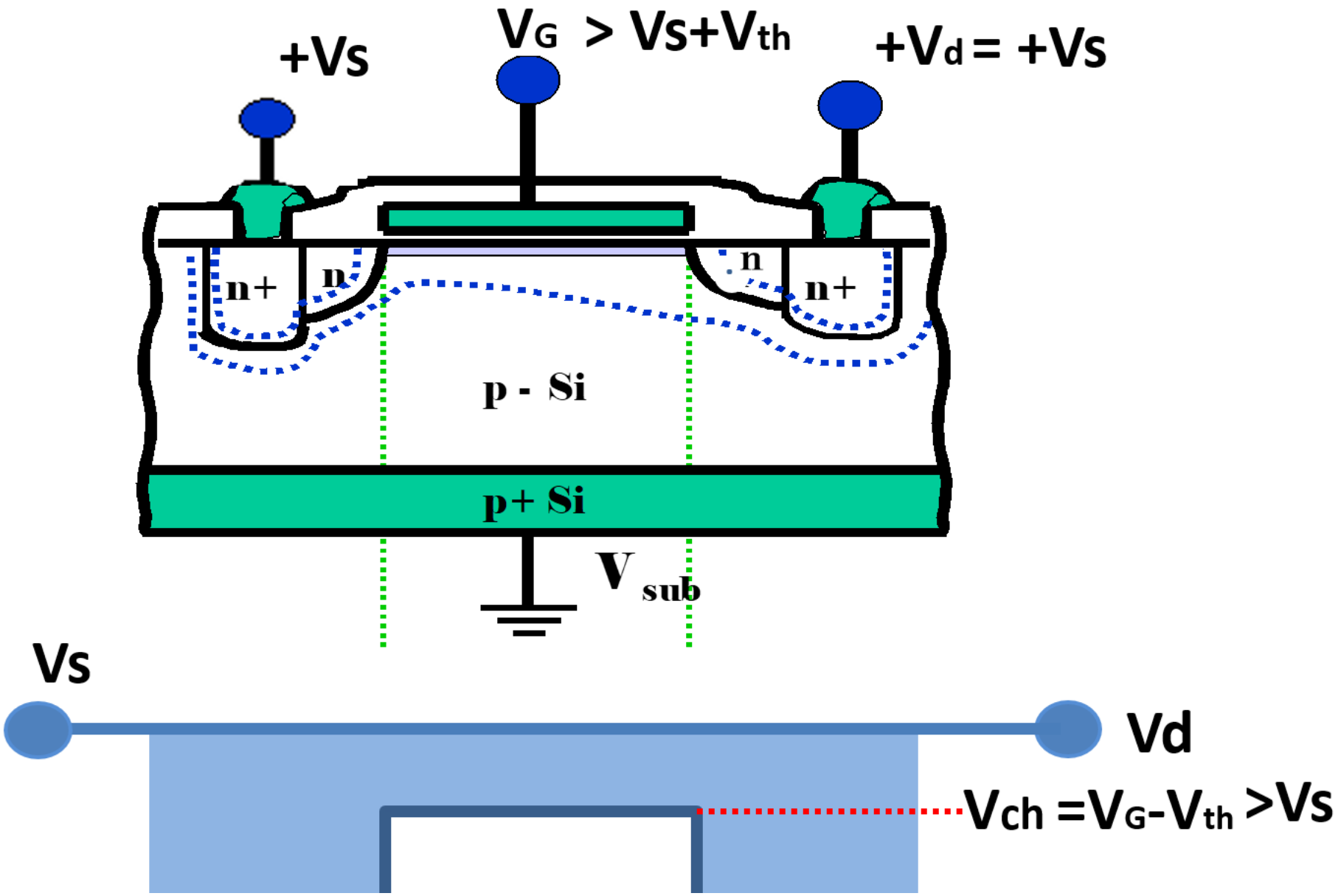

Saturation mode 動作での MOS transistor の様子

図 4-4-4(3)



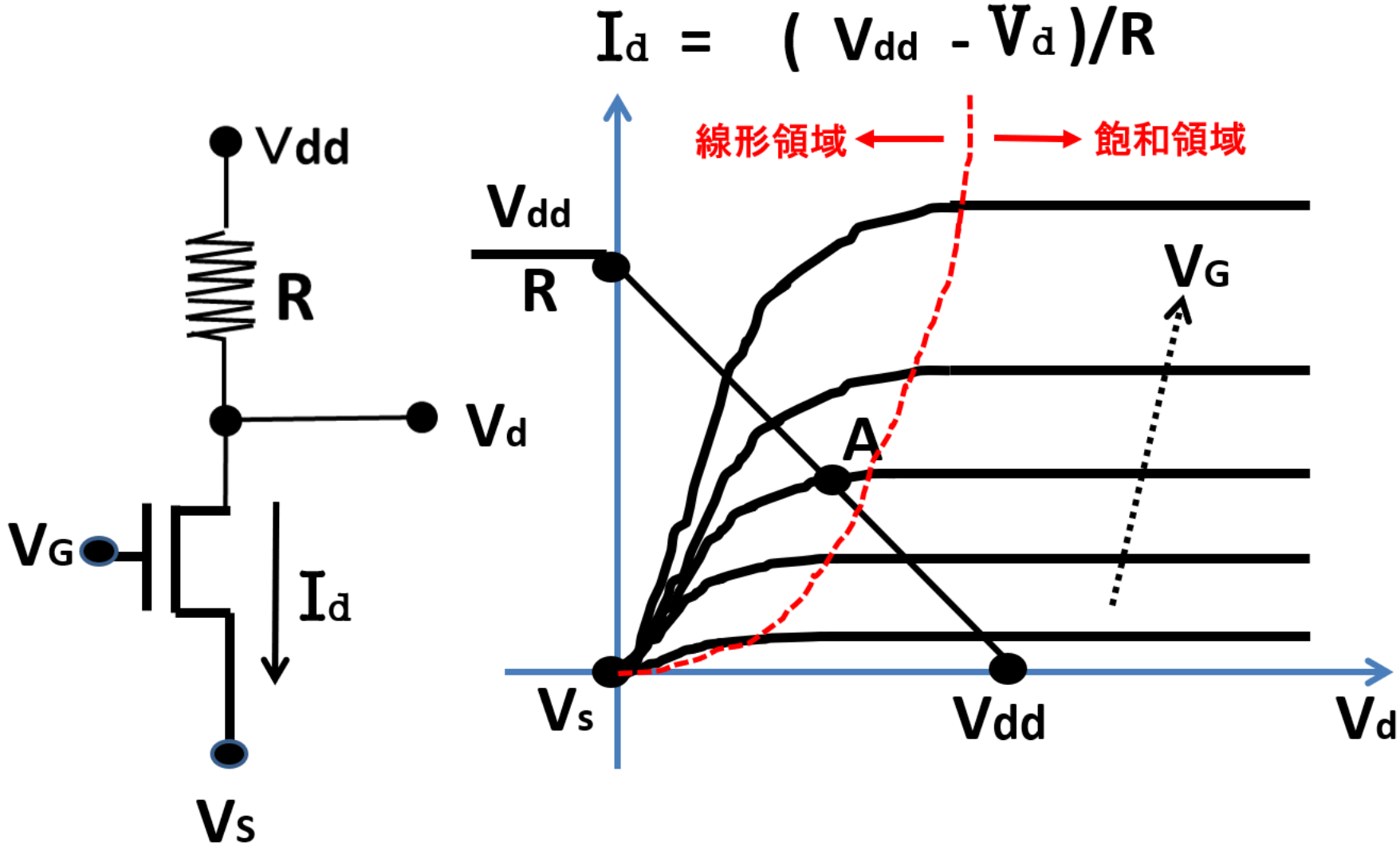

Linear mode 動作での MOS transistor の様子

図 4-4-4(4)



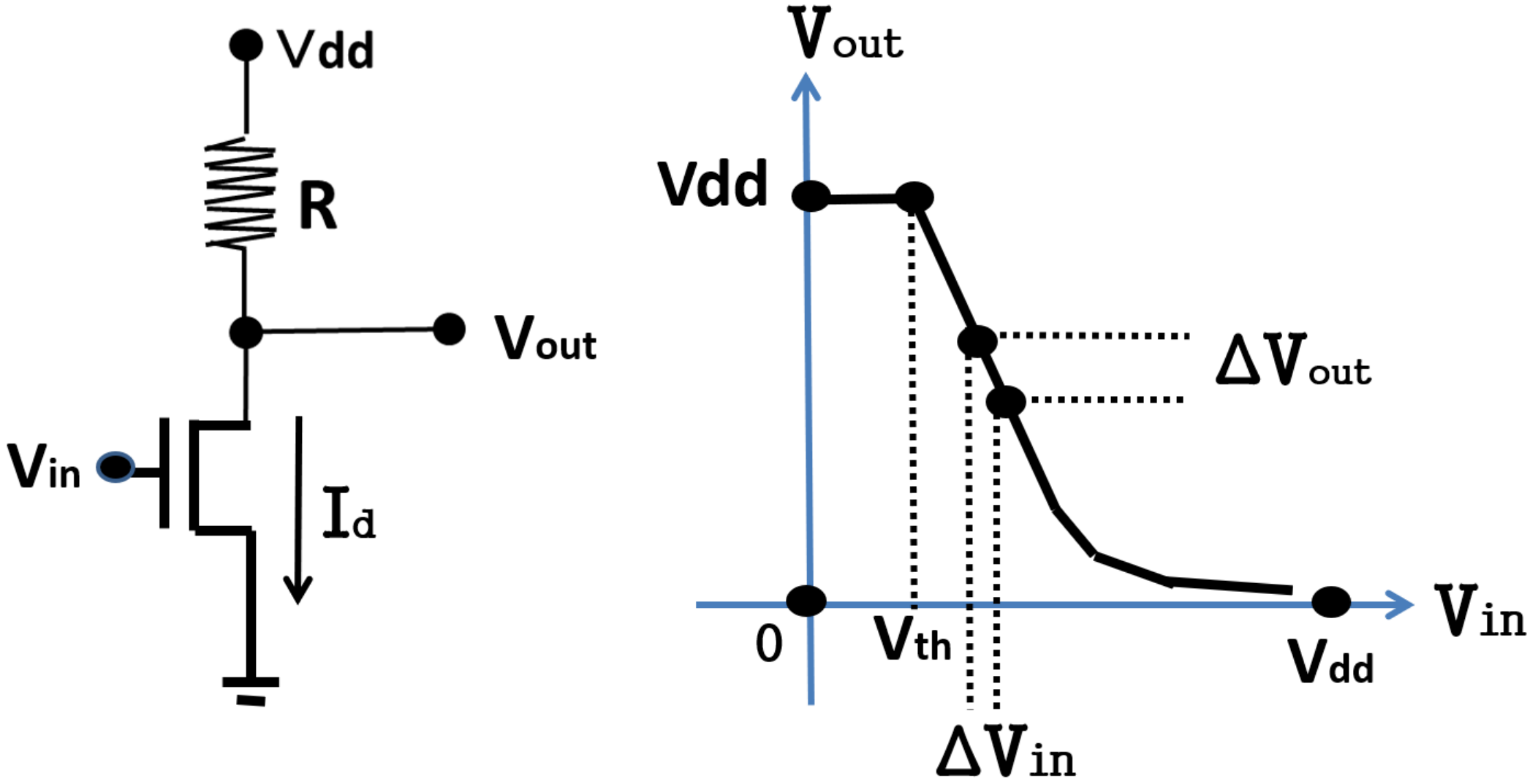

Vd = Vs での MOS transistor の様子

図 4-4-5



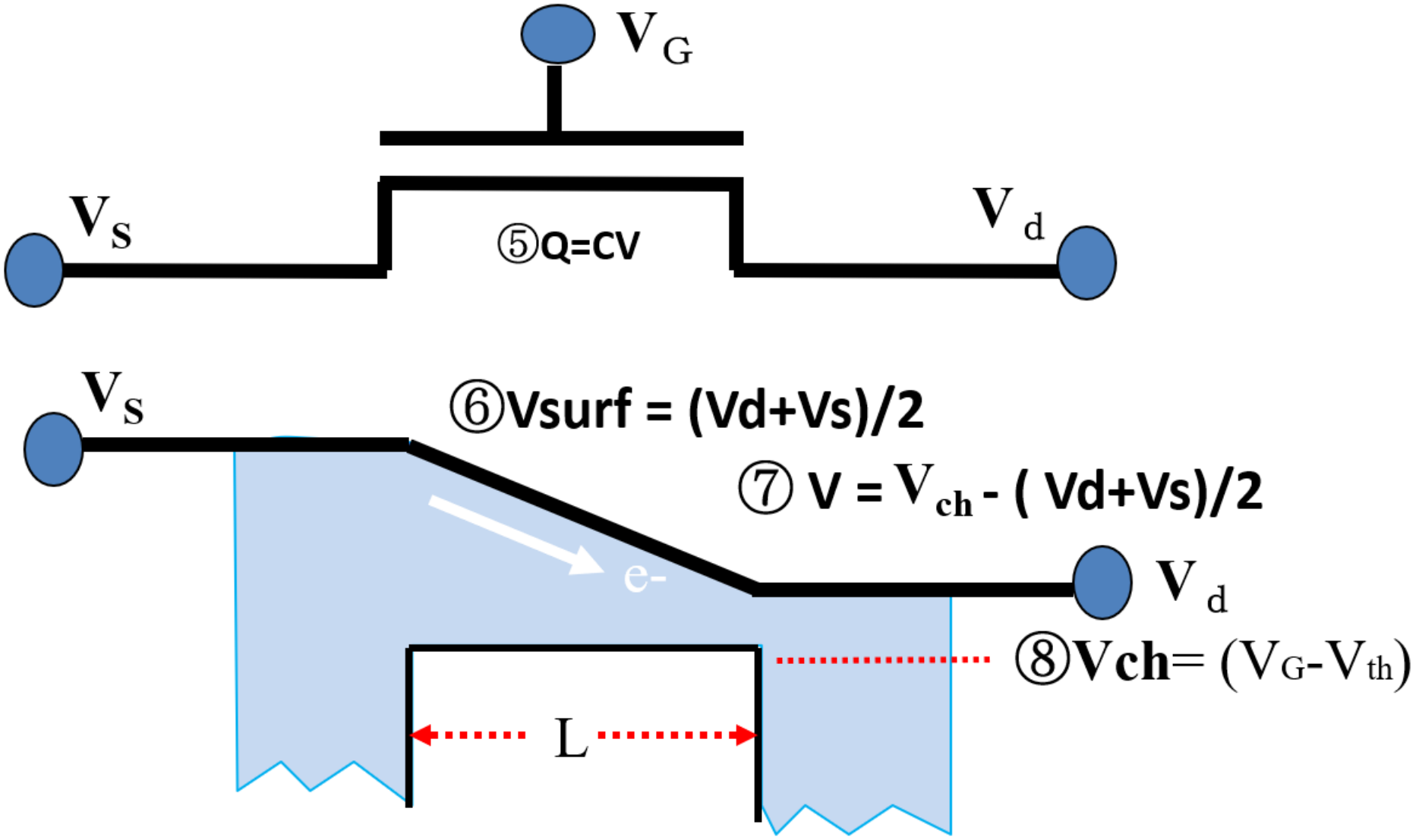

NMOS transistor を使った電圧増幅回路 MOSAmp( ) の I-V 特性

図 4-4-6



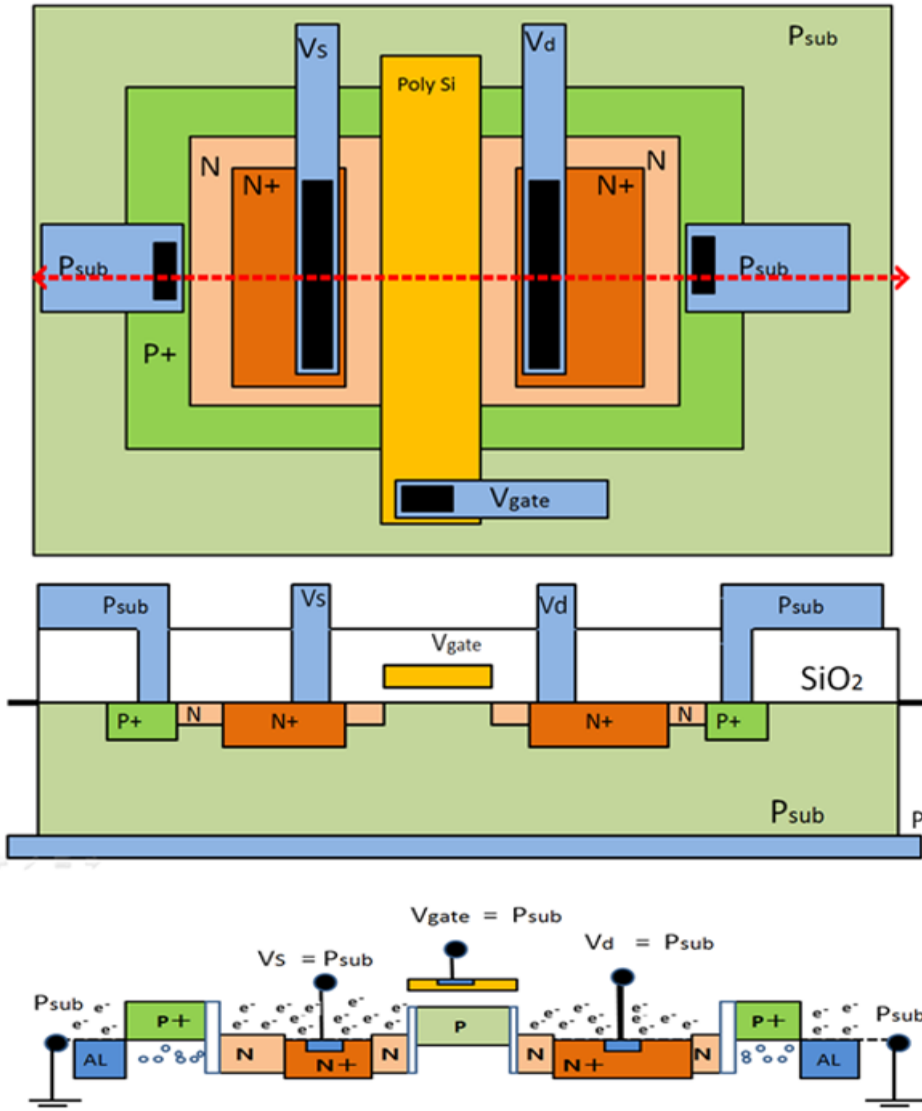

NMOS transistor を使った抵抗負荷型反転回路 invNMOSR( ) の入出力電圧特性

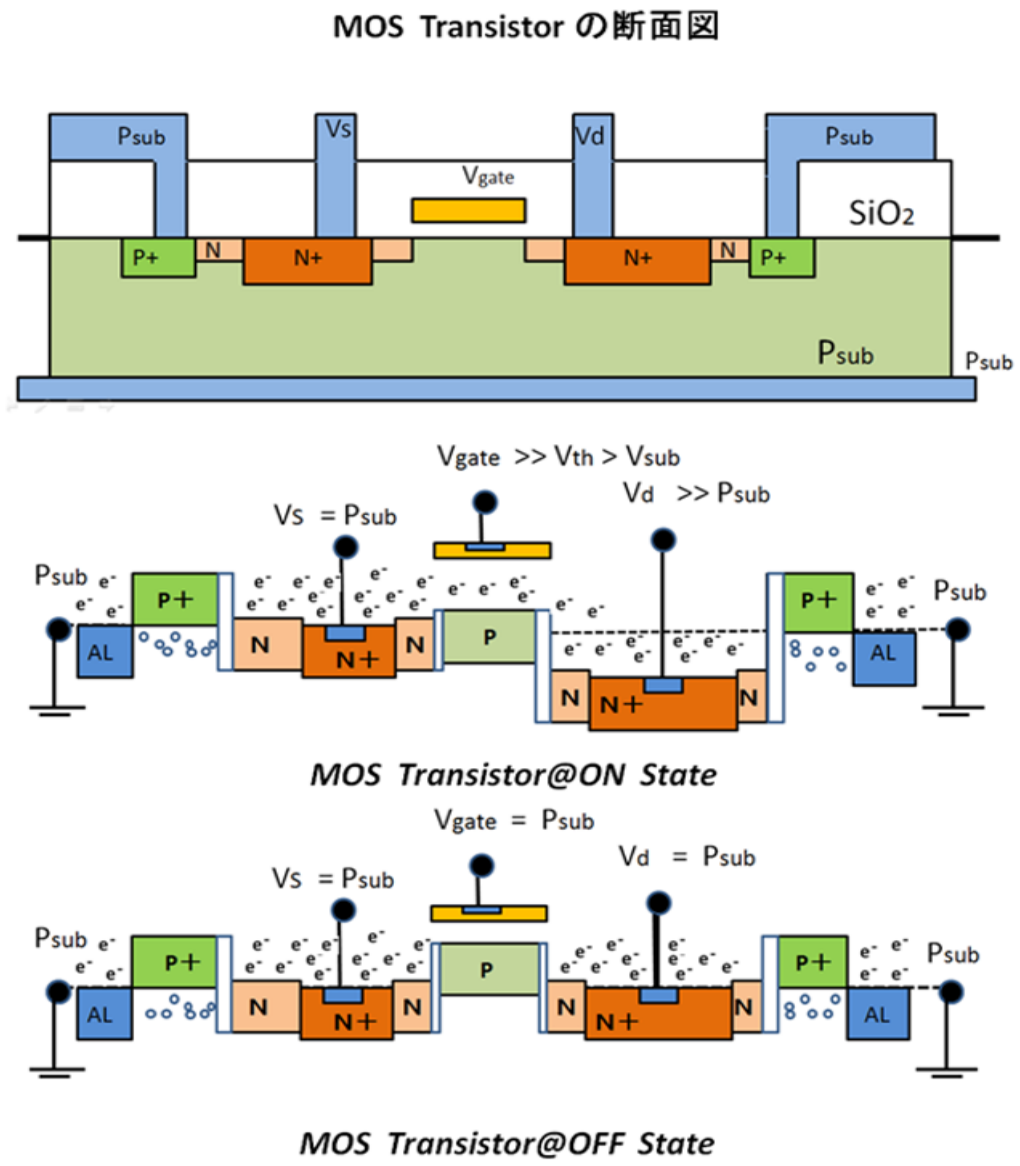
図 4-4-7




NMOS transistor のいろいろな物理定数とその関係式

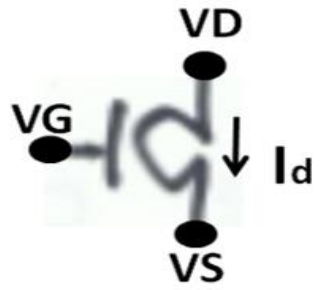
図 4-4-8

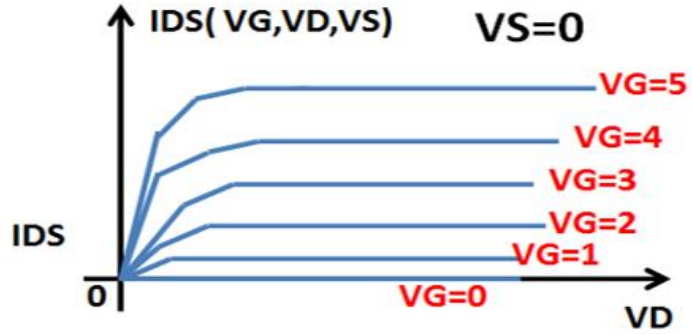



# NMOS transistor の断面図と layout 図

図 4-4-9

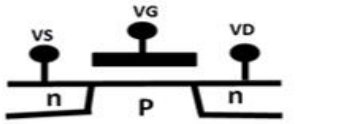


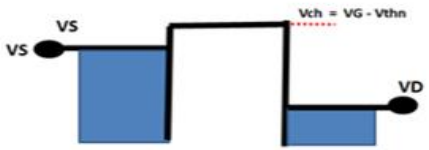




(1) Off Mode

When Vch = VG – Vthn < VS ,

Id = 0 ;



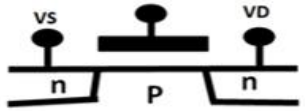



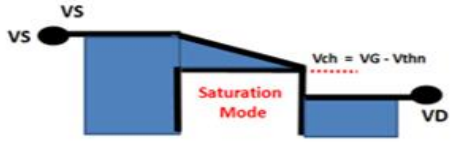

(2) Saturation Mode

When Vch = VG – Vthn < VD ,

B = 2 ( VG – Vthn - VS ) ;

$Id = B^2 / 2$ ;



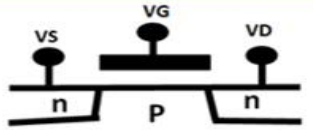



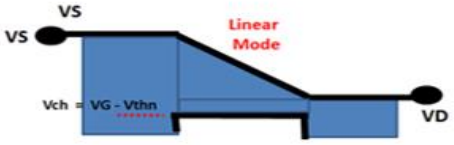

(3) Linear Mode

When Vch = VG – Vthn > VD ,

B = 2 ( VG – Vthn - VS ) ;

Id = (Vd –Vs){ B - (Vd-Vs)}/2 ;



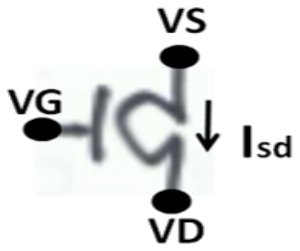



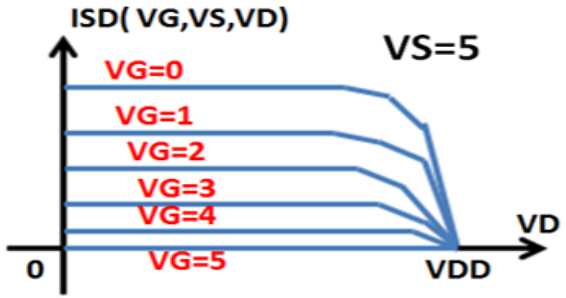

```
define  NMOS( ) { input VG,VD,VS ;  output IDS ; Vthn=0.1;

 /* Off Mode */                  B= 2 ( VG-Vthn-VS) ; if B<0 , return 0 ;
/* Saturation Mode */            Vch=VG-Vthn; if Vch < VD, return B*B/2 ;
/*Linear Mode*/                 return  (VD-VS)(B-(VD-VS))/2;          }
```

# NMOS transistor の 電流電圧（Ｉvs Ｖ）特性のまとめ

図 4-4-10

PMOS　Transistor の　I/V 特性




(1) Off Mode

When Vch = VG + Vthp > VS ,

Isd = 0 ;

(2) Saturation Mode

When Vch = VG + Vthp > VD ,

B = 2 ( VS - VG - Vthp ) > 0 ;

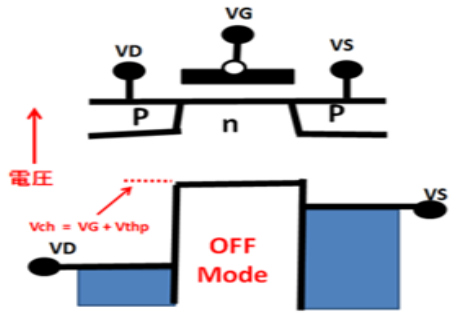
Isd = $B^2$ / 2 ;

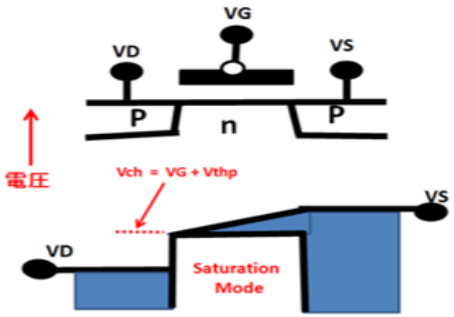
(3) Linear Mode

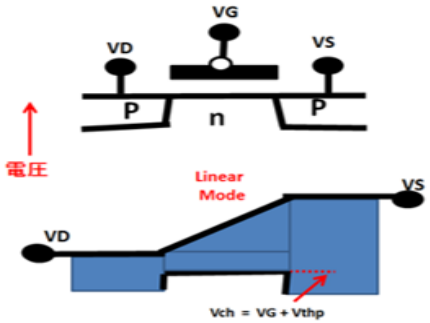
When Vch = VG +Vthp < VD ,

B = 2 ( VS - VG - Vthp ) > 0 ;

Isd = (Vs –Vd){ B - (Vs-Vd)}/2 ;



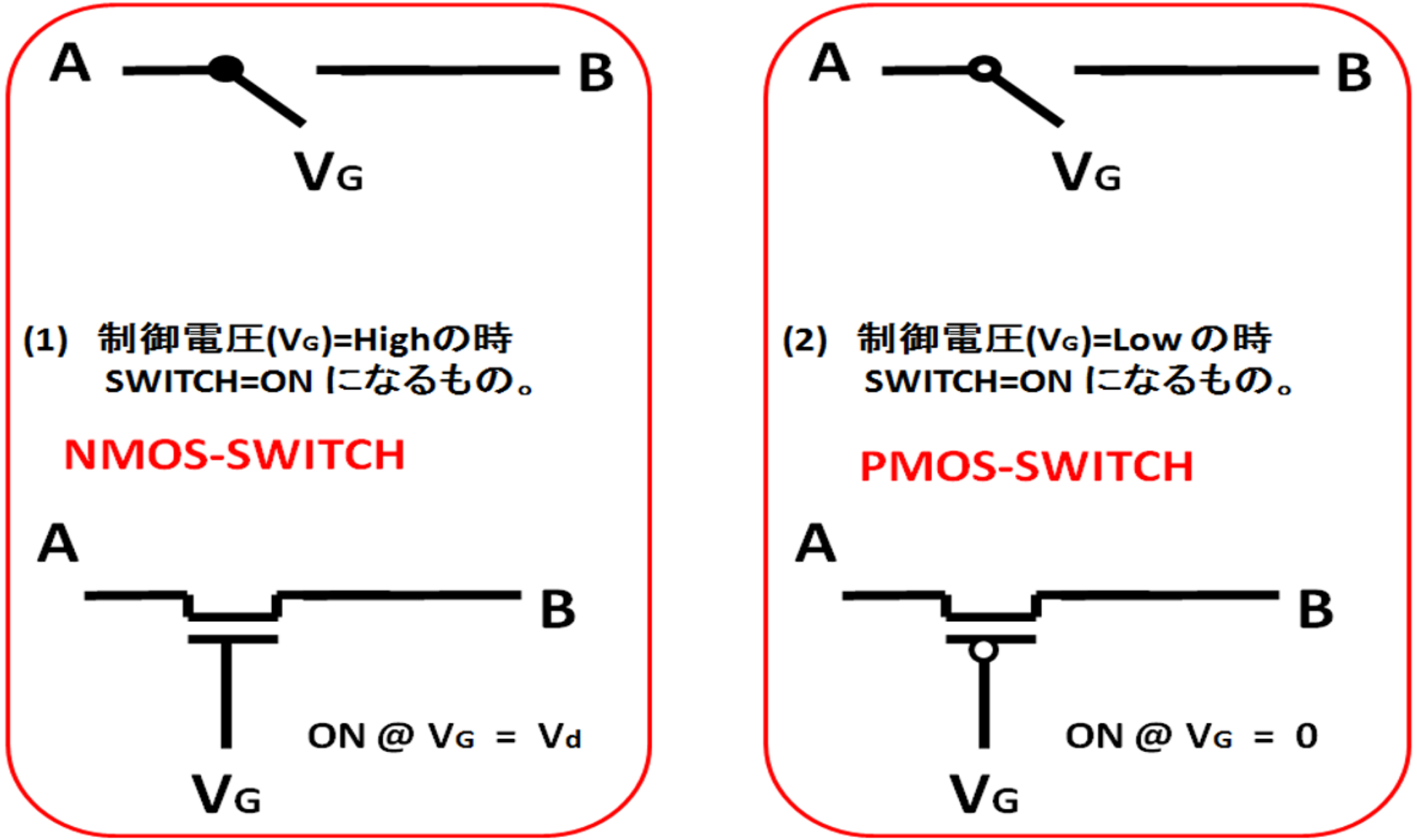




```
define  PMOS( ) {  input VG,VS,VD ;  output ISD ; Vthp=0.2;

 /* Off Mode */                  B=2( VS-VG-Vthp); if B<0 , return 0 ;
/* Saturation Mode */            Vch=VG+Vthp; if Vch > VD, return B*B/2 ;
/*Linear Mode*/                 return  (VS-VD)(B-(VS-VD))/2;              }
```

# PMOS transistor の 電流電圧（Ｉvs Ｖ）特性のまとめ

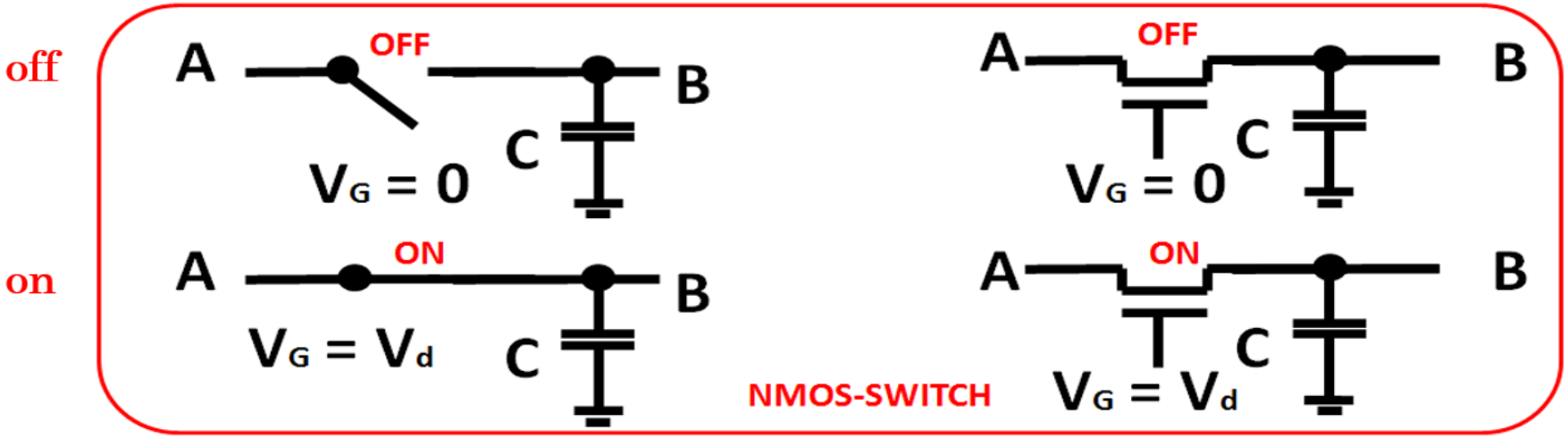
図 4-4-11



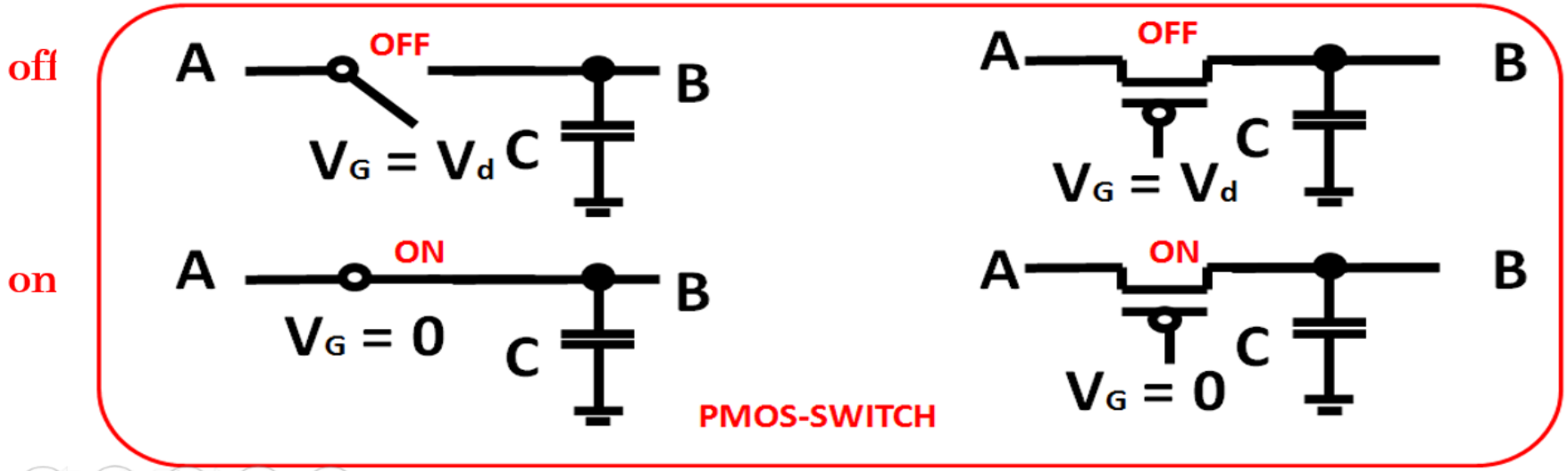

2 種類のデジタル Switch 回路

図 4-4-12

NMOS switch 回路　SwitchN(　)

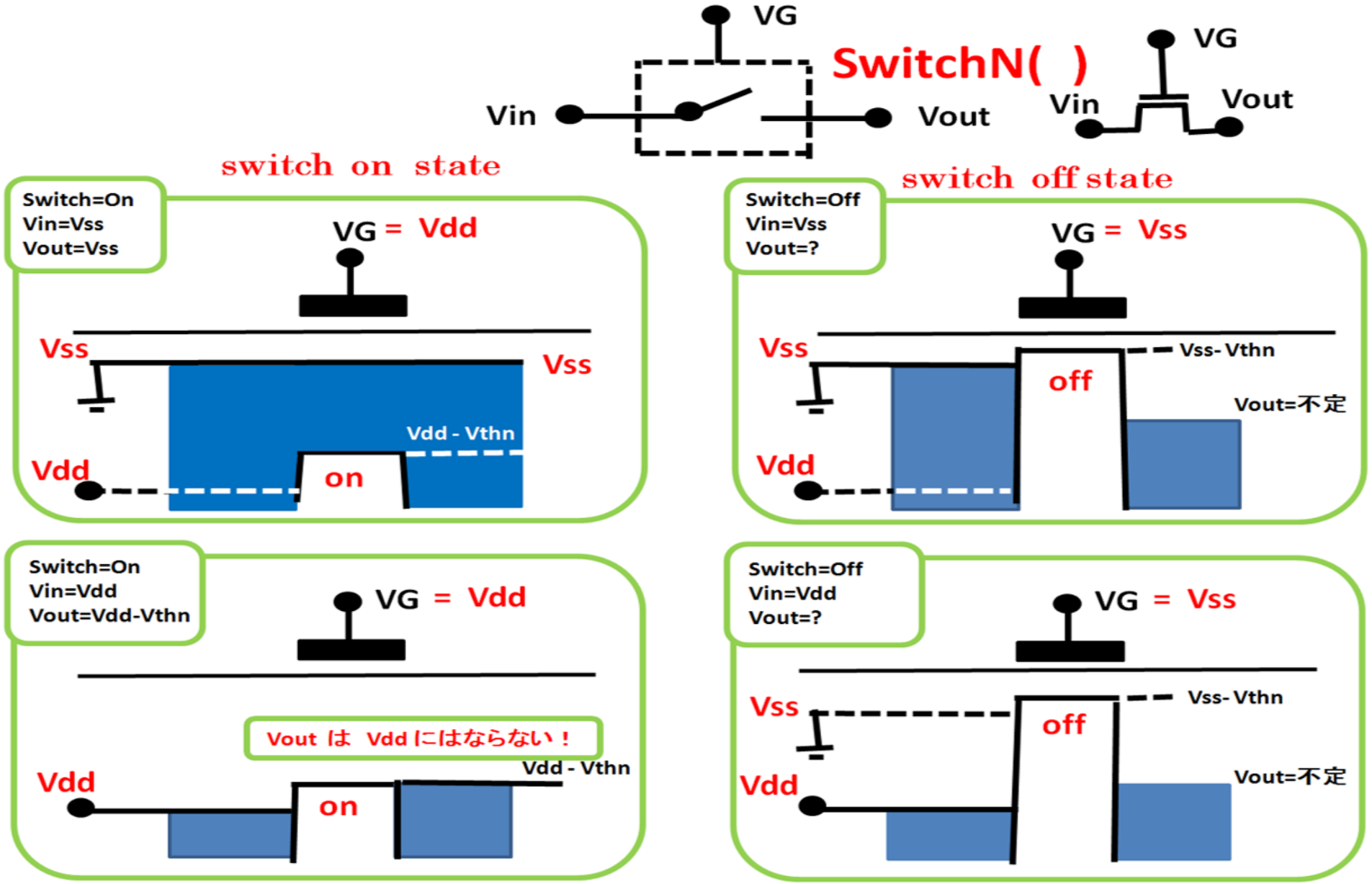



PMOS switch 回路　SwitchP(　)



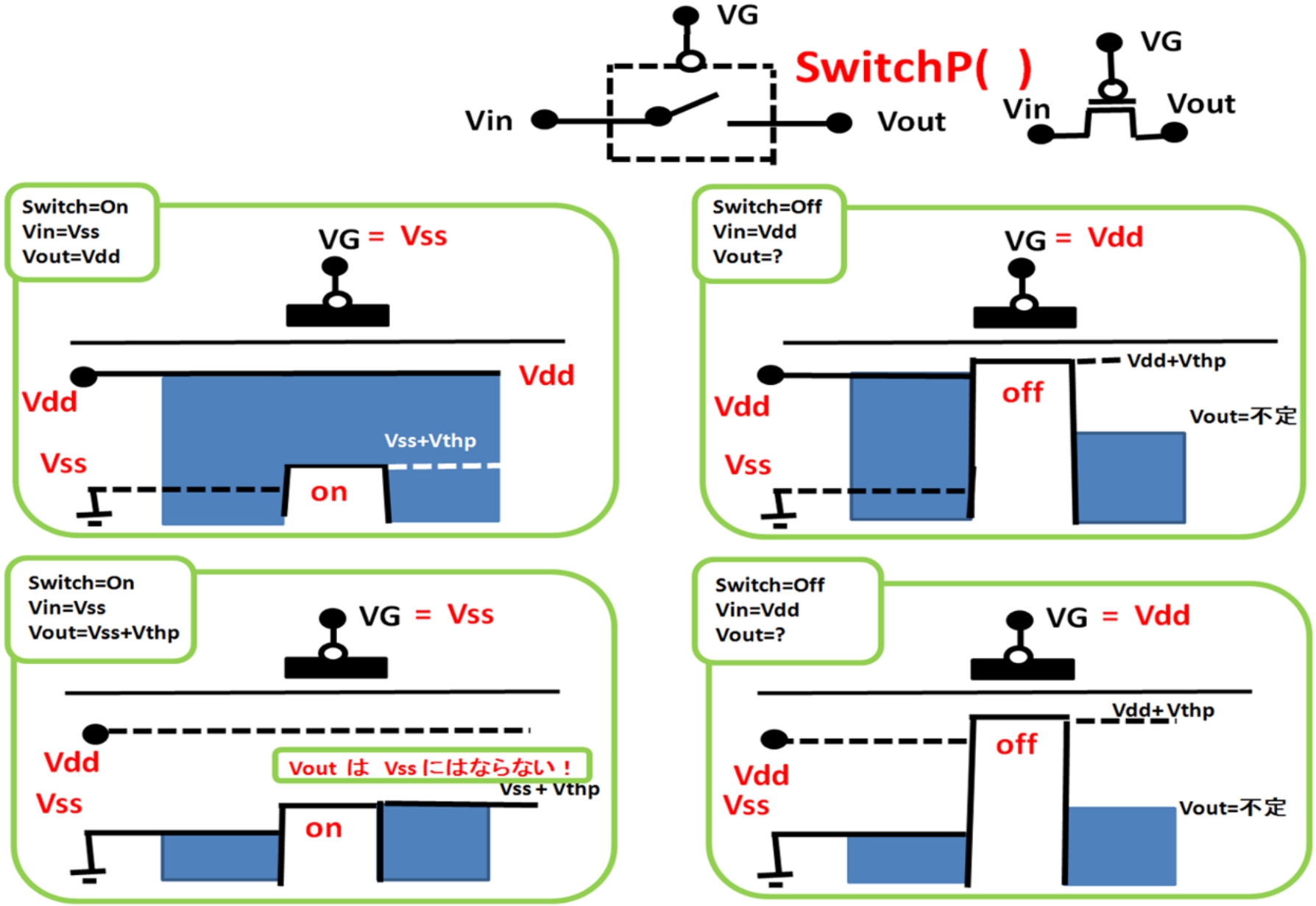

2 x 2 ＝ 4 通りの Switch 回路の状態

図 4-4-13(1)




SwitchN( )回路の入出力特性

図 4-4-13(2)

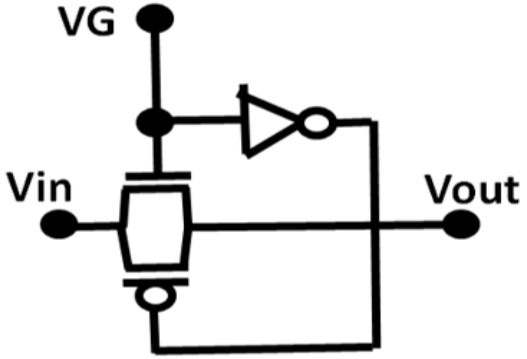


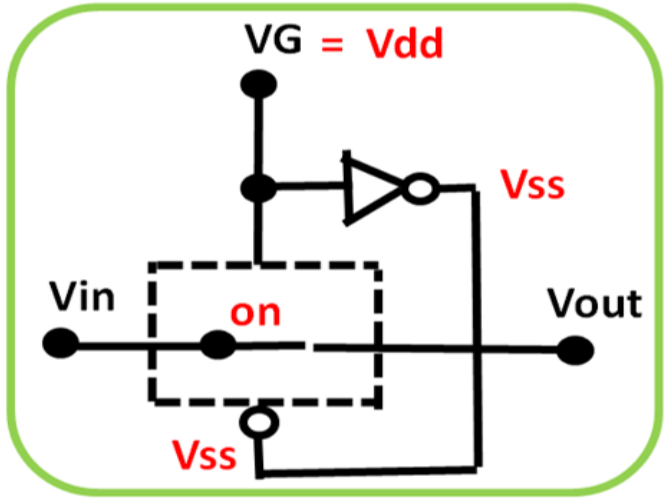

SwitchP( )回路の入出力特性

図 4-4-14(1)

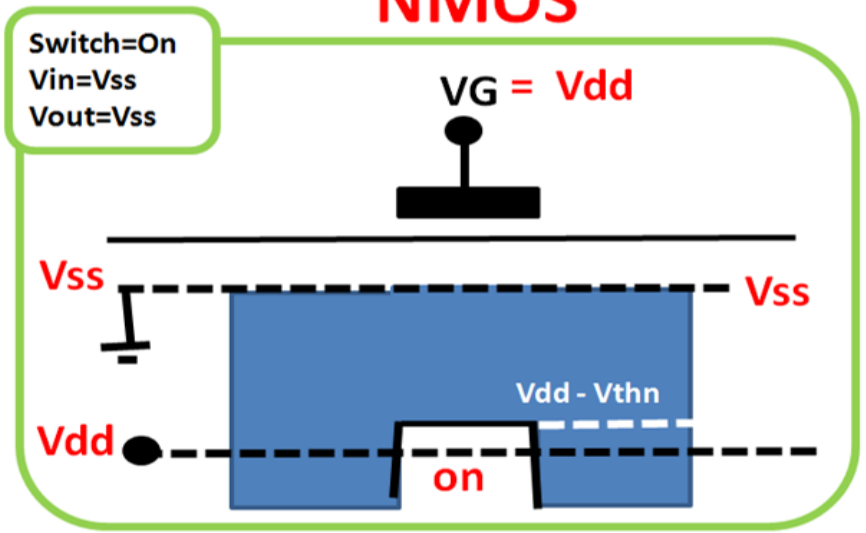
SwitchCN( )

when Vin=Vss

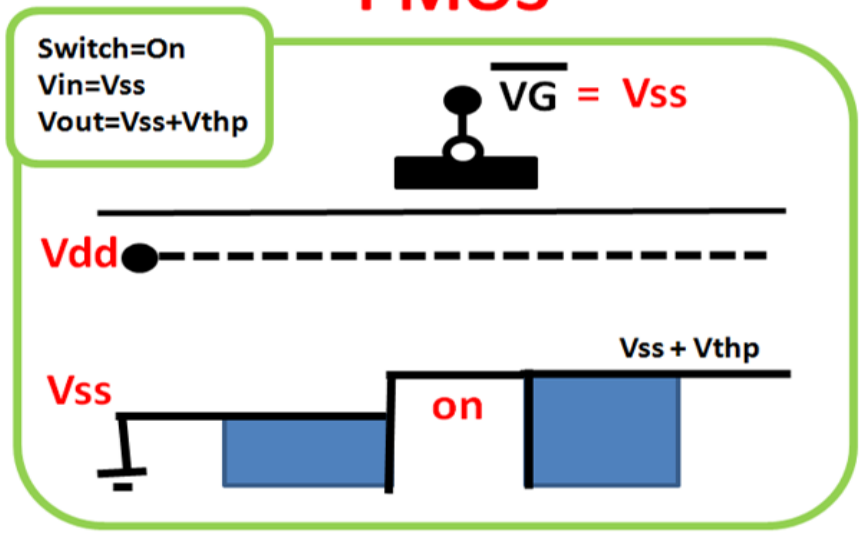



NMOS




PMOS



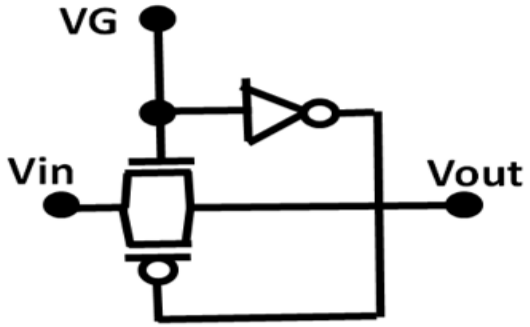

( PMOS alone cannot make Vout equal to Vss without NMOS)

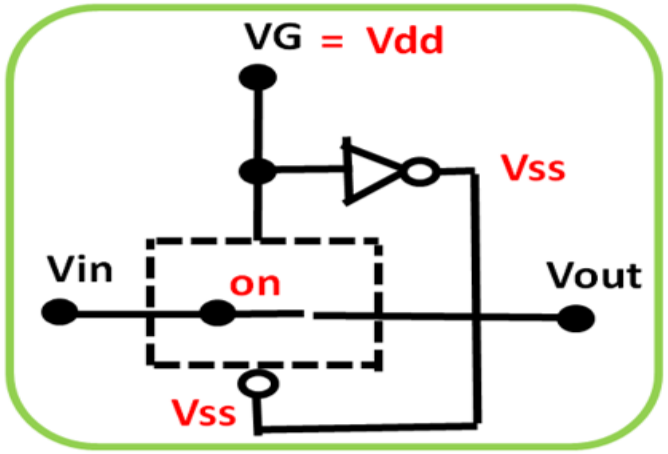
SwitchCN( )回路の入出力特性 Vin=Vssの場合

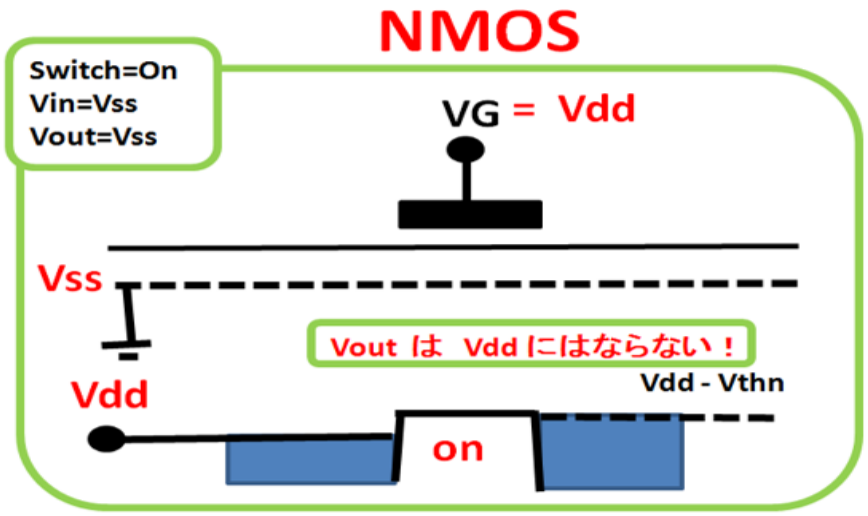
図 4-4-14(2)

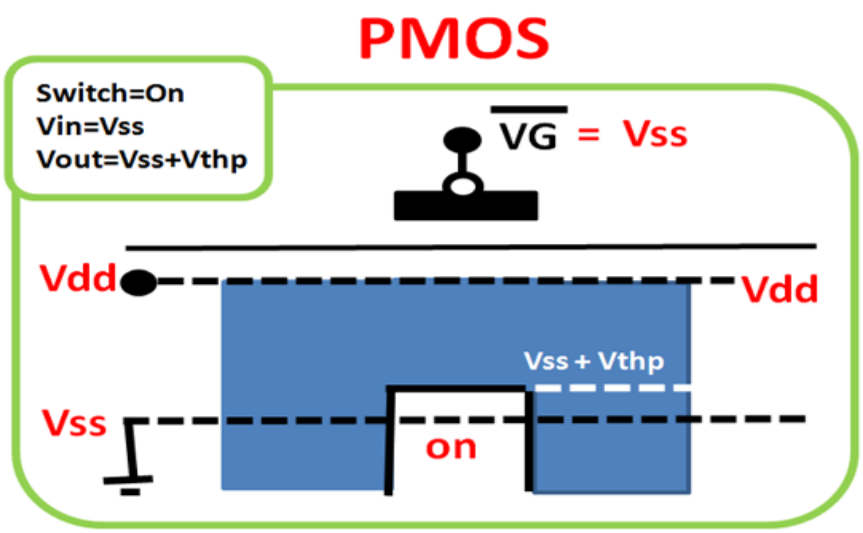
SwitchCN( )

when Vin=Vdd



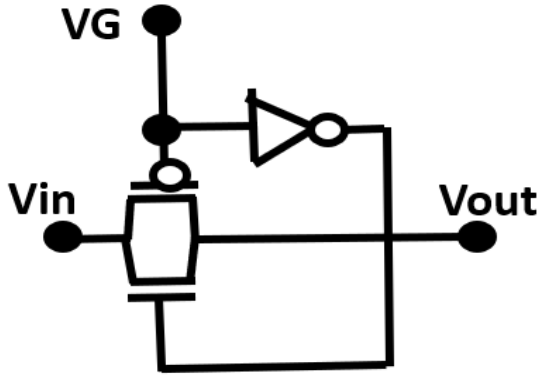

( NMOS alone cannot make Vout equal to Vdd without PMOS )

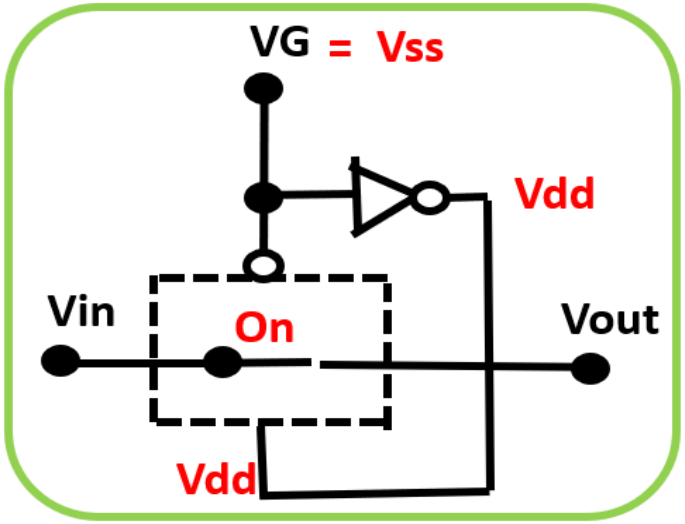
SwitchCN( )回路の入出力特性 Vin=Vddの場合

図 4-4-15(1)

SwitchCP( )

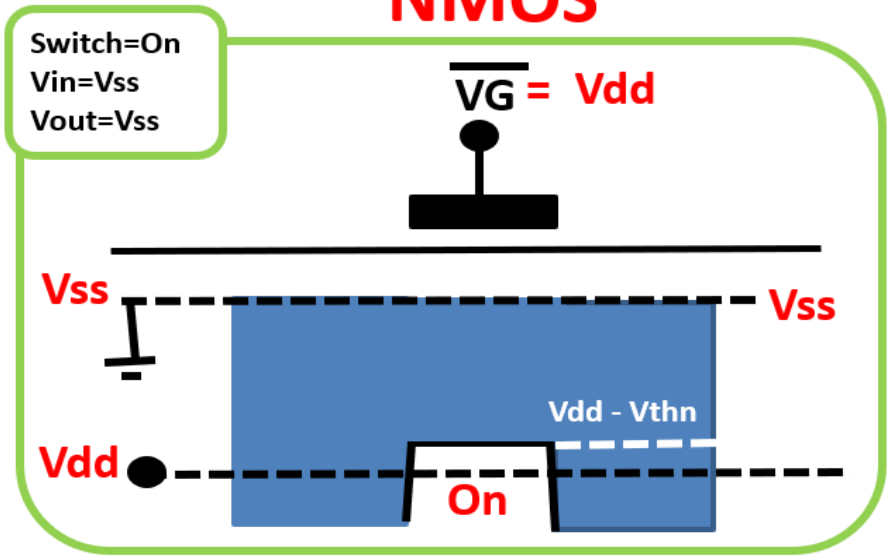
when Vin=Vss



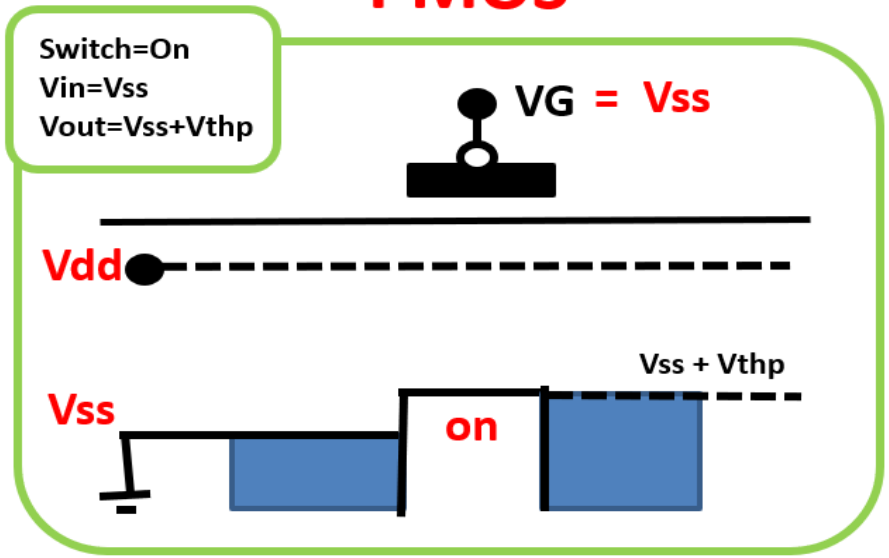

NMOS

Switch=On
Vin=Vss
Vout=Vss




PMOS

Switch=On
Vin=Vss
Vout=Vss+Vthp



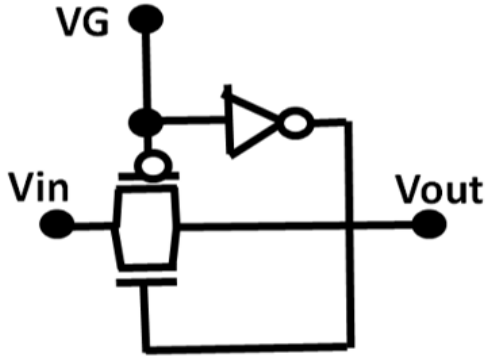

( PMOS alone cannot make Vout equal to Vss without NMOS)

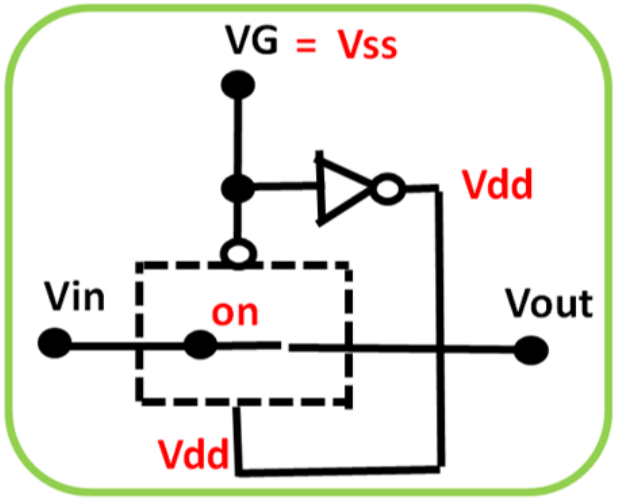
SwitchCP( )回路の入出力特性 Vin=Vss の場合

図 4-4-15(2)

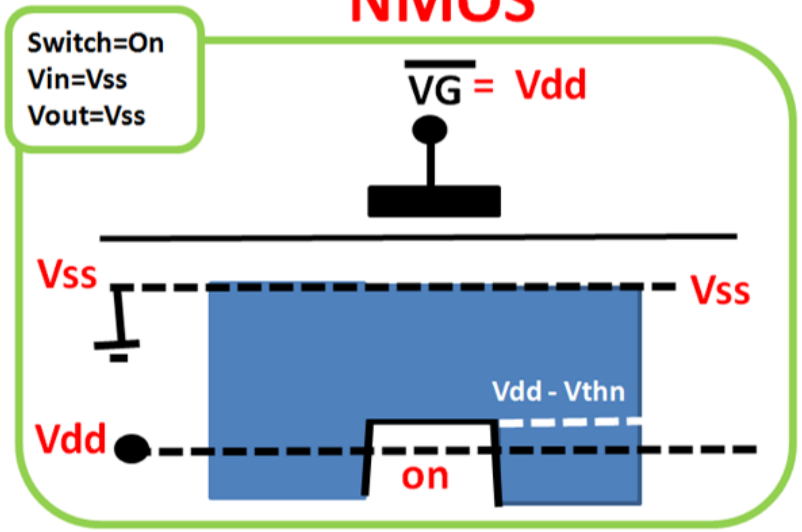
SwitchCP( )

when Vin=Vss

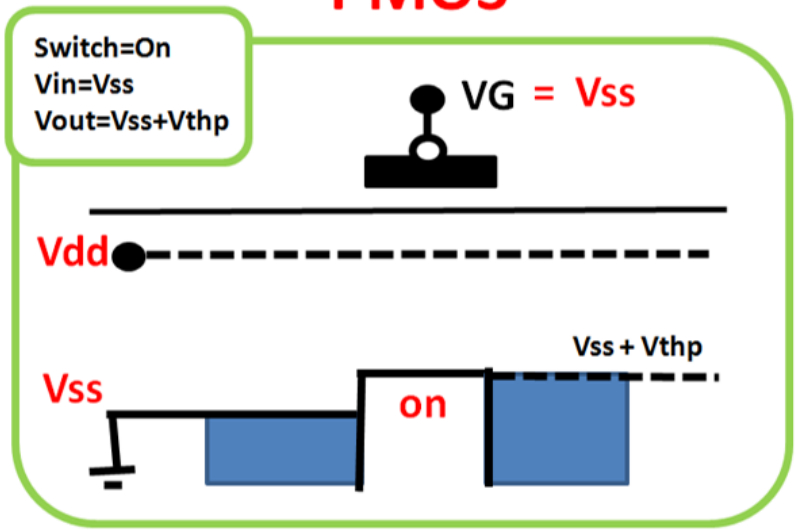



NMOS




PMOS

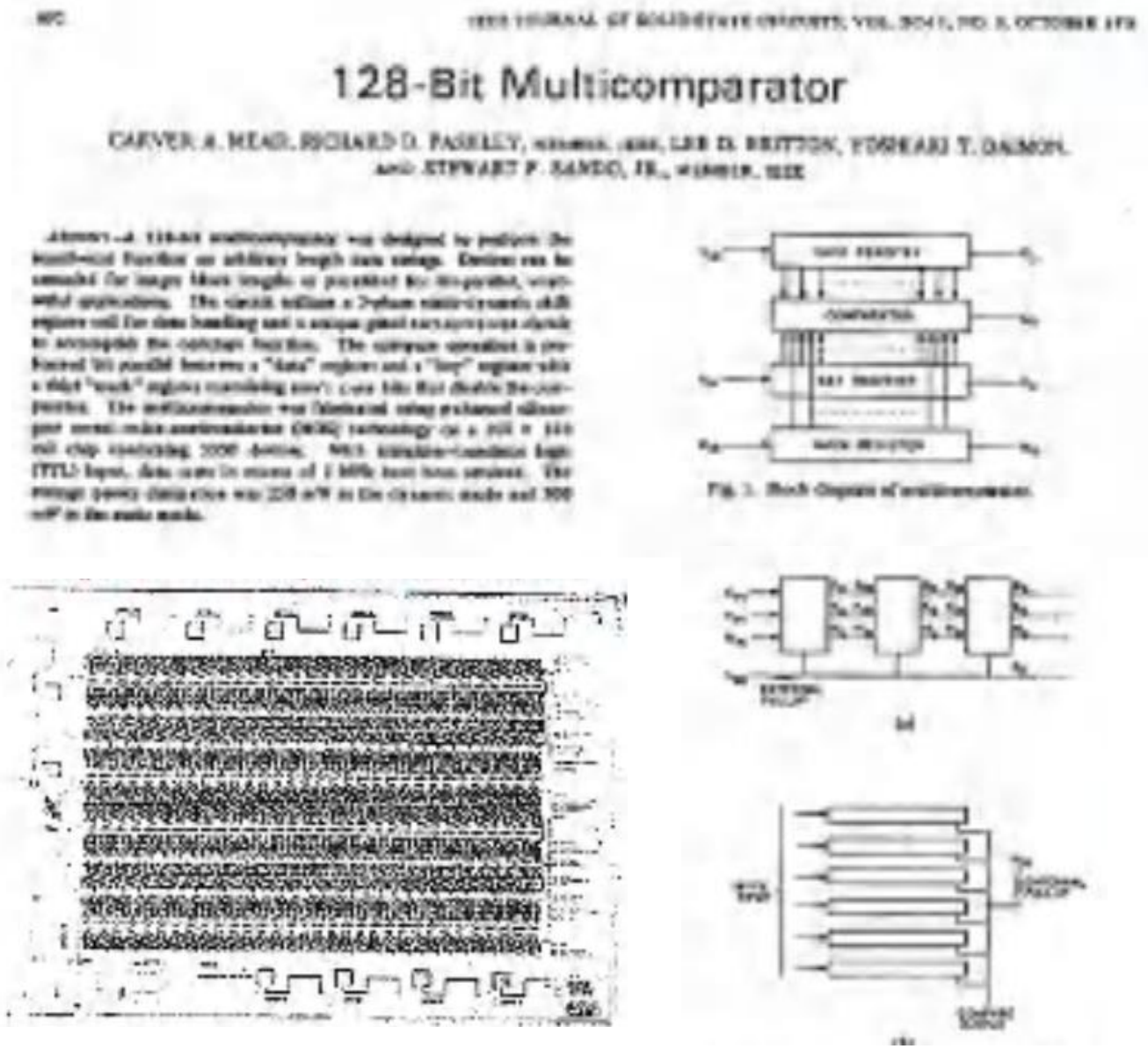



( PMOS alone cannot make Vout equal to Vss without NMOS)

SwitchCP( )回路の入出力特性 Vin=Vddの場合

# 128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

## Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976



128-Bit Multicomparator

CARVER A. MEAD, RICHARD D. PASLEY, [illegible], LEE D. BRITTON, YOSHIAKI T. DAIMON, AND STEWART F. SANDO, III, [illegible]

Prof. C. A. Mead and Yoshiaki Daimon Hagiwara working on the silicon chip design at Caltech in 1972

128-bit Multicomparator chip, designed by Hagiwara in 1972-1973 and fabricated by Intel PMOS process.

# 128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976

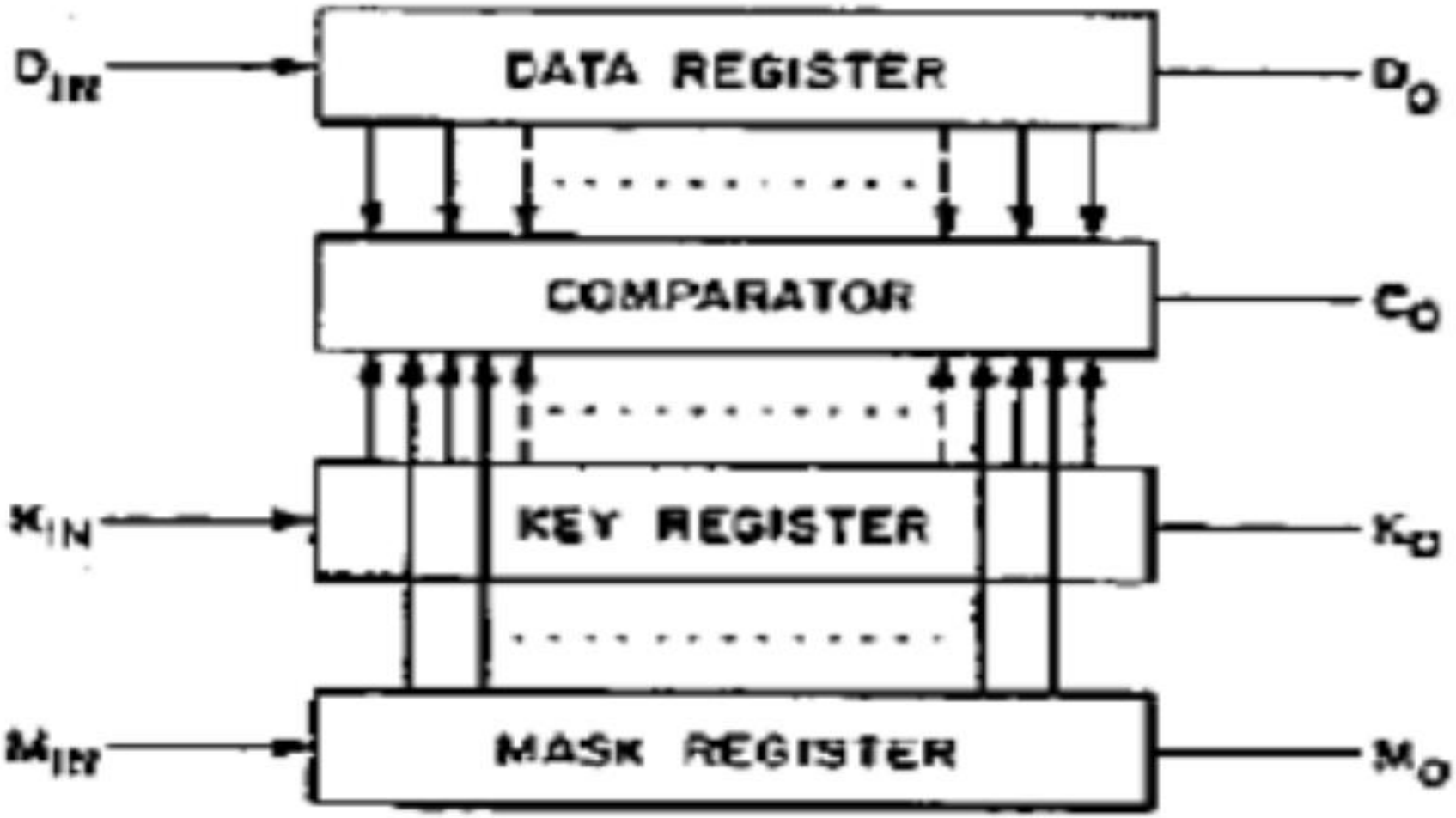



Fig. 1. Block diagram of multicomparator.

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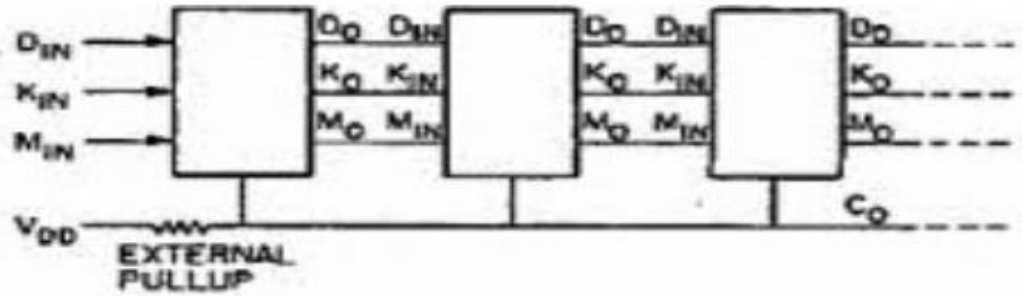
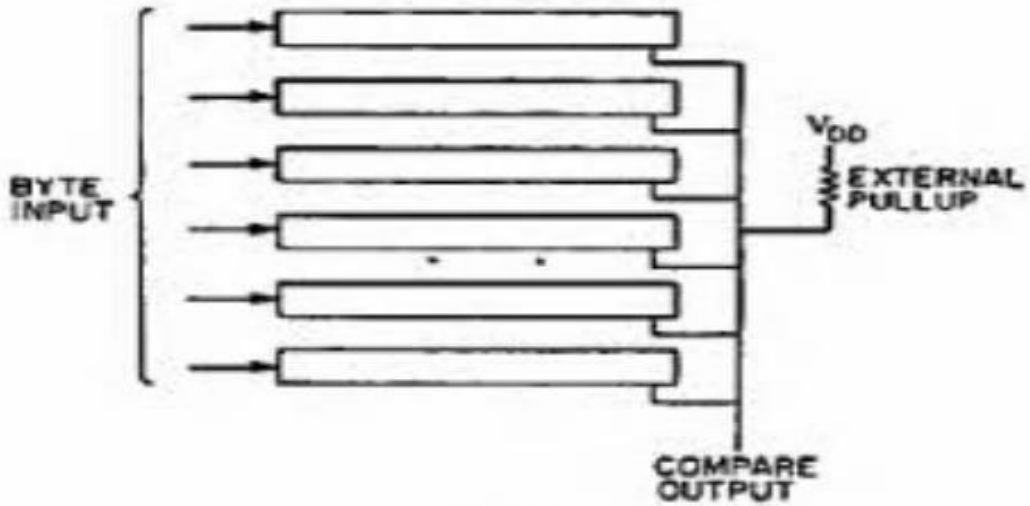



(a)




(b)

Fig. 2. Possible connections of multicomparator. (a) Cascaded. (b) Bit-parallel, word-serial.

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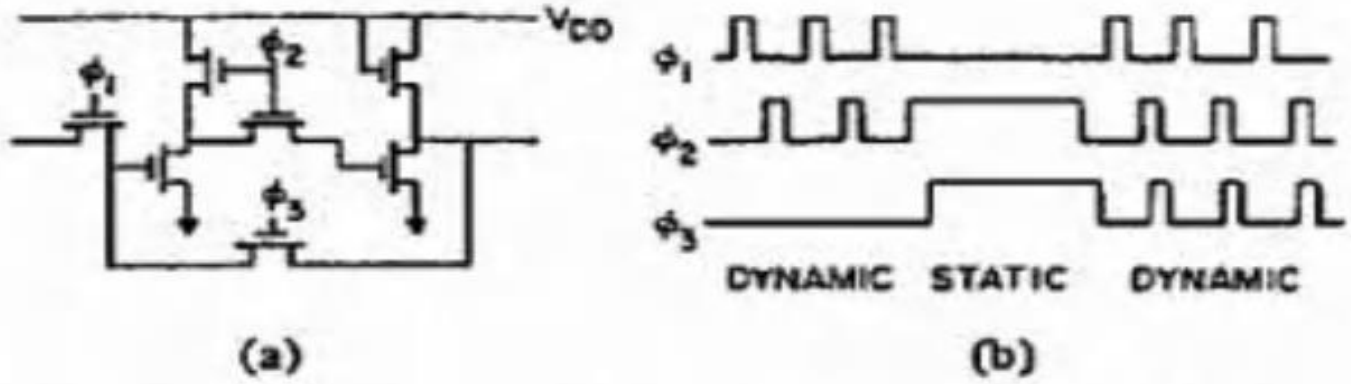


Fig. 3. Basic shift register cell. (a) Schematic. (b) Clock timing.

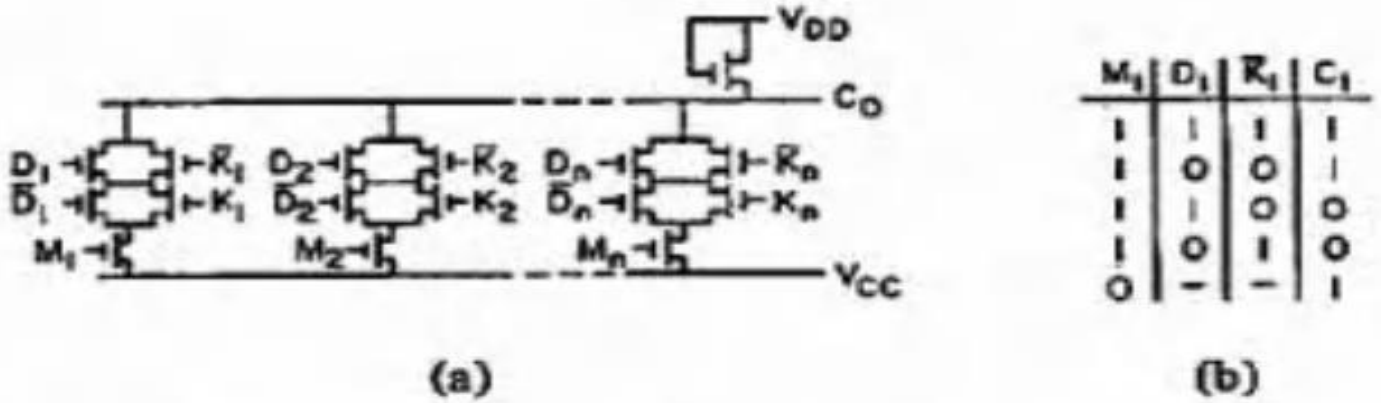


Fig. 4. Gated EXCLUSIVE-NOR gate. (a) Schematic. (b) Truth table.

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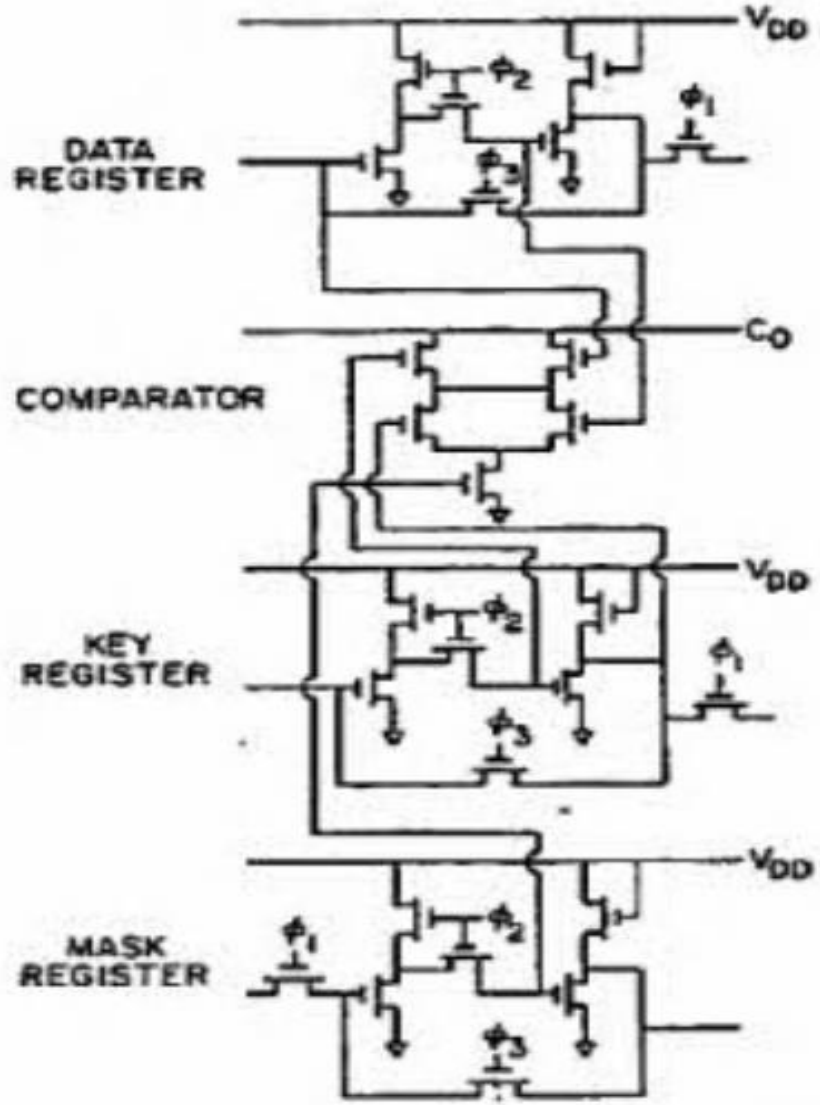


Fig. 5. Full schematic of one bit slice of the multicomparator.

# 128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

**Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976**

*serial-in/serial-out fast 128 bit parallel data comparator chip*
*fabricated by Intel corporation p-channel E/D MOS fabrication line*

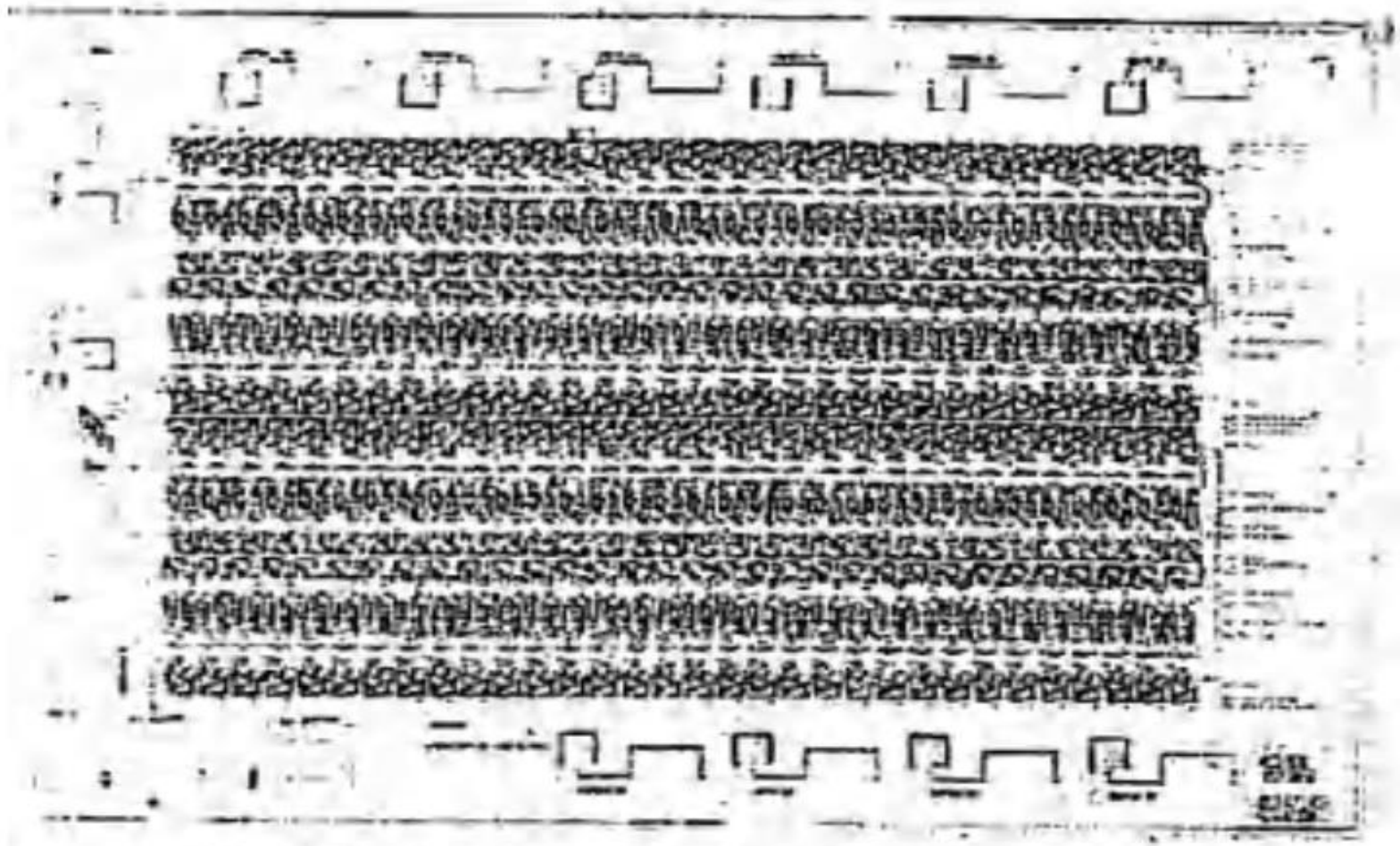

Fig. 6. Photomicrograph of multicomparator chip.

# 128-Bit Multicomparator Chip designed by Caltech Students and fabricated by Intel.

Ref: IEEE Journal of Solid State Circuits, VOL.SC11, No.4, October 1976

TABLE I

| Parameter | Performance[a] |
|---|---|
| Clock rate | 0.0001–2 MHz |
| Dynamic supply current | 25 mA |
| Static supply current | 30 mA |
| Clock leakage current ($\phi_1$) | 120 nA |
| Clock leakage current ($\phi_2$) | 300 nA |
| Clock capacitance ($\phi_1$) | 40 pF |
| Clock capacitance ($\phi_2$) | 60 pF |
| Clock capacitance ($\phi_3$) | 40 pF |
| Interclock capacitance | 7 pF |
| Input capacitance | 10 pF |
| Output capacitance | 10 pF |

[a] *Test Conditions:*

$$T = 23^{\circ}\text{C}, V_{cc} = 5\text{ V}, V_{DD} = -5\text{ V},$$

$$V_{\phi L} = +5\text{ V}, V_{\phi H} = -5\text{ V}, V_{\text{input}} = 0.5\text{ V}.$$

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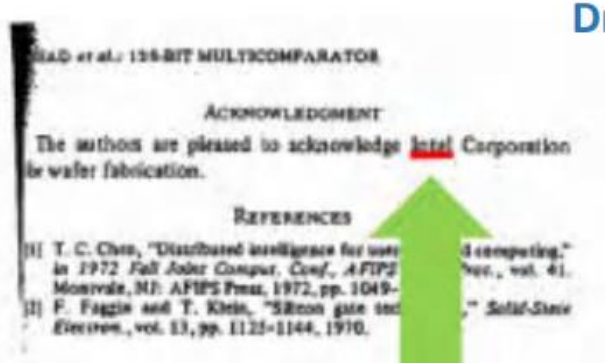

ACKNOWLEDGMENT

The authors are pleased to acknowledge Intel Corporation for wafer fabrication.

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[2] F. Faggin and T. Klein, "Silicon gate tec ," *Solid-State Electron.*, vol. 13, pp. 1125–1144, 1970.

**Dr. Lee Barton at Hewlett-Packard**
**Caltech Graduate, 1973**

Lee D. Brinton received the B.S.E.E. degree from the California Institute of Technology, Pasadena, in 1973.

He then invented and marketed a computer-aided memory for theater lighting control, and now works for Hewlett-Packard Laboratories, Cupertino, CA, designing and testing LSI integrated circuits for mini-computers.

**Dr. Yoshiaki Hagiwara at Sony**
**Caltech Graduate, 1975**

Yoshiaki Hagiwara was born in Kyoto, Japan, on July 4, 1948. He received the B.S., M.S., and Ph.D. degrees from the California Institute of Technology, Pasadena, in 1971, 1972, and 1975, respectively.

Since 1967, he has served several research groups in the Institute. He worked as a Data Processor in hydraulics from 1967 to 1969, engaging in the analysis of the pressure distribution of solitary waves, the influence of the geological features of a harbor upon the induced standing-wave amplitude in the harbor, and the diffusion mechanism of polluted objects in moving fluids. From 1969 to 1971, he worked as an Experimentalist in the Material Science Department and studied the switching and other electronic properties of newly developed amorphous alloys from the low temperature of 4 K to room temperature. From 1971 to 1975 he was a Research and Teaching Assistant both in the Electrical Engineering and Physics Departments at the California Institute of Technology. In the summer of 1971 and 1973, he visited Sony Corporation, Tokyo, Japan, as a Product-Appraisal Engineer at the Atsugi plant and engaged in developments and applications of bipolar technologies in video and power integrated circuits. He is presently with the Sony Corporation, Tokyo, Japan. His interests lie in the areas of digital and linear integrated circuit designs, the physics of microelectronics, and artificial intelligence.

**Prof. C.A.Mead at Caltech**

Carver A. Mead received S., M.S., and Ph.D. degrees from the a Institute of Technology, Pasadena, , 1957, and 1959, respectively.

He has been a member Faculty of the California Institute of D., Pasadena, CA, since 1957. His re as contributed to the understanding o ing in solids, current flow mechanis his dielectric films, metal-semiconduct rs, band energies in semiconductors, a onic processes in insulators. He has proposed and demonstr peration of a number of new solid-state electronic devices s several U.S. patents.

Dr. Mead is a Fellow of the American Physical and a member of Sigma Xi.

**Dr. Richard Pashley at Intel**
**Caltech Graduate, 1974**

Richard D. Pashley (M born in Ft. Belvoir, VA, on Septem 1947. He re-

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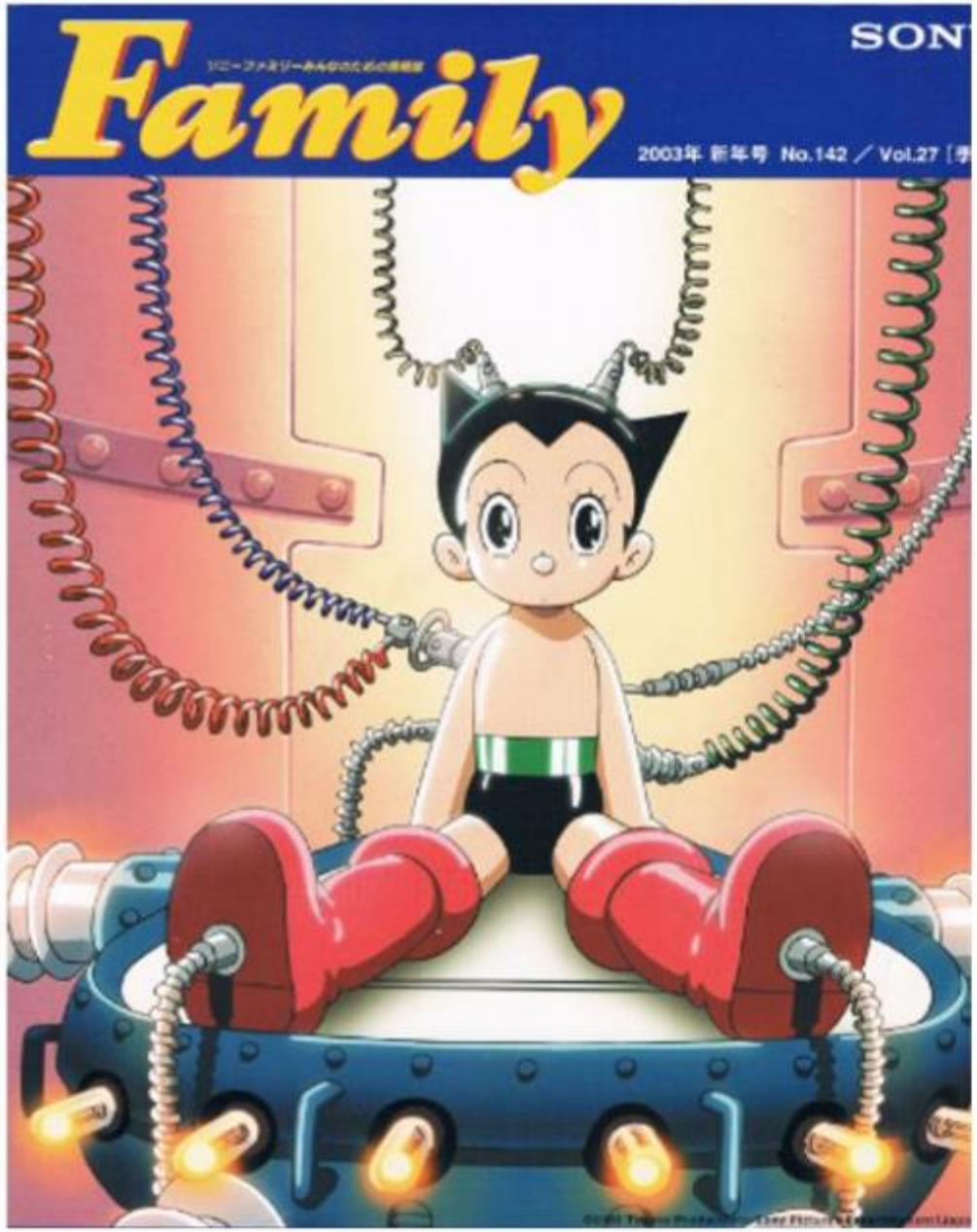


Sony Family Journal 2003 January Issue, No.142/Vol.27

**Yoshiaki Hagiwara was born on July 4, 1948 in Kyoto Japan. Graduated from Murasaki-no Elementary School in 1958. Lady Murasaki Shikibu is very famous as the writer of the story of Genji. Graduated from Rakusei Middle High School in 1961. Moved to Riverside-city in California USA in 1965 and graduated from Riverside City Polytechnique High School in 1967. Lived in Pasadena California since 1967 and received BS1971, MS1972 and PhD1975 in Electrical Engineering and Physics from California Institute of Technology (Caltech) . Joined Sony on February 1975 till July 2008. Taught at Sojo University as a professor till 2017. He is now serving for the ssis.or.jp.**

# Artificial Intelligent Partner System(AIPS) Home Page Top

hagiwara-yoshiaki@aiplab.com

Hello, my name is Yoshiaki Hagiwara. I am also called simply as Yoshi, and as Yoshiaki Daimon and also as Yoshiaki Daimon-Hagihara. I believe that I am the true inventor of the digital camera with the mechanical shutter function capability, which is completely filmless and free from mechanical parts. I worked at Sony from 1975 till 2008. My friends in Sony developed the digital camera in 1987. Sony is now enjoying image sensor business. Image sensors are very important to realize Artificial Intelligent AI robots and self-driving cars.

Evidence that Yoshiaki Hagiwara is the inventor of Pinned Buried Photodiode with in-pixel overflow Drain (VOD) function is given by the three basic Japanese Patent Applications, JPA1975-127646, JPA1975-127647 and JPA1975-134985.

Hagiwara also invented the in in-pixel Overflow Drain (OFD) Punch-thru Clocking Scheme to realize the completely-mechanical-part-free Electrical Shutter for digital cameras, opening a way to realize our modern digital TV world.

Evidence that Yoshiaki Hagiwara is the inventor of Electrical Shutter is given by the basic Japanese Patent Applications, JPA1977-126885.

The first Double Junction Pinned Buried Photodiode was developed by Hagiwara team at Sony in 1978. The first Triple Junction Pinned Buried Photodiode with Electrical Shutter function was developed by Hamazaki team at Sony in 1987.

**Yoshiaki Hagiwara joined Sony in Feb 1975 to build Artificial Intelligent Partner System(AIPS), which includes Artificial Intelligent Robot System, Artificial Intelligent Self-Driving Car, and Artificial Intelligent Vision Sensor System. His first work was developing the CCD image sensors. Hagiwara Team at Sony in 1989 developed 4M Cache SRAM for SNAPSHOT picture acquisition which opened a way to build the digital camera system. Hagiwara is also the inventor of the electrical shutter of the digital camera system.**

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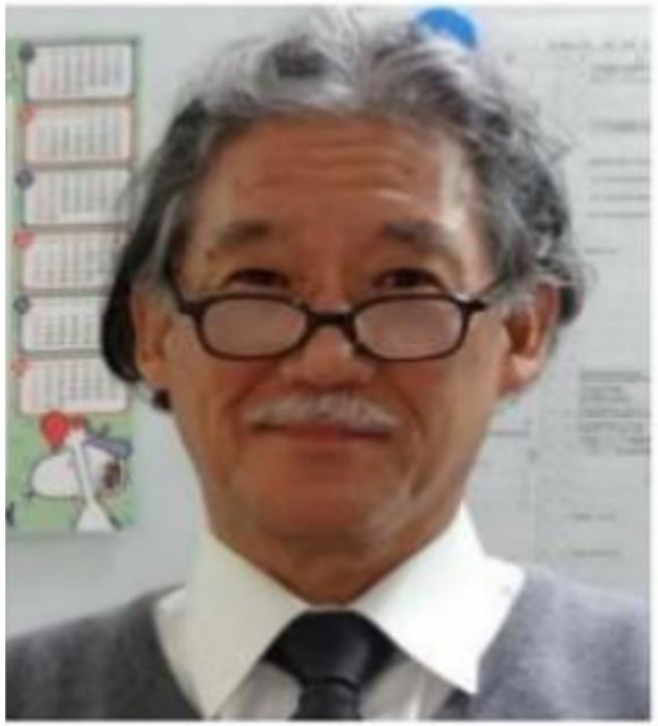


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**IEEE Life Fellow, Ph.D., 工学博士**



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