Fossum insulted in his 2014 paper Sony and Hagiwara 1975 PPD invention.

Indeed, Hagiwara invented PPD with VOD and the virtual charge transfer in 1975 !!

IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY, VOL. 2, NO. 3, MAY 2014 33

Sony HAD (PPD+VOD) does not use LOCOS !!!

A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, *Fellow, IEEE,* and Donald B. Hondongwa, *Student Member, IEEE*

False

Many people now said this is a fake paper !

C. Other Contributions to the PPD Invention

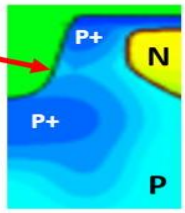
The PPD structure, while invented for low lag ILT CCD application, shares a strong resemblance to the Hynecek virtual-phase CCD structure, with the exception of the VOD. The two inventions were solving different problems with essentially the same device structure and operating principles.

In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top *p* layer was connected by metal to a bias used to control full-well capacity and the *n*-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called "Hole Accumulation Diode," or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the "narrow-gate" CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

The PPD, as it is most commonly used today, bears the strongest resemblance to the Teranishi et al. ILT CCD device. Thus, these days Teranishi is considered as the primary inventor of the modern PPD [29].

False

The surface P+ layer is NOT connected to the LOCOS P+ layer. The surface P+ layer may be floating and this photodiode may have serious image lag.



Serious Image Lag ?

NOT connected

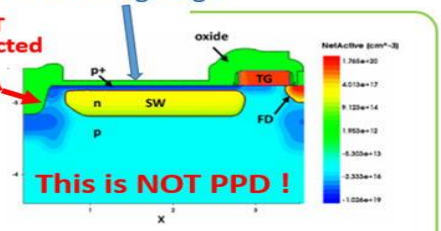


Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

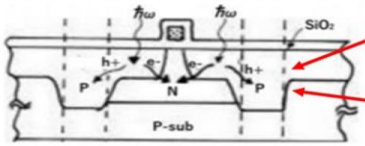
Hagiwara in 1975 invented PPD with VOD and the virtual charge transfer.
Study the Japanese Patents 1975-127646, 1975-127647 and 1975-134985.

True Historv of Photodiode

First Pinned Photodiode was invented by Hagiwara in 1975 and reported at SSDM1978 by Sony.

Sony never used LOCOS isolation nor Shallow Trench Isolation. Both suffer the yield problem of Dark Current and White Defects. Instead, Sony used high energy ion implantation to form the adjacent heavily doped P+ channel stops region with the Lamp Anneal Technology invented by Kazuo Nishiyama at Sony.

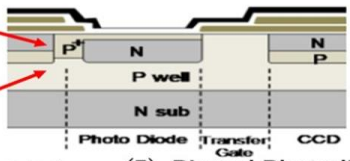
(1) The first Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation invented and reported at SSDM1978 by Hagiwara.



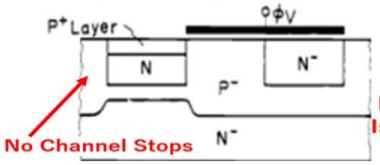
No LOCOS Isolation

No Shallow Trench Isolation

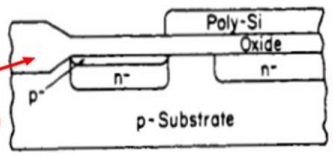
(2) Pinned Photodiode with the adjacent P+ channel stops and no LOCOS isolation as explained by ssis.or.jp in the official Semiconductor History Museum WEB site.



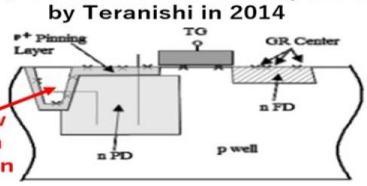
(3) Buried Photodiode reported at IEDM1982 by NEC



(4) Pinned Photodiode reported at IEDM1984 by KODAK



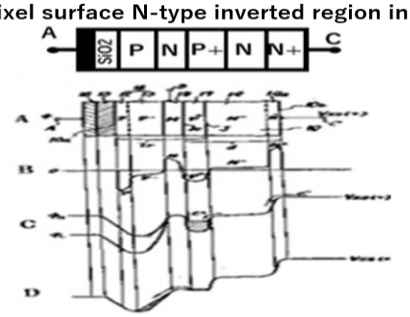
(5) Pinned Photodiode reported by Teranishi in 2014



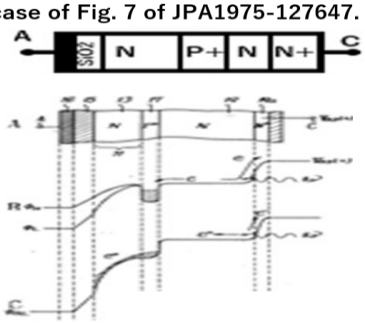
Sony Pinned Photodiode has the adjacent P+ heavily doped channel stops always directly grounded to the metal wire at the surface since 1978. Sony never used LOCOS isolation nor Shallow Trench Isolation.

Who invented Electric Shutter ?

Hagiwara at Sony invented Electric Shutter in October 23, 1975. The evidence is give and explained in Fig. 7 of the Japanese patent application, JPA1975-127646, in which the first Electric Shutter function was defined. The photo charge is transferred and drained to the in-pixel buried channel type vertical overflow drain (VOD) region, which is defined as the buried channel region of the buried channel type CCD/MOS buffer memory capacitor. The three-voltage-level clocking scheme (Clock C and D) of the first Electric Shutter Function mode was defined in Fig. 7 of JPA1975-127646, using the strong punch-thru action mode between the buried P type photo charge storage region and the P-type in-pixel vertical overflow drain (VOD) region. The strong draining gate clock D voltage as shown by creates the very deep potential well in the in-pixel P-type buried vertical overflow drain (VOD) region in case of Fig. 7 of JPA1975-127646 while the strong draining gate clock C voltage creates the very deep potential well in the in-pixel surface N-type inverted region in case of Fig. 7 of JPA1975-127647.



JPA1975-127646 Fig. 7



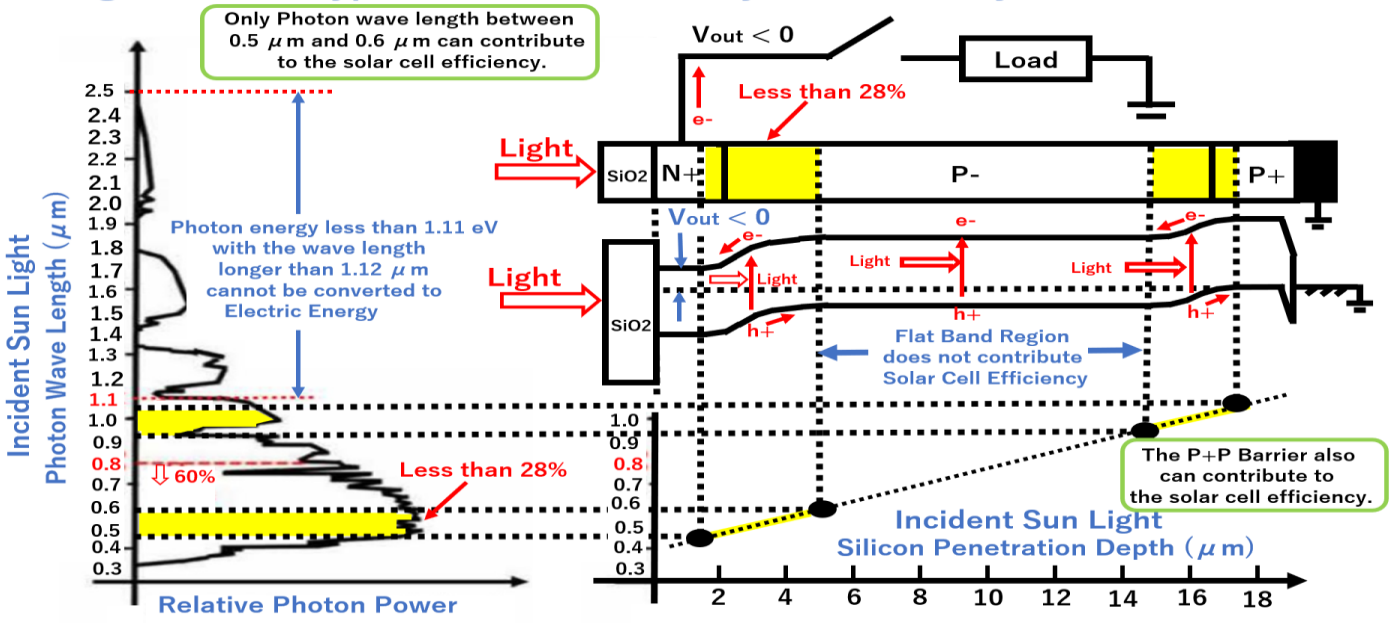
JPA1975-127647 Fig. 7

Hagiwara at Sony invented in 1975 the first Electric Shutter Function.

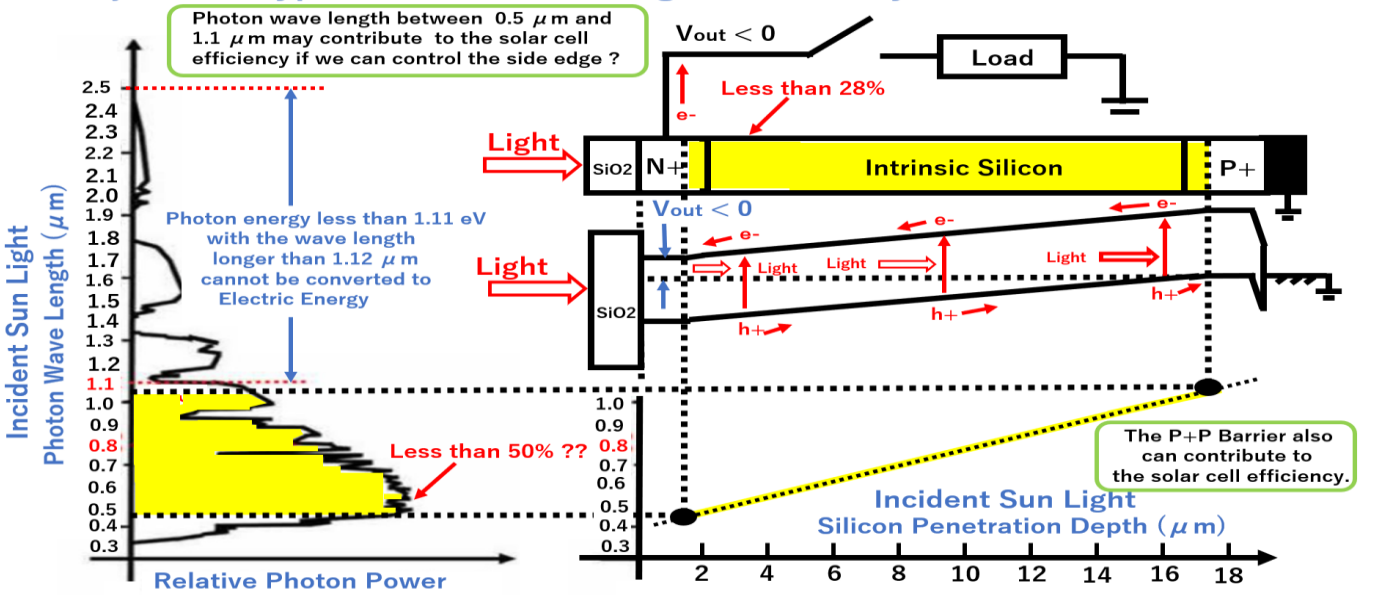
To achieve the complete Electric Shutter function, the surface of the photodiode must be pinned and fixed by the external constant voltage with the zero resistance.

The first Pinned Photodiode was invented by Hagiwara in 1975 to achieve the electric shutter function.

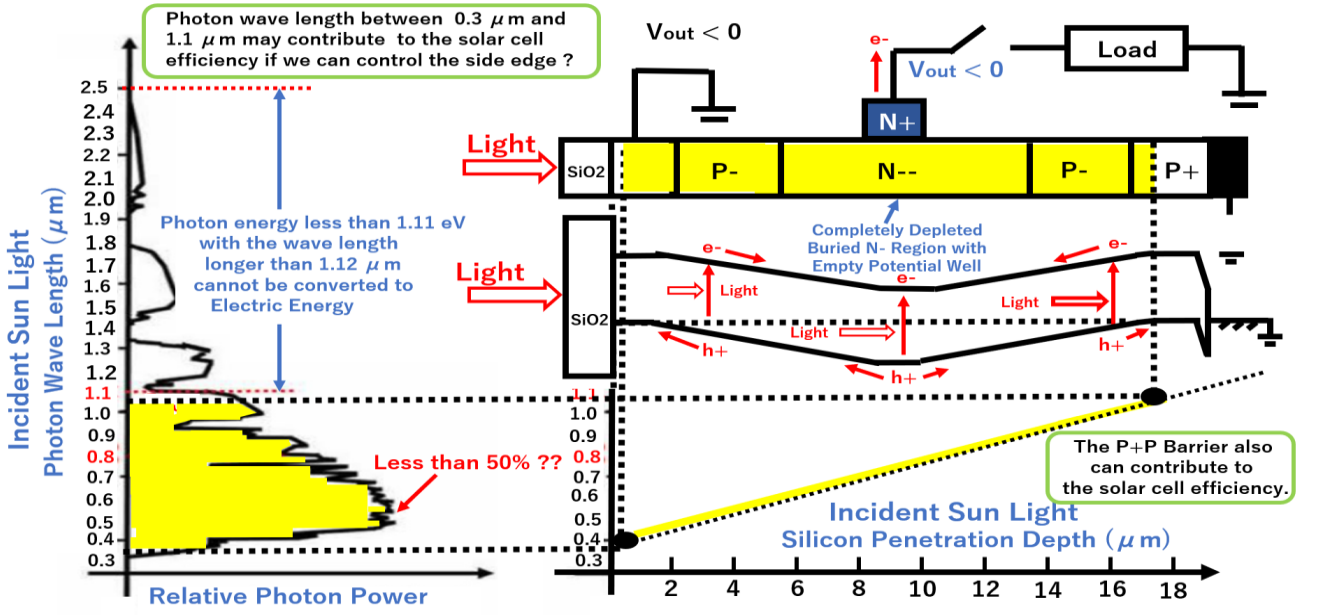
Single Junction type Solar Cell has a very low efficiency of less than 28%.



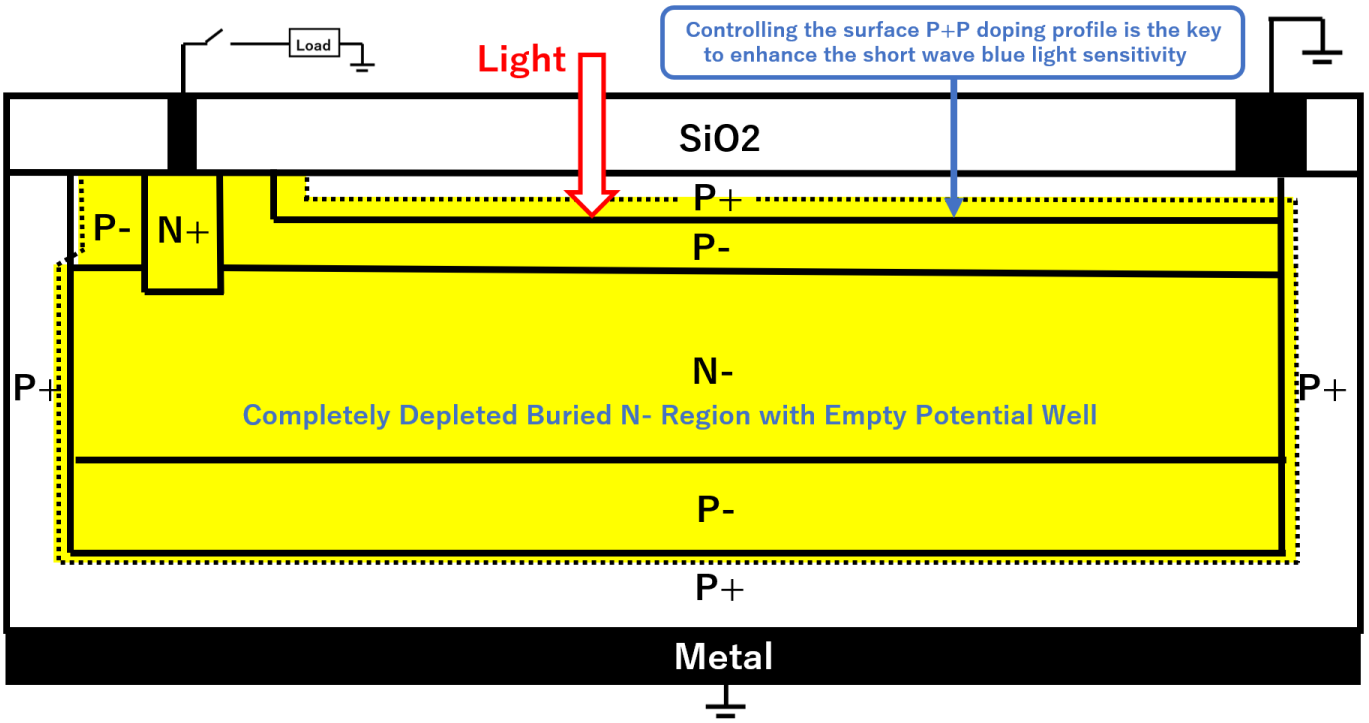
PIN junction type Solar Cell has a higher efficiency but still less than 28% ??



P+P-N-P-P+ double junction type Solar Cell may have much higher efficiency



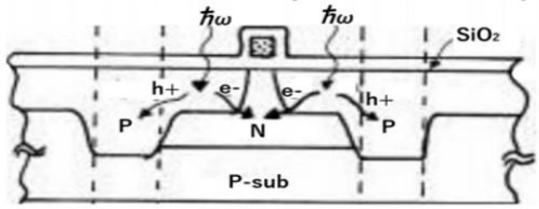
The newly proposed P+P-N-P-P+ junction type Solar Cell may have a higher efficiency.



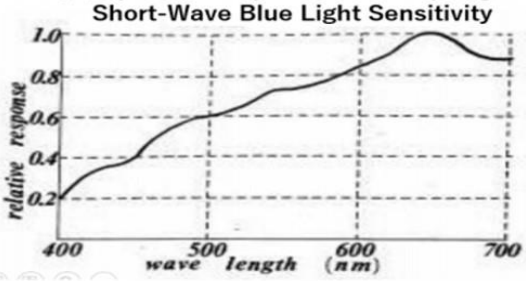
Wide Gap and Tandem Semiconductors were needed for the short-wave high-energy sun-light component to penetrate deep into the semiconductor crystal, where we can form the depletion region with the barrier electric field, which is needed to separate the photo electron and hole pairs. However, the surface P+P doping variation by the clever ion implantation technology can also create the surface barrier electric field for the short-wave blue light. This idea was confirmed in 1978 and reported in SSDM1978 by Hagiwara.

SSDM1978 paper on the PNP junction type Pinned Photodiode with the Pinned P+ surface connected to the adjacent P+ channel stops

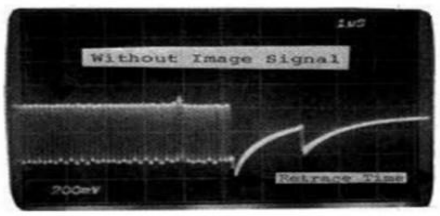
(A) Pinned-Surface and Buried-Storage PNP Photodiode with Adjacent Channel Stops



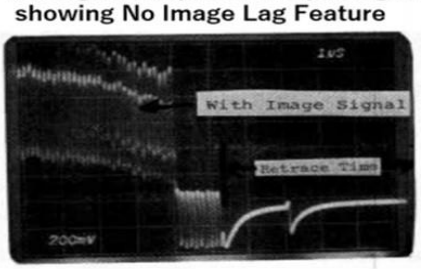
(B) Spectral Response with Very High Short-Wave Blue Light Sensitivity



(C) Signal Output with No Light showing Very Low Dark Current Feature



(D) Signal Output with Input Light showing No Image Lag Feature



Yoshiaki Hagiwara, Motoaki Abe and Chikara Okada, " A 380H x 488V CCD Imager with Narrow Channel Transfer Gates", Proceeding of 10th Conference on Solid State Devices, Tokyo 1978, Japanese Journal of Applied Physics, Volume 18 Sup 18-1, pp. 367-369.

True History of Photodiode

(1) Single Junction Type Dynamic Photodiode before 1970

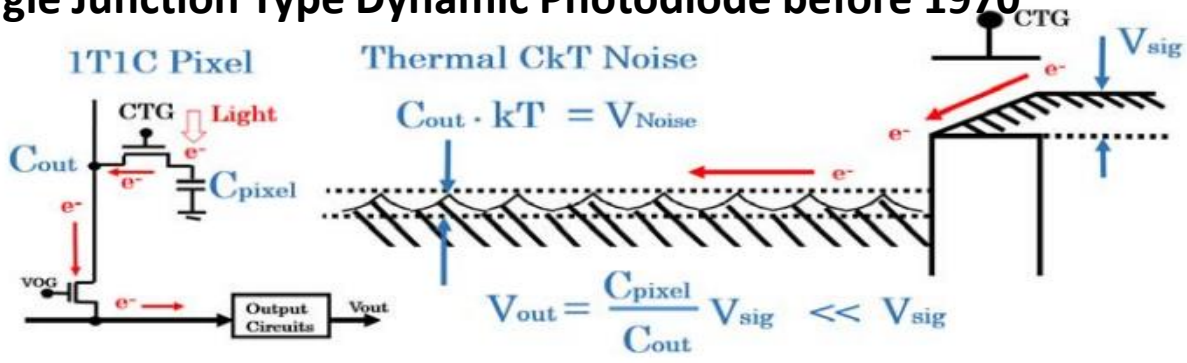
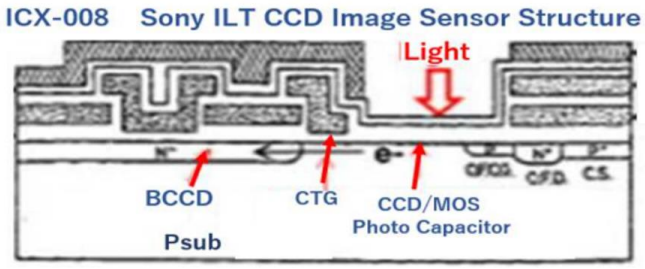


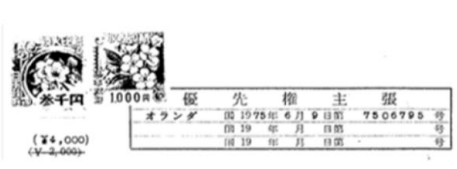
Figure 3. 1T1C type MOS Image Sensor with a Large Output Data Line Capacitance.

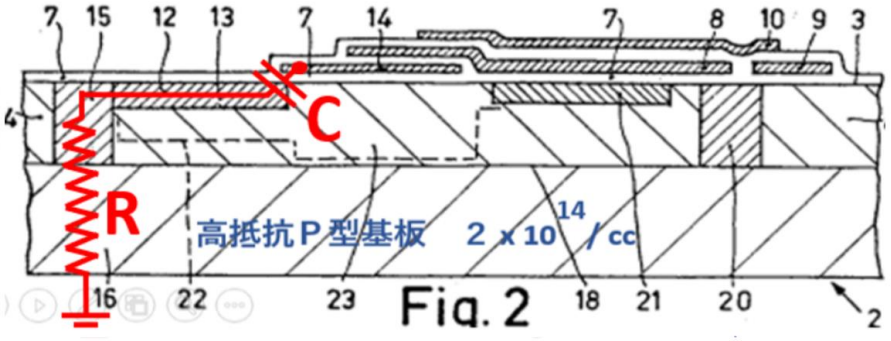
(2) CCD/MOS Capacitor type Dynamic Photodiode invented in 1970



SONY 1980 Two-chip CCD Color Video Camera XC-1.

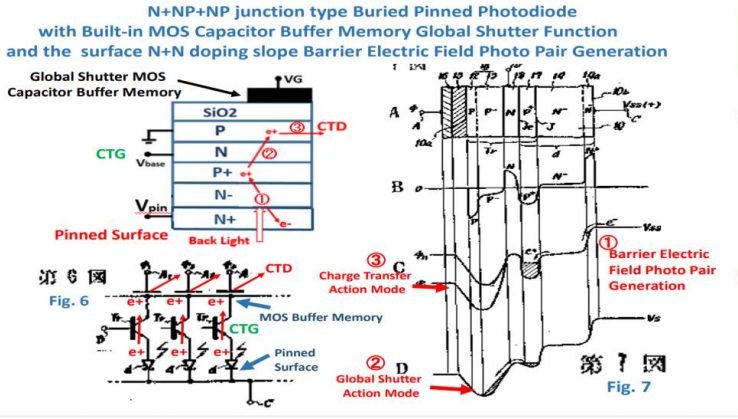
(3) Double Junction Buried Photodiode by Philips in June 6, 1975.

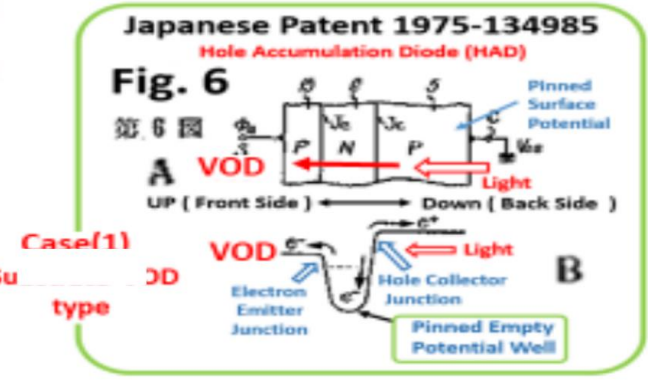




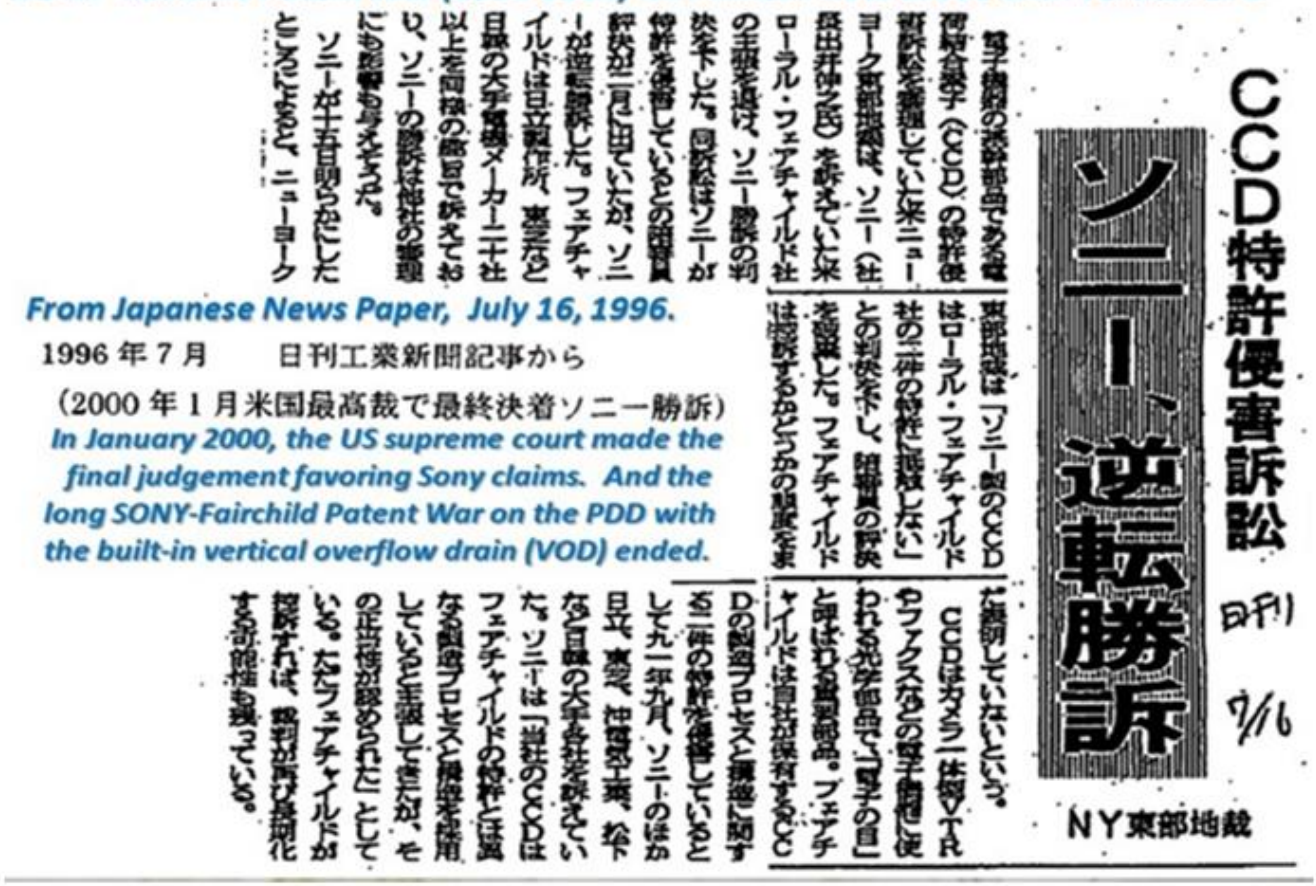
JPA1976-150288(Netherland Patent 7506795, priority June 7, 1975)

(4) Triple Junction type Pinned Photodiode with the pinned surface invented by Hagiwara at Sony in Oct 23, 1975.





SONY- Fairchild Patent War (1991-2000) on Pinned Photo Diode with Vertical OFD



CCD特許侵害訴訟

ソニー、逆転勝訴

NY東部地裁

日刊 7/16

電子機器の基幹部品である電荷結合素子（CCD）の特許侵害訴訟を審理していた米ニューヨーク東部地裁は、ソニー（社長出井伸之氏）を訴えていた米ローラル・フェアチャイルド社の主張を退け、ソニー勝訴の判決を下した。同訴訟はソニーが特許を侵害しているとの陪審員評決が二月に出ていたが、ソニーが逆転勝訴した。フェアチャイルドは日立製作所、東芝など日本の大手電機メーカー二十社以上を同様の訴訟で訴えており、ソニーの勝訴は他社の審理にも影響を与えそうだ。

ソニーが十五日明らかにしたところによると、ニューヨーク東部地裁は「ソニー製のCCDはローラル・フェアチャイルド社の二件の特許に抵触しない」との判決を下し、陪審員の評決を支持した。フェアチャイルドは控訴するかどうかの態度をまだ表明していないという。

CCDはカメラ一体型VTRやファクスなどの電子機器に使われる光学部品で「電子の目」とも呼ばれる基幹部品。フェアチャイルドは自社が保有するCCDの製造プロセスと構造に関する二件の特許を侵害しているとして九一年九月、ソニーのほか日立、東芝、仲電など十社、松下など日本の大手各社を訴えていた。ソニーは「当社のCCDはフェアチャイルドの特許とは異なる製造プロセスと構造を採用していると主張してきたが、その正当性が認められた」としている。ただフェアチャイルドが控訴すれば、裁判が再び長期化する可能性も残っている。

From Japanese News Paper, July 16, 1996.

1996 年 7 月　　日刊工業新聞記事から

（2000 年 1 月米国最高裁で最終決着ソニー勝訴）

In January 2000, the US supreme court made the final judgement favoring Sony claims. And the long SONY-Fairchild Patent War on the PDD with the built-in vertical overflow drain (VOD) ended.

Finally the Sony-Fairchild Patent Wat(1991-2000) ended over the Sony HAD Sensor which is identical to the P+NPNsub junction type Pinned Photodiode with Vertical Overflow Drain, originally invented by Hagiwara at Sony in 1975.

And finally Hagiwara received for his 1975-134985 Japanese Patent officially , the First Patent Award from Mr. Ando, Sony president in April, 2001 after more 26 years of struggles since his invention.

SONY

2000年度

発明考案実施褒賞

1級

萩原 良昭 殿

特許第1215101号

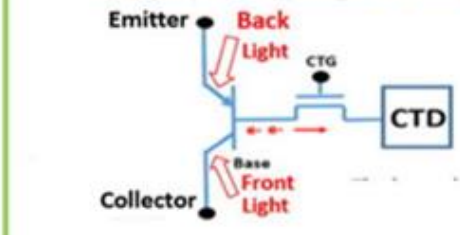
固体撮像装置

貴発明は卓越した創造性および先見性により
会社に対し顕著な貢献がありましたので
発明考案規定に基づき
ここに本賞を贈りこれを賞します

2001年4月26日

ソニー株式会社
社長
安藤 国威

Dynamic Photo Transistor Operation
Proposed by Hagiwara at Sony in 1975



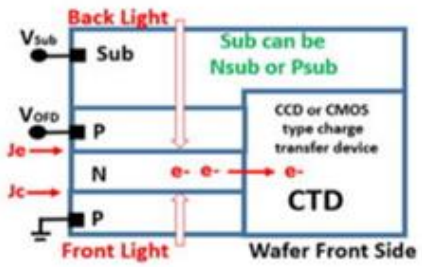
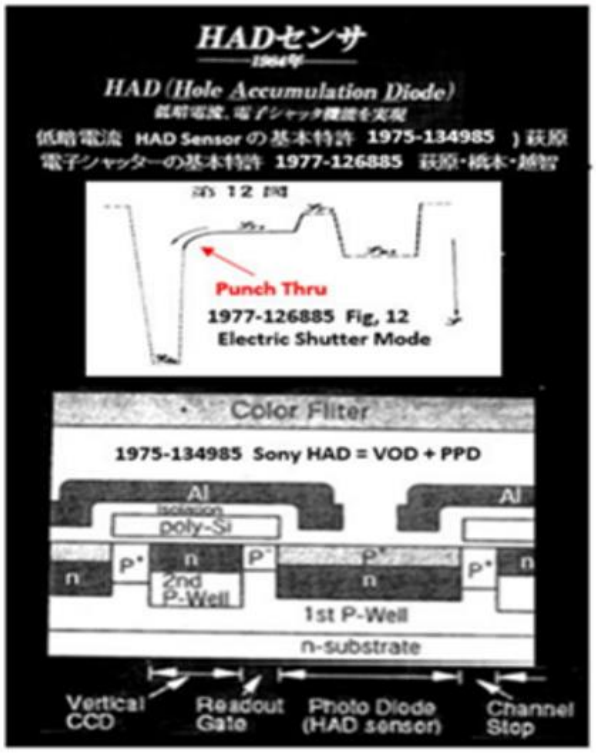


Image Lag Free Complete majority Carrier charge Extraction From the base(N) region is possible.

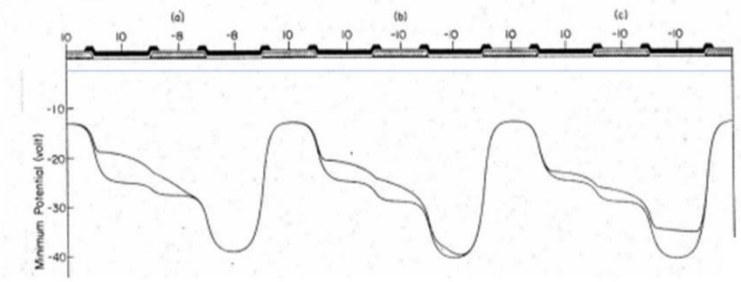
Hagiwara also proposed the thyristor type punch-thru clocking scheme, synchronized with the TV scanning system to achieve the electric shutter.



Electric Shutter Basic Patent Award
from Sony President Idei to Yoshiaki Hagiwara
for Japanese Patent 1977-126885 by Hagiwara

Caltech_1975_PhD_Thesis_Yoshiaki_Daimon_Hagihara.pdf

Exact Numerical Computer Simulation of Charge Transfer Action
in Buried Channel CCD presented in ISSCC1974 by Yoshiaki Daimon-Hagiwara

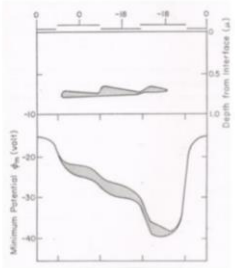


for details see the PhD Thesis by Yoshiaki Daimon-Hagiwara on June 1975 from Caltech.

Charge-Coupled Devices and Applications

Daimon
Lewis M. Terman

My PhD thesis paper
on buried channel CCD
at ISSCC1974, in Philadelphia, USA



Prof. T. C. McGill

Prof. C. A. Mead

Four Japanese Patent Applications on Pinned Photodiode with Electric Shutter Function and also With the in-Pixel Global Shutter MOS/CCD Buffer Memory Function for Modern CMOS Image Sensors.

Japanese Patent Application JPA1975-127646
Japanese Patent Application JPA1975-127647
Japanese Patent Application JPA1975-134985
Japanese Patent Application JPA1977-126885

Prof. James McCaldin and Hagiwara

Five Recently Published Papers by Hagiwara(AIPS)

ICECET2021_Paper75.pdf
ICECET2021_Paper61.pdf
IJSSM2021 e-Journal Paper on Pinned Photodiode.html
EDTM2020 Conference Paper_ID_3C4_by_Hagiwara(PDF)
P2019_3DIC2019_Paper_on_3D_Pinned_Photodiode_6_pages.pdf

The first Pinned Photodiode papers in 1977 and 1978 by Hagiwara at Sony

Hagiwara_SSDM1978_Paper_on_Pinned_Buried_Photodiode.pdf
P1977_Narrow_Cahnnel_Transfer_Gate_CCD_SSDM1977_Paper_by_Hagiwara.pdf"