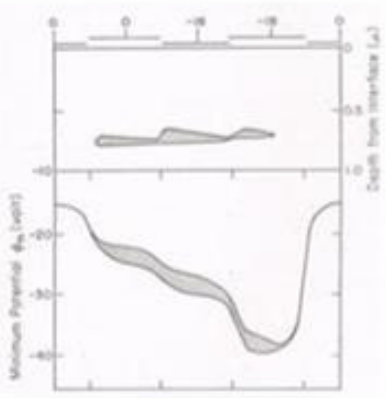
# Acknowledgment

Charge-Coupled Devices and Applications

Chairman

Lewis M. Terman

My PhD thesis paper
on buried channel CCD
at ISSCC1974 in Philadelphia, USA



Prof. T. C. McGill

Prof. C. A. Mead

My first publication was a PhD thesis paper published at the ISSCC1974 in Philadelphia in Feb 1974. CalTech/JPL NASA (IBM) computers were used to perform three dimensional ( x, y and t ) BCCD device simulations for polysilicon and aluminum overlapping gate buried channel CCD structure with the two dimensional Poisson 's equation and time domain continuity equation.

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Slide 34

The author expresses sincere gratitude to Prof. C.A. Mead and Prof. T.C. McGill, for advising my original 1971 work at Caltech on the Ga2O3 – Au Schottky Barrier interface study and characterization, and also for guiding my original 1974 PhD thesis work. on the Charge Transfer Analysis of Buried Channel CCD Image sensors, Thank you very much.

Yoshiaki Hagiwara March 16 , 2020

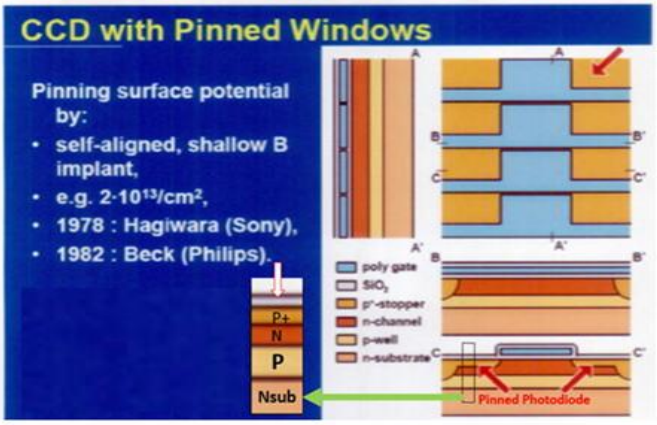
**Hagiwara reported the Pinned Windows and Pinning Surface Potential in 1978 based on his 1975 invention of the P+NPNsub junction type Pinned Photo diode.**

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 12, DECEMBER 2006

The Hole Role in Solid-State Imagers

Albert J. P. Theuwissen, *Fellow, IEEE*

Despite these advantages, notice that parts of the depleted n-type CCD channels are not covered by gate material. In this way, their electrostatic potential is not defined! Such a structure will suffer from serious charge transport issues during its operation, because charge can and will be trapped in local potential pockets. The effect can simply be solved by defining the potential in the open areas through an extension of the $p^+$-channel stopper. A simple self-aligned p-implant of $2 - 10^{13}/cm^2$ B-ions after the gate construction is sufficient to extend the channel stop area to the gate edge and, consequently, fix the potential in the open areas. The result after this self-aligned implant is shown in Fig. 4. The presence of enough holes plays a crucial role in fixing the potential for the regions normally "beyond control" of the gates. [Is this structure the mother of the PPD or buried diode or hole-accumulation device (HAD)?]




**Albert Theuwissen quoted Hagiwara 1978 paper and explained the importance of hole role in image sensors @ Workshop on CMOS Imaging, Duisburg May 16, 2006**

**Direct Quotation** The presence of enough holes plays a crucial role in fixing the potential for the regions normally "beyond control" of the gates. [Is this structure the mother of the PPD or buried diode or hole-accumulation device (HAD)?]

Quoted directly from IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL.53, No.12, DEC 2006

To search page

# 1975-80

# Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

**~ Discrete Semiconductor/Others ~**

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Photodiodes are used for photodetectors of image sensors. In 1987, Sony introduced a 2 / 3-inch, 380,000-pixel CCD image sensor (ICX022) using a new type of photodetector, now called a Pinned Photodiode (Sony named it HAD: Hole Accumulation Diode)[1].

The Pinned Photodiode is a photodiode in which the entire N layer is covered with a P layer. The part of the P layer on the light incident surface is heavily doped P+ (Fig-1). Kodak named this structure Pinned Photodiode in 1984 because the P + surface of the light incident surface was pinned to the substrate potential. This device has features such as high light sensitivity, wide dynamic range, image lag free, much smaller dark current due to reduced influence of GR center on the light receiving surface, and no white scars.

In 1975, Sony proposed using a PNP transistor as the photodetector[3]. By providing a P + layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated, greatly improving the light sensitivity. This P + layer was also a proposal to reduce the dark current and image lag which became the basis of the pinned photodiode.

In 1978, Sony presented a 93,000-pixel FT (Frame Transfer) -CCD image sensor compliant with the Analog TV Broadcasting Standard (SDTV) for the first time in the world[5], using the photodiode with the same structure as above. Sony succeeded in 1981 in trial production of a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor by further improvement of this technology[6].

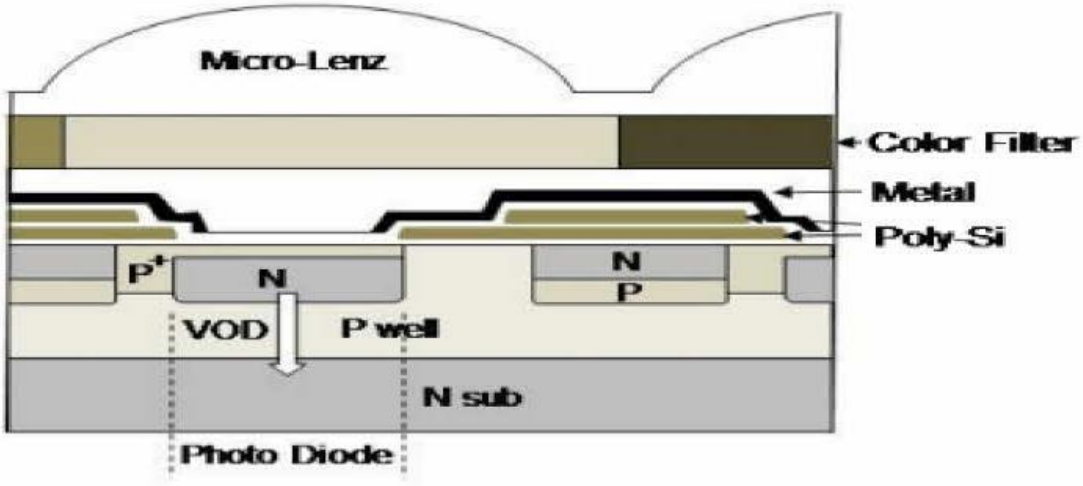



Fig-1 Recent Image Sensor with Pinned Photodiode

References:

【1】M. Hamasaki, T. Suzuki, Y. Kagawa, K. Ishikawa, K. Miyata and H. Kambe, "An IT-CCD imager with electronically variable shutter speed" , Technical Report of The Institute of Image Information and Television Engineers, vol. 12, no. 12, pp. 31-36, (1988)

【3】Y. Hagiwara, Japanese Patent JP1975—134985

【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

【6】I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara, "Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain"、Technical Report of The Institute of Image Information and Television Engineers、vol. 5, no. 29, pp.

# Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

Sony Corporation
Sony Semiconductor Solutions Corporation

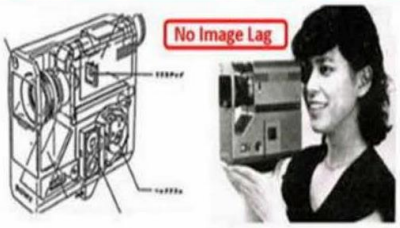
**https://www.sony.net/SonyInfo/News/notice/20200626/**

## Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

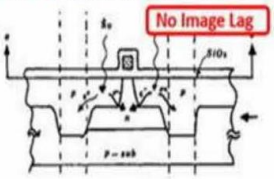
The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

**Sony original 570H x 498 V one-chip FT CCD Image Sensor with Pinned Photodiode, July 1980**




P+NP Junction Pinned Photodiode




On July 1980, Iwama Kazuo at Sony Tokyo Press Conference and Morita Akio at New York Press Conference announced the one chip CCD video camera with the 8 mm VTR in one box.

**See the Original 1978 Publication of the Pinned Photodiode Sensor**

Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates," Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Appllied Physics , vol. 18, supplement 18–1, pp. 335–340, 1979

**High quality picture of SONY CMOS Imager is also based on SONY HAD ( Pinned Photodiode).**

**These figures shows (1) Excellent Blue Light Sensitivity (2) Low Surface Dark Current and (3) NO Image Lag Features of the P+NP junction type Pinned Photodiode.**

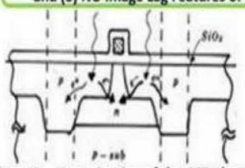


Figure 2 Cross Section of the CCD charge Transfer Region with the P+NP junction tvoe Pinned Photodiode (PPD)

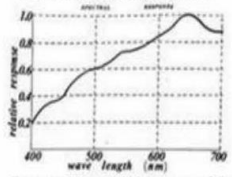



Figure 13 Spectral Response of the P+NP junction Pinned Photodiode (PPD) with the excellent blue light sensitivity

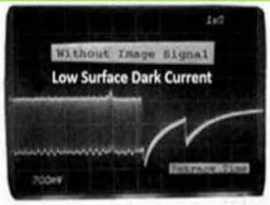




Figure 14 Comparison of CCD image sensor output signals with and without image signal.

# Pinned Photodiode and Sony Hole Accumulation Diode (HAD)

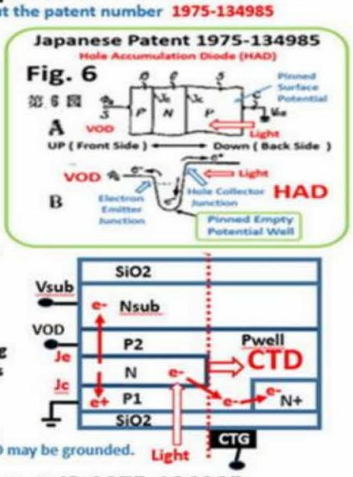
## PNPN junction Transistor type Pinned Photodiode

Visit https://www.j-platpat.inpit.go.jp/ and put the patent number 1975-134985

| | | | |
|---|---|---|---|
| File | 1975-134985 | Filed | 1975/11/10 |
| Public | 1975-058414 | Public | 1977/05/13 |
| | | Grant | 1983/10/19 |

**Patent Claim in English Translation**

(1) In the semiconductor substrate (Nsub), the first region( P1 ) of the first impurity type is formed, (2) on which, the second region ( N ) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N) is is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction ( Je ) is formed on the second region (N) of the light collecting part (N) . And (6) Collector junction ( Jc ) is formed by the second region (N) and the first region (P1), forming a transistor structure ( P2NP1 ) (7) Photo charge is stored in the Base region (N) according to the illuminated light intensity, and transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.




Yoshiaki Hagiwara, Japanese Patent JP 1975-134985

## Pinned Photodiode defined in JPA 1975-127647 by Hagiwara in 1975

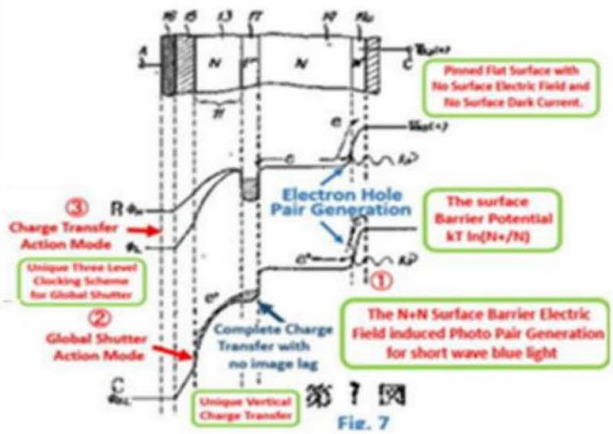



Fig. 7

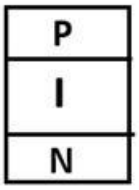
ELECTRICALENGINEERING

# Difference between Buried Photodiode and Pinned Photodiode

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

**PIN diode**




In 1975 the first PPD was invented by Hagiwara at Sony and used in ILT CCD PDs by Hamazaki at Sony in 1987.

PPD must have the P+ channel stops nearby to pin the surface P+ layer.

This is a commonly misunderstood misused set of terminologies.

First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

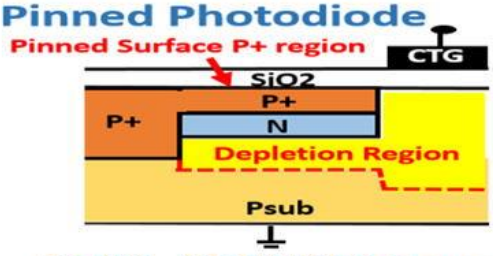
A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

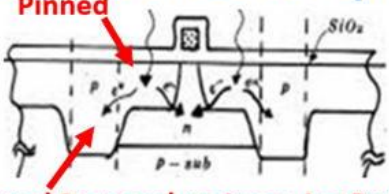
I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

## Difference of Buried Photodiode and Pinned Photodiode

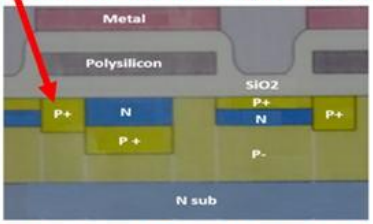
### Pinned Photodiode




SONY SSDM1978 Paper

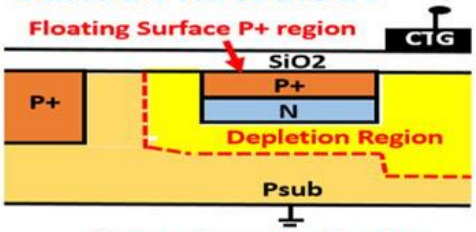



P+ Channel Stops and no Image Lag Problem



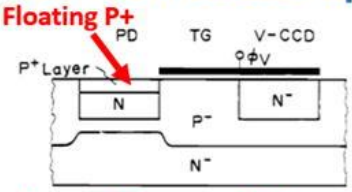

SONY 1987 HAD Sensor

### Buried Photodiode

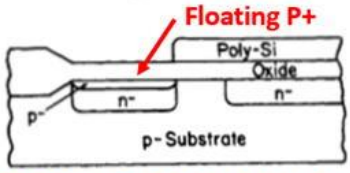



Serious Image Lag Problem

NEC IEDM1982 Paper




No P+ Channel Stops and Serious Image Lag




KODAK IEDM1984 Paper

Sony

Sony Image Sensors do not use the LOCOS process of serious oxidation-stress induced defects and the possible isolation of the surface P+ hole accumulation layer from the the channel stops under the LOCOS.

## Fossum insulted in his 2014 paper Sony and Hagiwara 1975 PPD invention.

**Indeed, Hagiwara invented PPD with VOD and the virtual charge transfer in 1975 !!**

IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY, VOL. 2, NO. 3, MAY 2014 33

**Sony HAD (PPD+VOD) does not use LOCOS !!!**

### A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, *Fellow, IEEE,* and Donald B. Hondongwa, *Student Member, IEEE*

False

**Many people now said this is a fake paper !**

*C. Other Contributions to the PPD Invention*

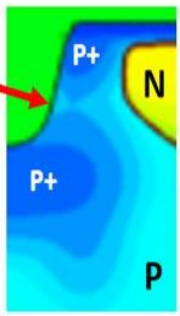
The PPD structure, while invented for low lag ILT CCD application, shares a strong resemblance to the Hynecek virtual-phase CCD structure, with the exception of the VOD. The two inventions were solving different problems with essentially the same device structure and operating principles.

In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top *p* layer was connected by metal to a bias used to control full-well capacity and the *n*-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called "Hole Accumulation Diode," or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the "narrow-gate" CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

The PPD, as it is most commonly used today, bears the strongest resemblance to the Teranishi et al. ILT CCD device. Thus, these days Teranishi is considered as the primary inventor of the modern PPD [29].

False

The surface P+ layer is NOT connected to the LOCOS P+ layer. The surface P+ layer may be floating and this photodiode may have serious image lag.




Serious Image Lag ?

NOT connected

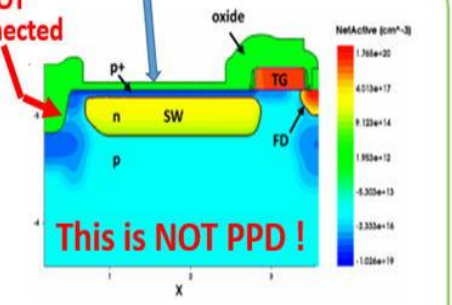


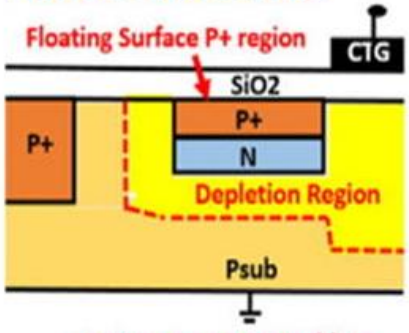

Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

## Hagiwara in 1975 invented PPD with VOD and the virtual charge transfer.

## Study the Japanese Patents 1975-127646, 1975-127647 and 1975-134985.

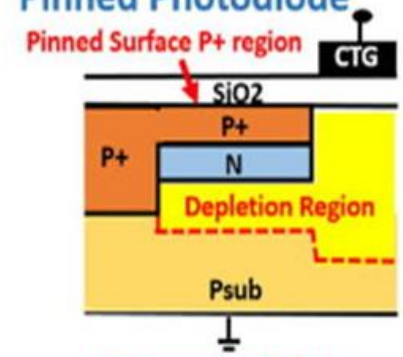
## Pinned Photodiode Must Have the Grounded P+ Channel Stops Nearby.

### Buried Photodiode




Serious Image Lag Problem

### Pinned Photodiode




No Image Lag Problem

The resistivity ρ of the P+ hole accumulation layer is given by

$$\rho = R * W * d / L$$

In the 2/3 inch optical lens system, we have the optical image size of 8.8 mm (H) x 6.6 mm (V) which was a common size in 1980s. Hence, we then have L = 6.6 mm = 6600 μm

The short wave blue light cannot penetrate more than d = 0.2 μm into the silicon crystal in depth. Hagiwara reported in SSDM1978 paper $Qd = 2 \times 10^{13} cm^{-2}$ which gives $Nd = Qd/d = 1 \times 10^{18} cm^{-3}$

For $Nd = 1 \times 10^{18} cm^{-3}$, we have $\rho = 0.04$ ohm cm = 400 ohm μm

$$RC = \{ L\rho / (W*d) \} \{ \varepsilon W*L / Xo \} = \varepsilon \rho L^2 / (d Xo)$$

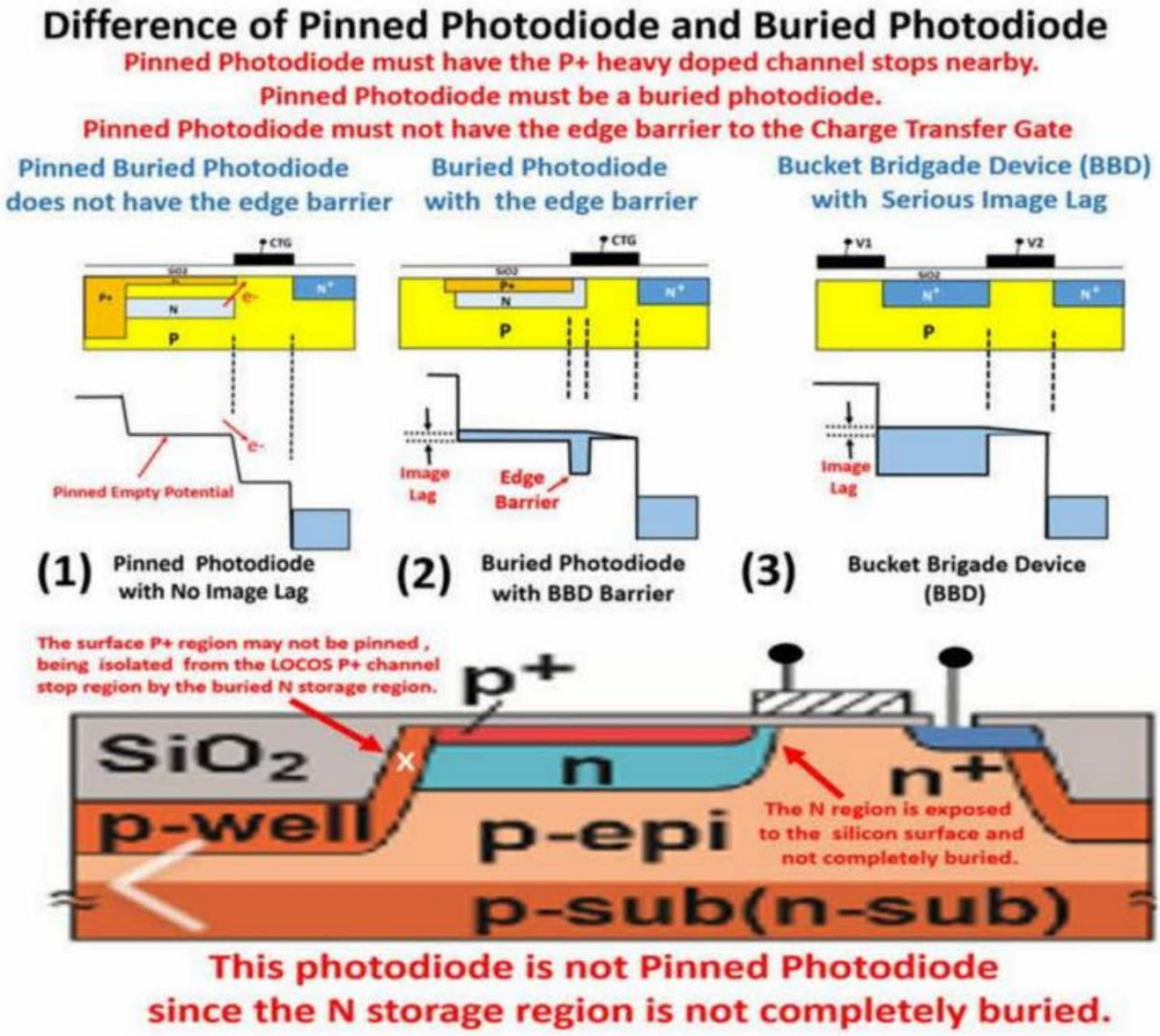
We have $\varepsilon = 216$ e/volt μm for silicon oxide and $e = 1.6 \times 10^{-19}$ Coulomb

$$RC = (216)(1.6 \times 10^{-19})(400)(6600)(6600) / (0.2)/(0.1) \text{ sec}$$

RC = 30.1 μsec while one frame is 1/60 sec = 16.7 msec and the Vertical CCD register clock period is 16.7/500 = 33.4 μsec

Hence RC delay time may not be ignored and surface P+ may be floating ?

Photodiode with Serious Image Lag is NOT a Pinned Photodiode by definition ???




In the SSDM1978 paper, Yoshiaki Hagiwara at SONY reported the P+NP double junction dynamic photo transistor used in a Frame Transfer CCD image sensor. Hagiwara is the true inventor and also the pioneering developer of the P+NP double junction dynamic photo transistor, which was called differently by NEC1982, KODAK1984 and SONY1987. The problem is that, NEC, KODAK and even Sony1987 HAD product announcement did not quote Hagiwara's original 1975 inventions and Hagiwara SSDM1987 important works, which reported the P+NP double junction dynamic photo transistor, originally invented by Hagiwara in 1975. Evidence is shown in Hagiwara's Japanese Patent Applications, JPA1975-127646, 1975-127646 and 1975-1234985. Examine these important evidence. Then, you will see that Yoshiaki Hagiwara, at Sony in 1975, is the true inventor of the Buried Photodiode reported in the NEC IEDM 1982 paper, the Pinned Photodiode reported in the KODAK IEDM1984 paper, and the Sony 1987 Hole Accumulation Diode (HAD). They are all the same thing that Hagiwara invented in 1975. Before Hagiwara 1975 inventions, all image sensors were based on the floating N+P single junction type photodiode with the serious image lag or the CCD/MOS type photo capacitor with the serious surface dark current and the very poor blue light sensitivity.