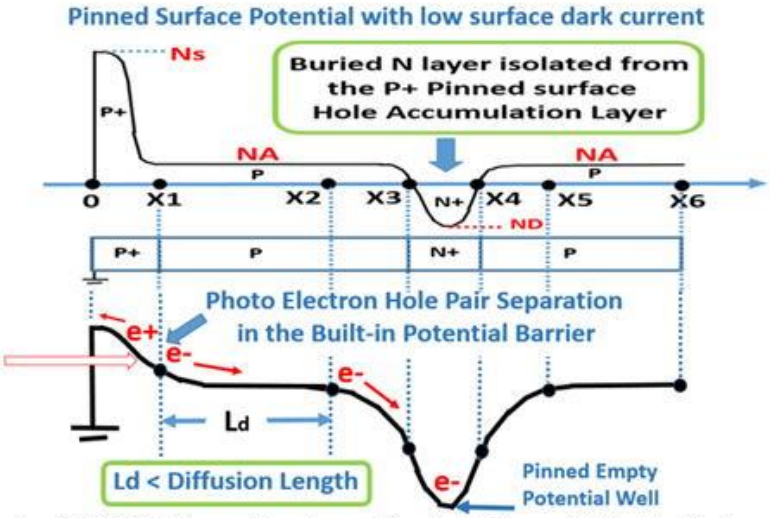

Fig. 5: P+PN+P junction type Buried Pinned Photodiode defined in Hagiwara Japanese 1975-127647 patent.

Slide 22

The Figure 5 shows our proposed P+PN+P junction type Buried Depletion Pinned Photodiode. Normally the photo electron and hole pair generation and separation is performed in the electric field inside the depletion region of the PN junction or under the CCD/MOS capacitor.

But the photo electron and hole pair generation and separation of
this P+PN+P junction Pinned Photodiode is different and quite unique.

The surface P+P impurity doping slope induces the built-in barrier potential
and results in the built-in barrier electric field, enhancing the photo electron pair separation at the very near surface region of the silicon crystal to give the excellent blue light sensitivity.

This photo electron hole separation mechanism is unique, quite different from the usual photo electron hole pair separations in the normal PN junction depletion regions.

Simulation and the electrostatic analysis is based on the fact that the maximum depth for the blue light penetration into the silicon crystal is only 0. 2 micro meter in depth which is very close to the silicon crystal surface where we cannot have a shallow PN junction depletion region with the strong surface electric field causing the undesired surface dark current.

The life time of the photo generated minority carrier can be measured using the photoconduction effect and the diffusion length can be determined, which is needed for electrons to survive in the majority carrier hole-rich P substrate area. Most of the photo electrons are expected to reach the buried N charge collecting region.