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hagiwara-yoshiaki@aiplab.com

Slide 01 Thank you for introduction.

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Simulation and Device Characterization of the P+PN+P Junction Type Pinned Photodiode and Schottky Barrier Photodiode

Yoshiaki Hagiwara
Artificial Intelligent Partner Laboratory
Atsugi-city, 243-0201 Japan
hagiwara-yoshiaki@aiplab.com; +81-80-2062-5657

01

Outline

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- Super Light Sensitivity Feature
- Low Surface Dark Current Feature
- No Image Lag Feature
- Schottky Barrier on Gallium Oxide
- Conclusions

02

Slide 02

This is the outline of my talk.

Image Sensors in general have the three most important features.
They are , First, Super Light Sensitivity Feature,
Secondly, Low Surface Dark Current Feature
and Thirdly No Image Lag Feature.

But we must not forget the most important basic feature of the common PN junction photodiode, which is the Low Leakage Current Feature.

The PN junction leakage is dependent on the minority carrier density
of the semiconductor material itself.

Related various historical photodiode structures will be reviewed,
including the gold metal and Ga2O3 type metal semiconductor Schottky Barrier photo sensor in search for the low leakage and dark current device.

Outline

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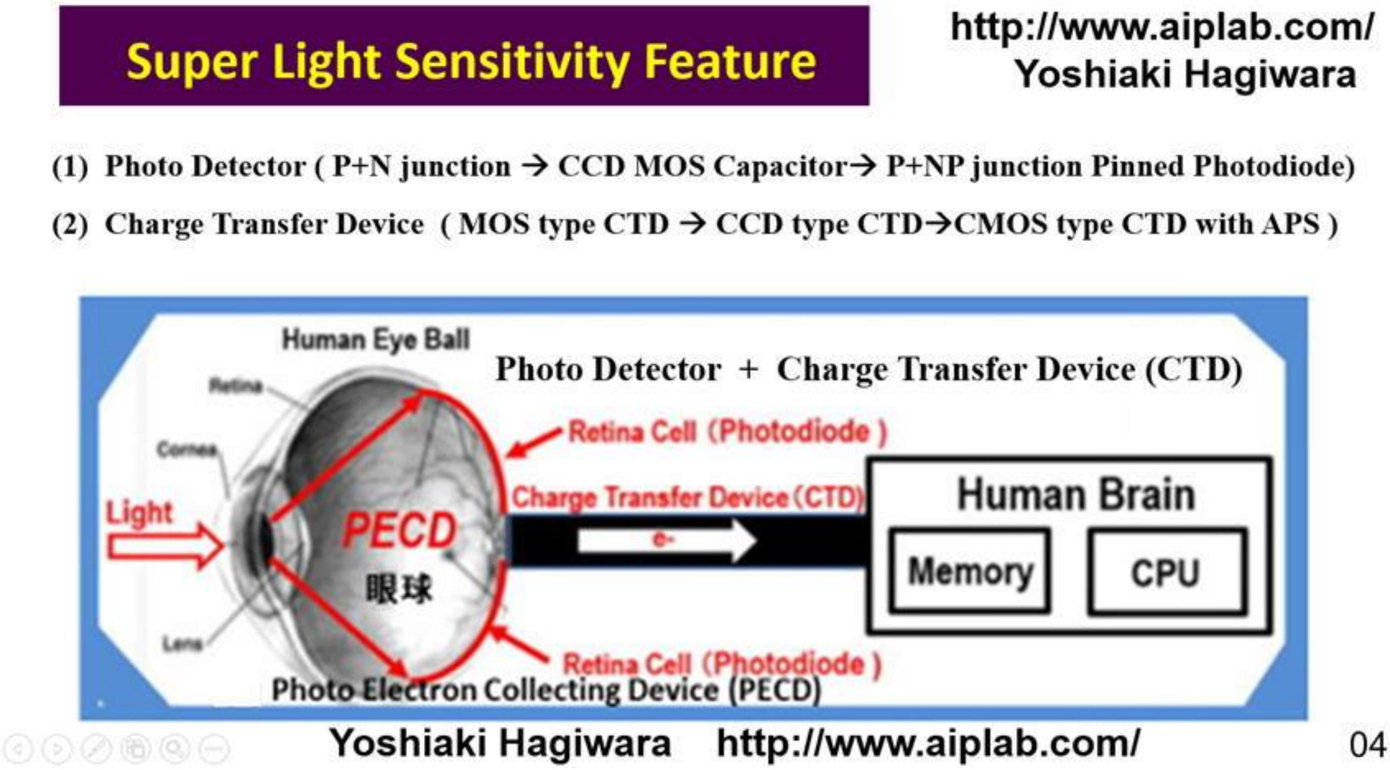
- **Super Light Sensitivity Feature**
- Low Surface Dark Current Feature
- No Image Lag Feature
- Schottky Barrier on Gallium Oxide
- Conclusions

03

Slide 03

We all know that
the super light sensitivity is
the most important feature of the image sensors.

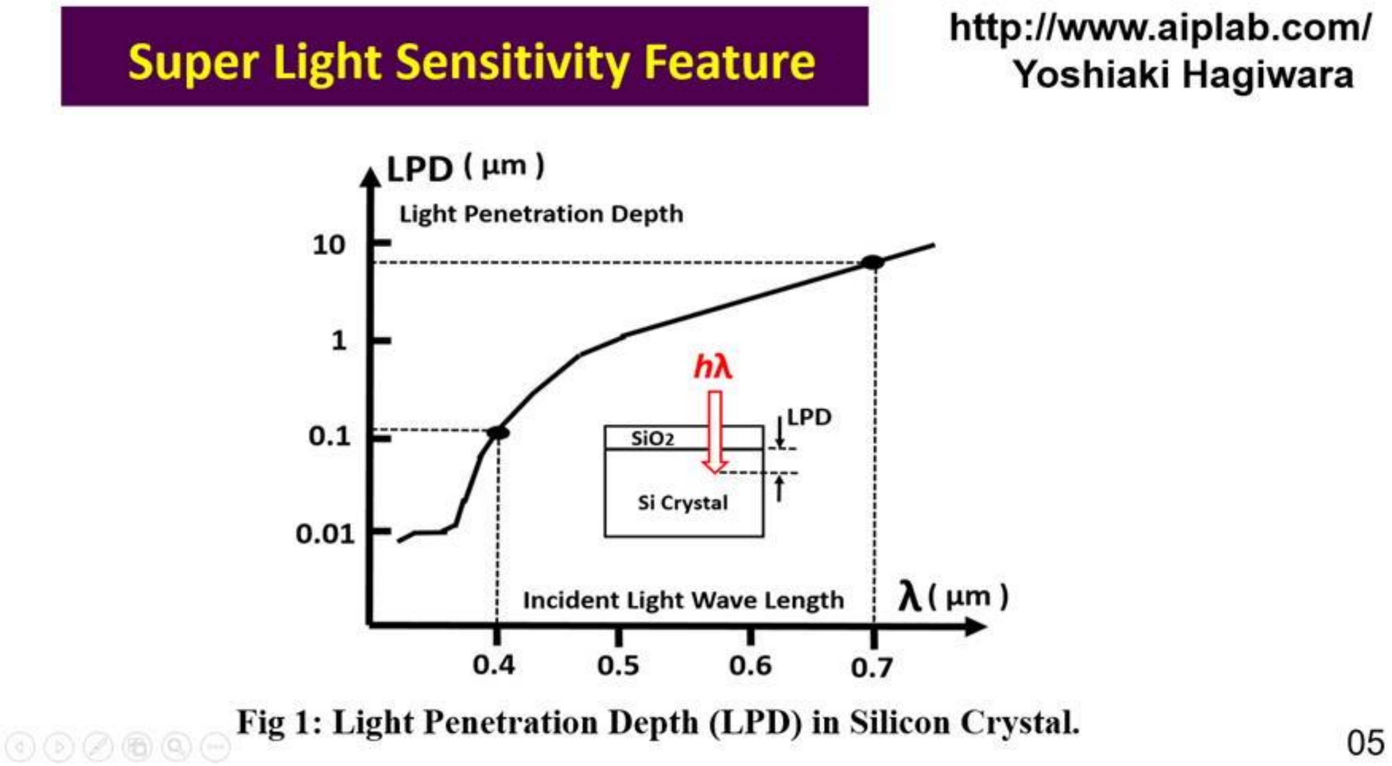


Slide 04

An image sensor in general
is composed of the super light sensitive photo detector
and the charge transfer device (CTD).

The CTD transports the signal charge to the outside processing units.
CCD type charge transfer devices have a very low charge transfer noise
and contributed very much to increase the S/N ratio of image sensors,
but now replaced and disappeared
from the image sensor markets
by more powerful CMOS type charge transfer devices
with active in pixel amplifier circuits.

However the super light sensitive photodetector,
which is now called as Pinned Photodiode
or Hole Accumulation Diode (HAD in short) remains
the same since its invention in 1975 by Hagiwara at Sony.



Slide 05

The figure 1 shows Light Penetration Depth (LPD) in Silicon Crystal.

As you can see,

the short wave blue light cannot penetrate
more than 0.1 micro meter into the silicon crystal.

To achieve the super light sensitive image sensor
we must convert the short wave light energy
into the electrical energy.

Super Light Sensitivity Feature

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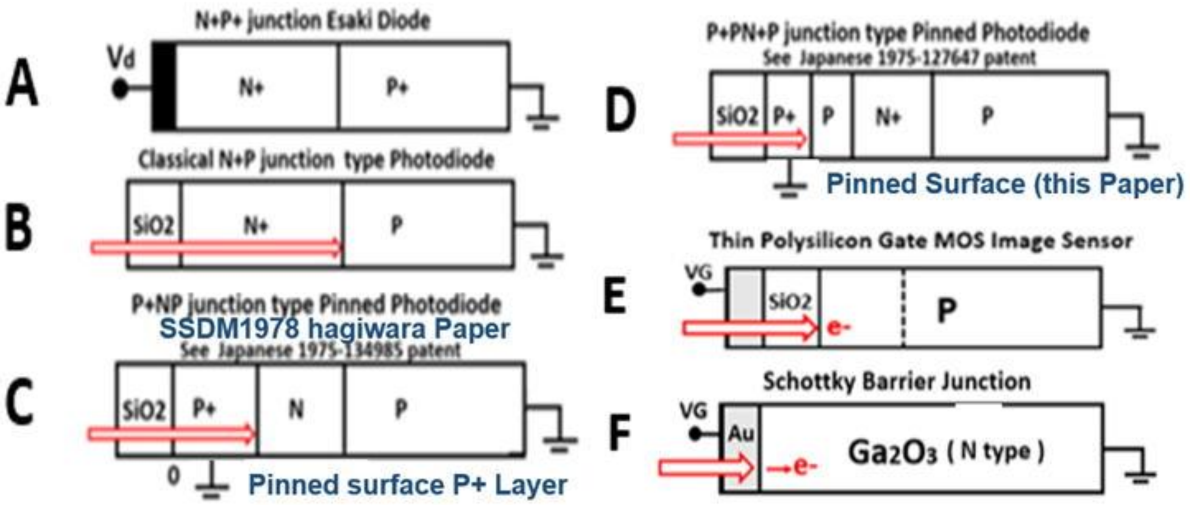

Fig 2: various types of photo sensor structures.

06

Slide 06

The figure 2 shows various types of photo sensor structures.

The type A device, which is the N+P+ junction Esaki diode is not a good photodiode
because it has a very narrow depletion width
and a very large electric field at the P+N+ junction inside the depletion region
causing the large leakage current problems in reverse operation mode.

The type B device of the N+P junction type classical photodiode, which is
widely used in classical MOS image sensors and early interline CCD image sensors
is known to have the serious image lag problems.

The type E device which is a MOS capacitor type photo sensor
has CCD like complete charge transfer operation mode with no image lag problems.
However, it has the metal electrode which reflects light like a mirror
and also absorbs the short wave length blue light, converting the illuminated light energy into heat.

Moreover the MOS capacitor has inherently the strong surface electric field
that creates the serious surface dark current.

The type D photodiode, which is, the P+PN+P junction Pinned Photodiode
can have the excellent blue light sensitivity near the silicon surface of 0. 2 micro meter in depth,
which is the main topics of this paper..

Super Light Sensitivity Feature

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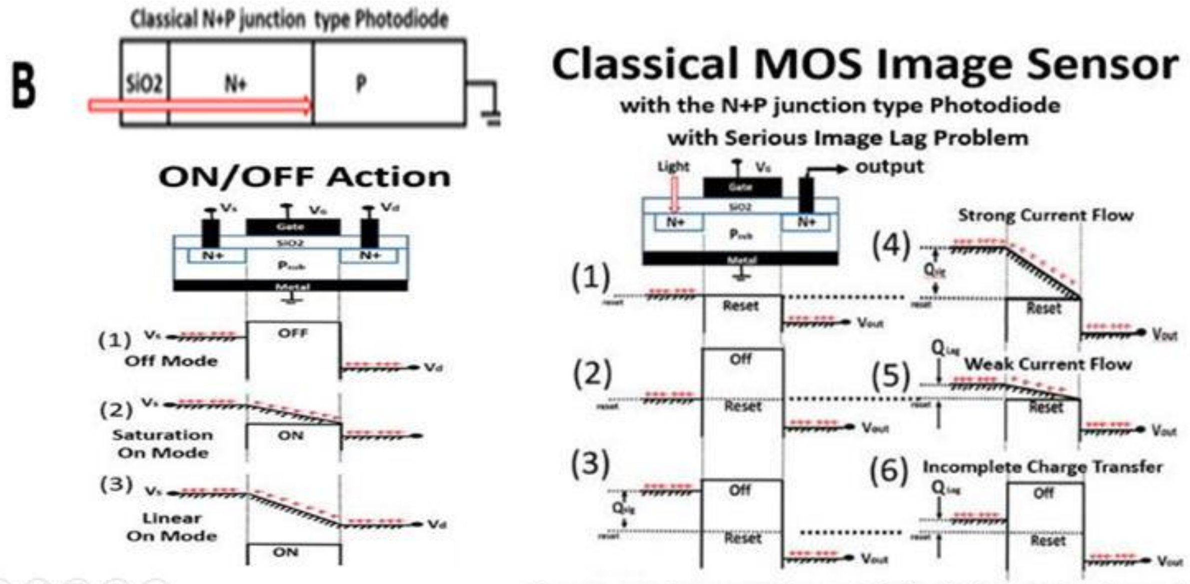


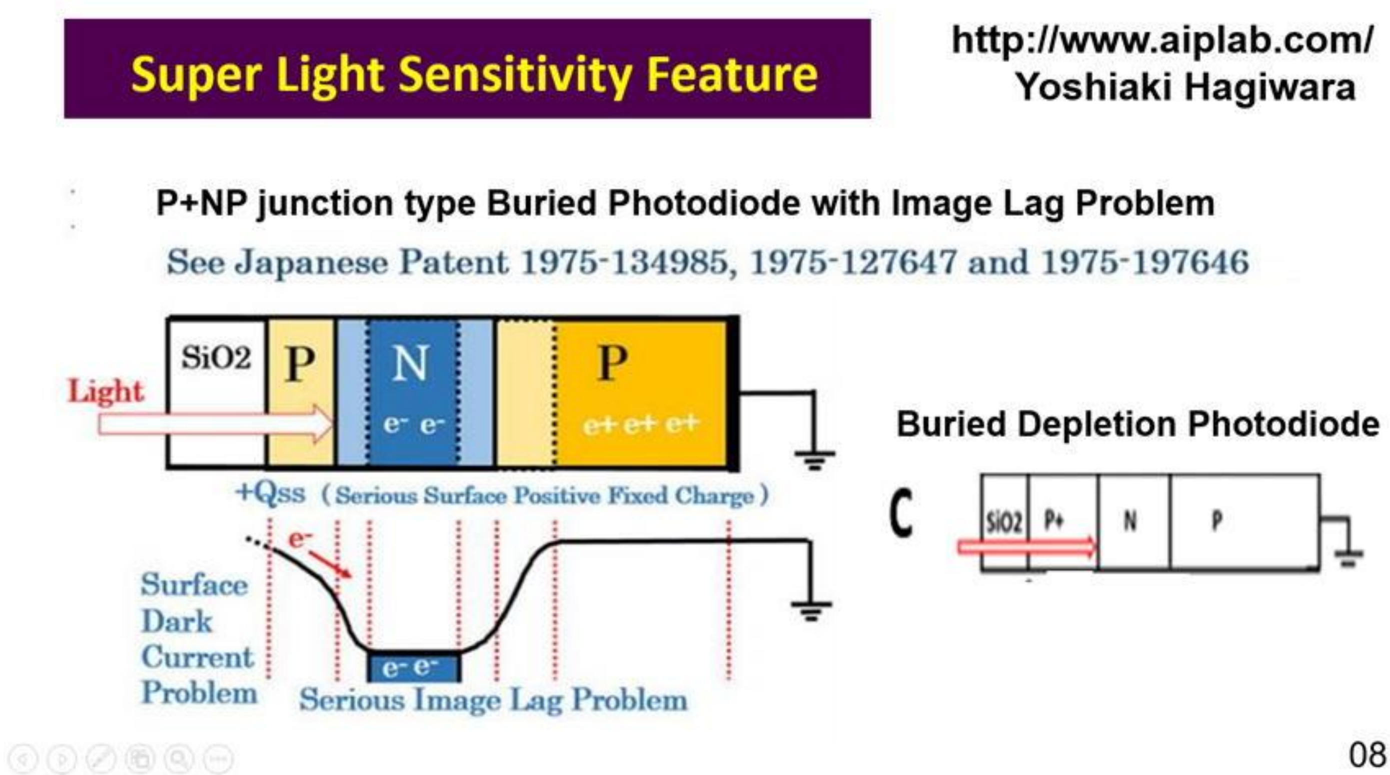
07

Slide 07

The image lag problem of the type B device,
which is, the N+P junction photodiode is
inherently caused by the floating potential level of
the N+ diffusion photo electron storage region.

The floating N+ diffusion storage region is
set nearly equal to the channel potential level
under the adjacent charge transfer gate,
by the gate oxide capacitance coupling.

The channel potential level under the charge transfer gate is
in the weak inversion state of high resistivity
for the short reset time causing the incomplete charge transfer.



Slide 08

The type C photodiode

which is the PNP junction type Buried Photodiode

may not be completely depleted of

the photo electrons in the N region,

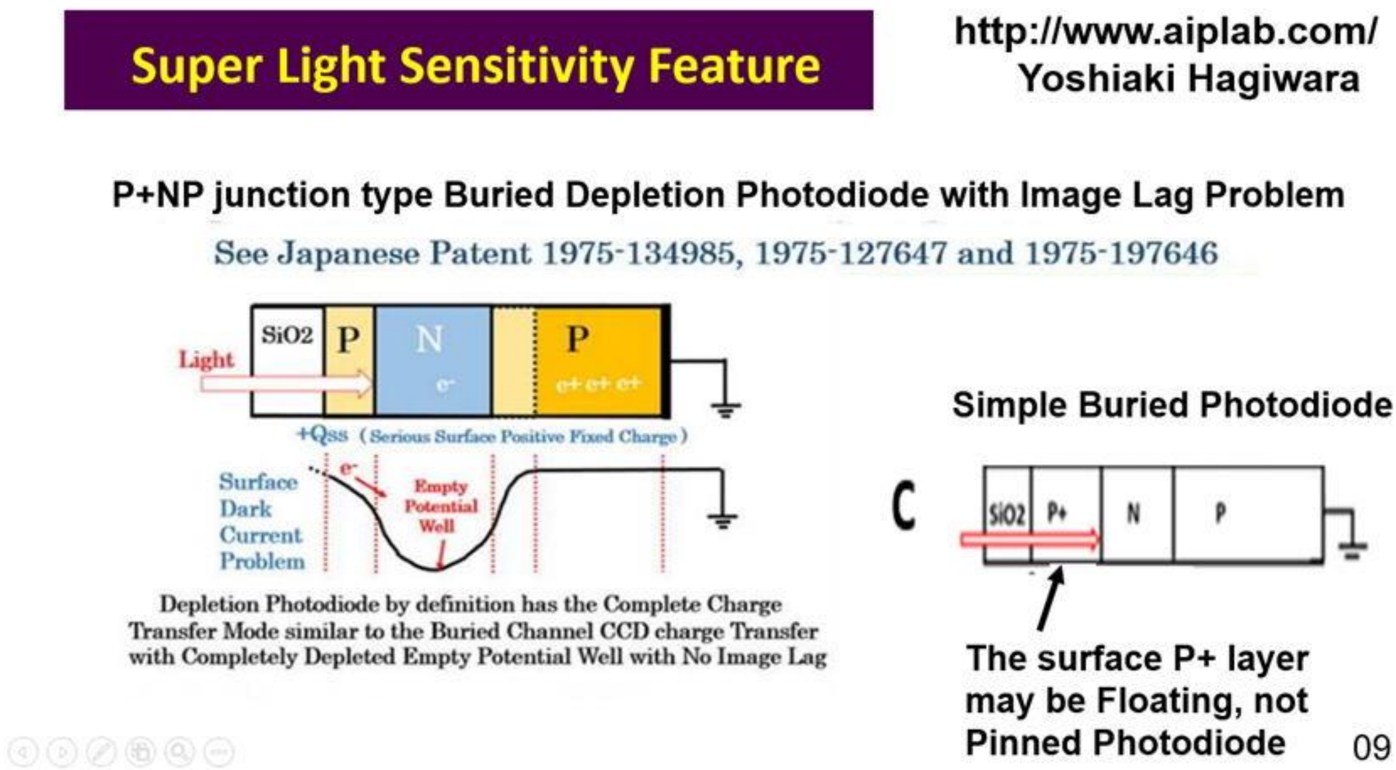
causing the image lag problem,

unless the surface p region is

pinned or fixed at a constant potential value

by the adjacent channel stops

or the adjacent metal external contact.



Slide 09

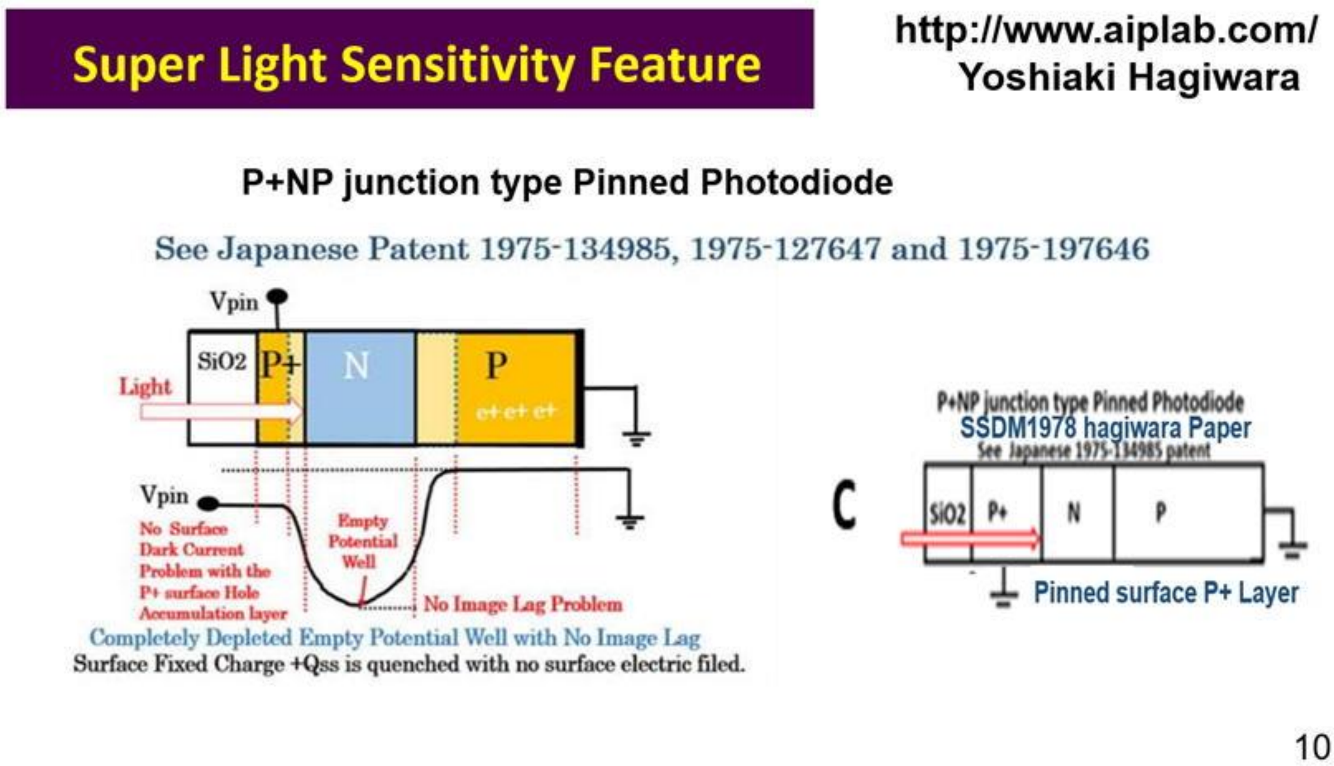
The Buried Depletion Photodiode shown in this figure,

also with the floating surface P+ layer with the surface electric field,

causes the same image lag problems with the similar reason

why the classical N+P junction type photodiode

inherently had the image lag problem.



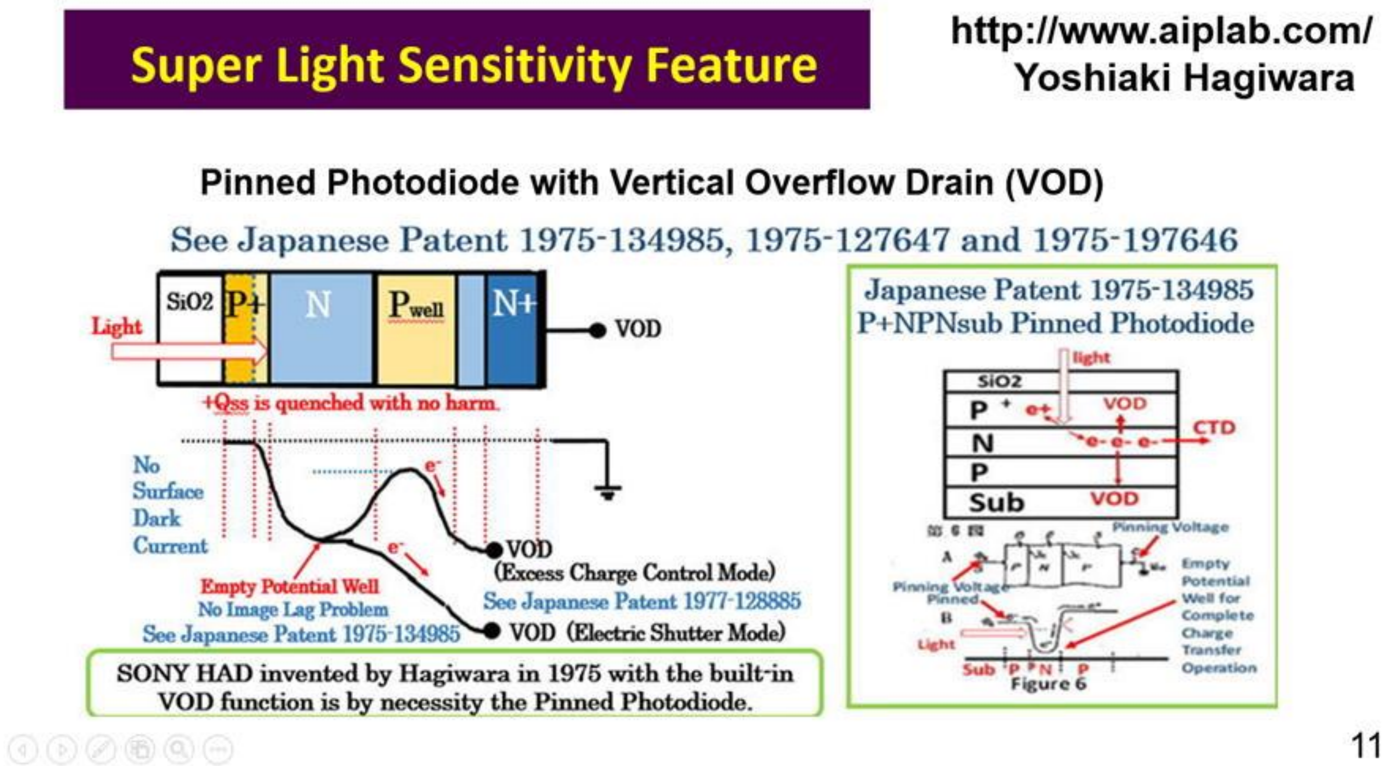
Slide 10

This slide shows the P+NP junction type Pinned Photodiode

with no image lag, with low surface dark current and

with the excellent short wave blue light sensitivity,

as originally proposed in Hagiwara 1975 inventions.



Slide11

This slide shows the conventional P+NPNjunction type,

The triple junction type dynamic photo thyristor type Pinned Photodiode

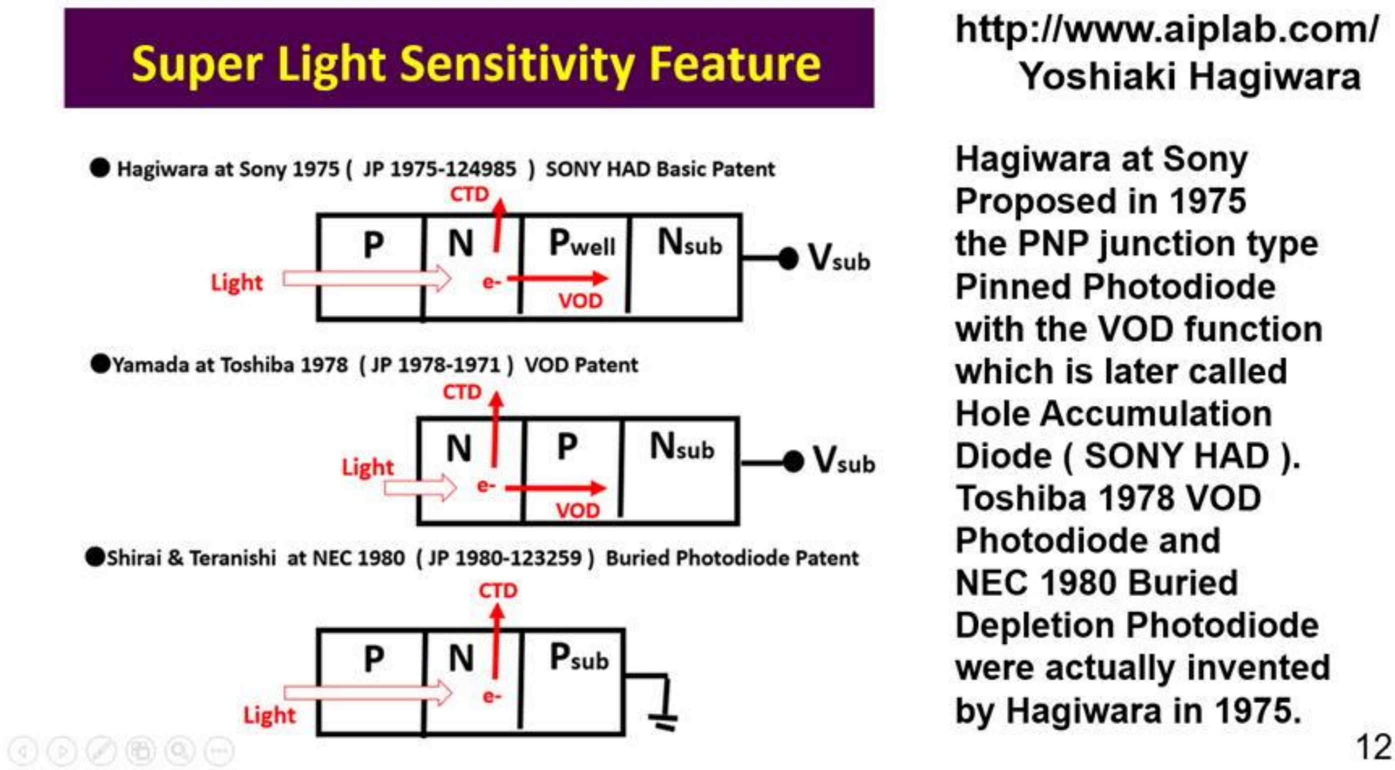
with the vertical overflow drain VOD function,

which is also called as Sony Hole Accumulation Diode,

which is also Hagiwara 1975 invention.

See also the Japanese Patent Application JPA1977-128885.

(Now finally disclosed now in the English Speaking Community. Sorry too late..)



Slide 12

Hagiwara at Sony Proposed in 1975

the PNPN triple junction type Pinned Photodiode

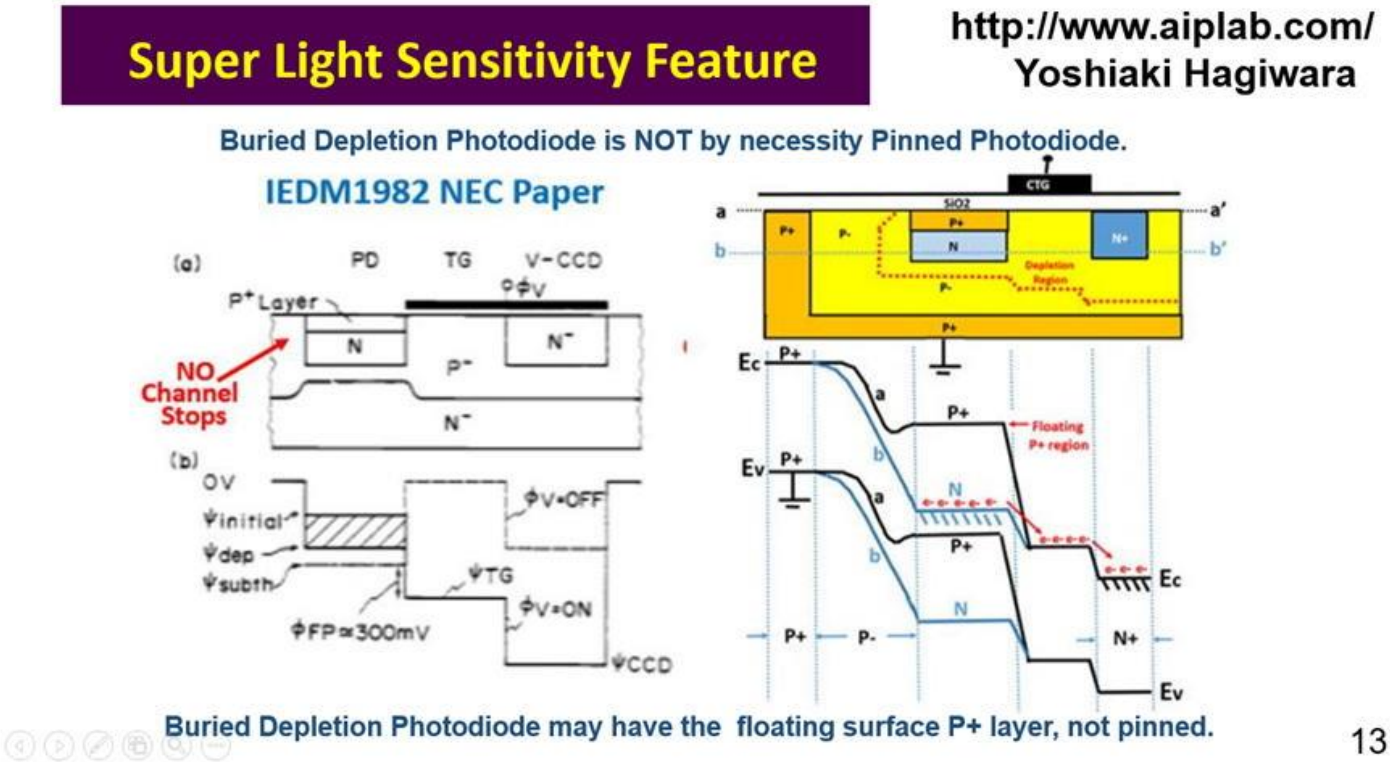
with the vertical overflow drain (VOD) function

which is later called Hole Accumulation Diode (SONY HAD).

In Hagiwara in his 1975 three patent applications, Hagiwara described the four basic and important features of the triple junction type Pinned Photodiode.

They are (1) very excellent short wave blue light sensitivity (2) in-pixel vertical overflow drain function (3) the completely mechanical-part-free electrical shutter function because of the no image lag feature of the empty potential well of the complete charge transfer operation (4) the pinned P+ surface hole accumulation layer with no surface dark current noise and (5) the Global Shutter Function Capability with the Buffer MOS capacitor memory.

Toshiba proposed the 1978 VOD Photodiode and NEC proposed 1980 Buried Depletion Photodiode. But they were proposed after Hagiwara 1975 inventions.



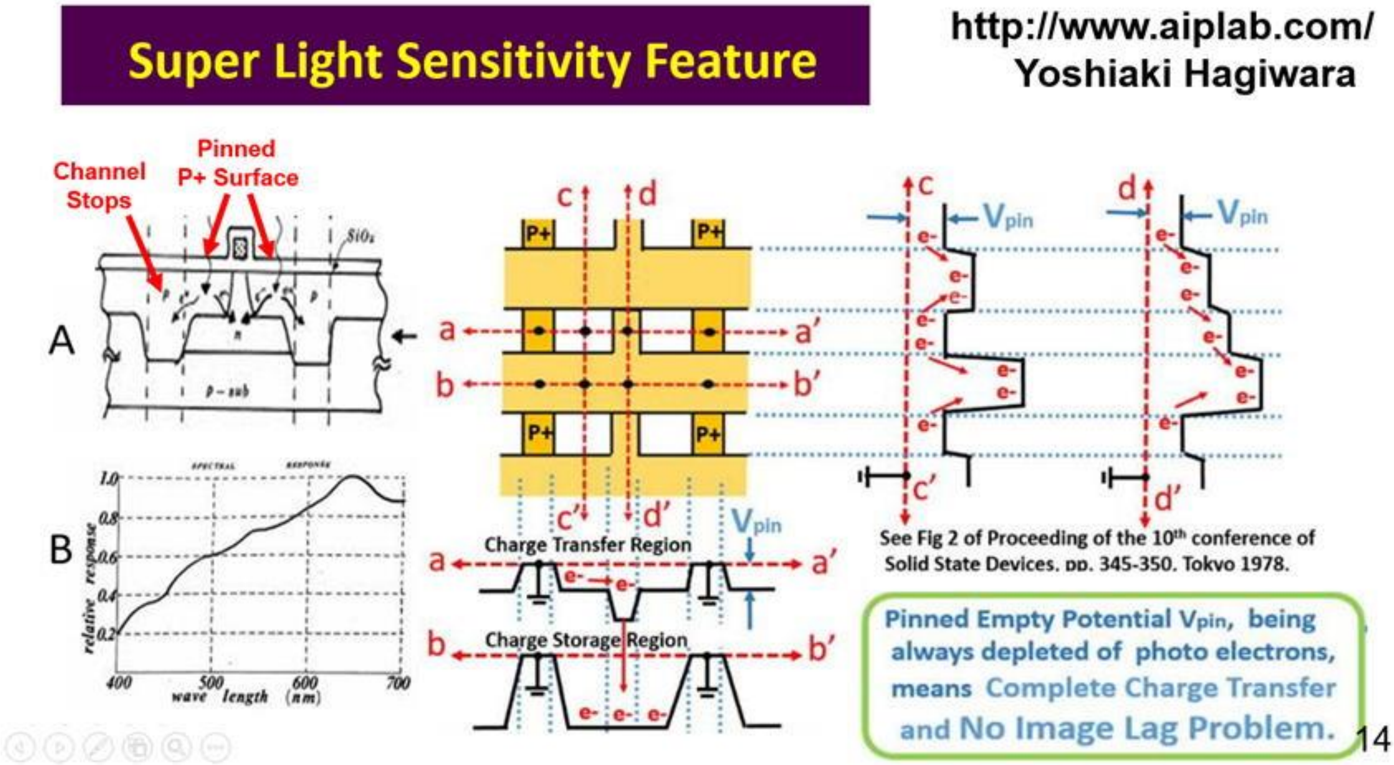
Slide 13

This slide shows that the buried depletion photodiode is not by necessity a pinned photodiode.

As you can see the surface P+ layer may not be pinned unless the surface P+ layer is directly connected to the adjacent P+ channel stops.

Otherwise, the surface potential can be floating, causing the serious image lag problem.

The surface P+ layer must be directly connected to the adjacent P+ channel stops.



Slide 14

This slide shows that the buried depletion pinned photodiode,

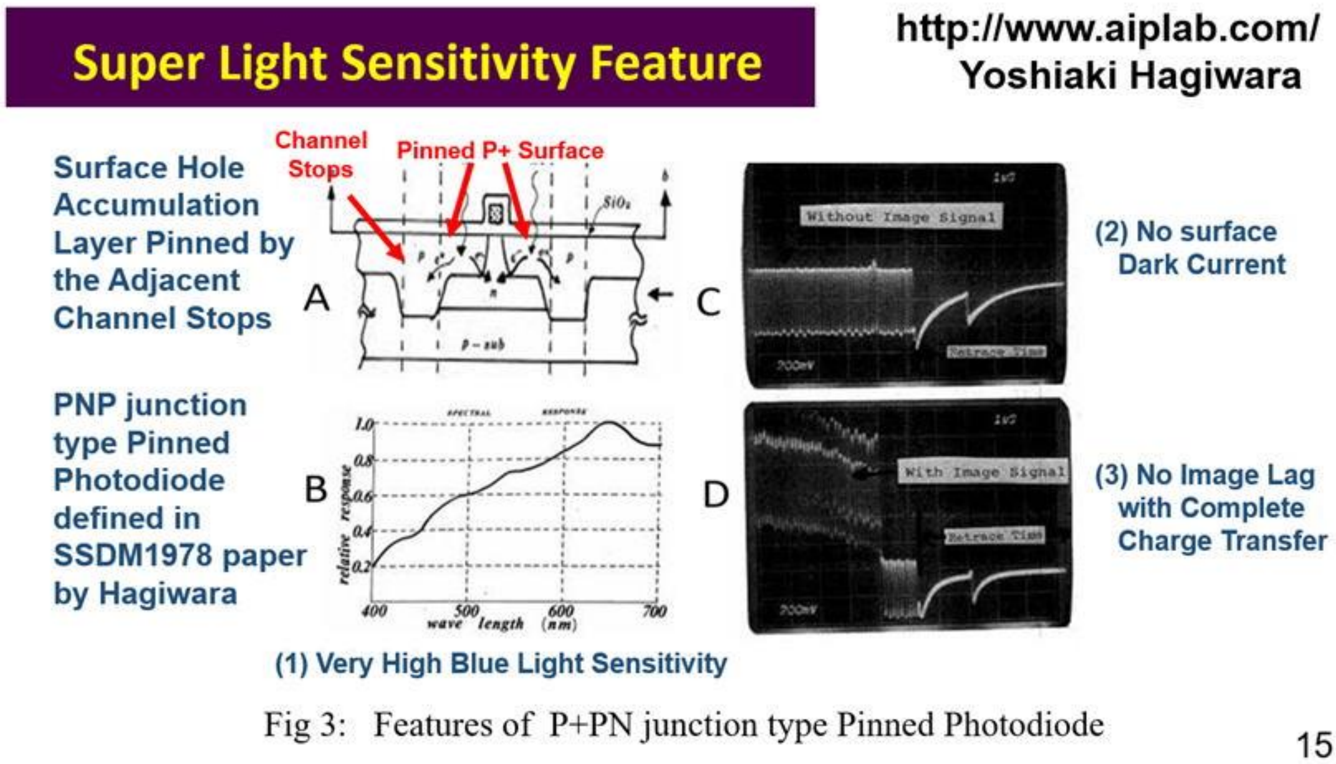
used in the 1978 Frame Transfer CCD image sensor

reported by Hagiwara in 1978　in his SSDM1978 paper.

The surface P+ potential is pinned to the ground potential

and also the empty potential well under the pinned surface P+ layer

is also pinned with no image lag problem.



Slide 15

The figure 3 shows important features of

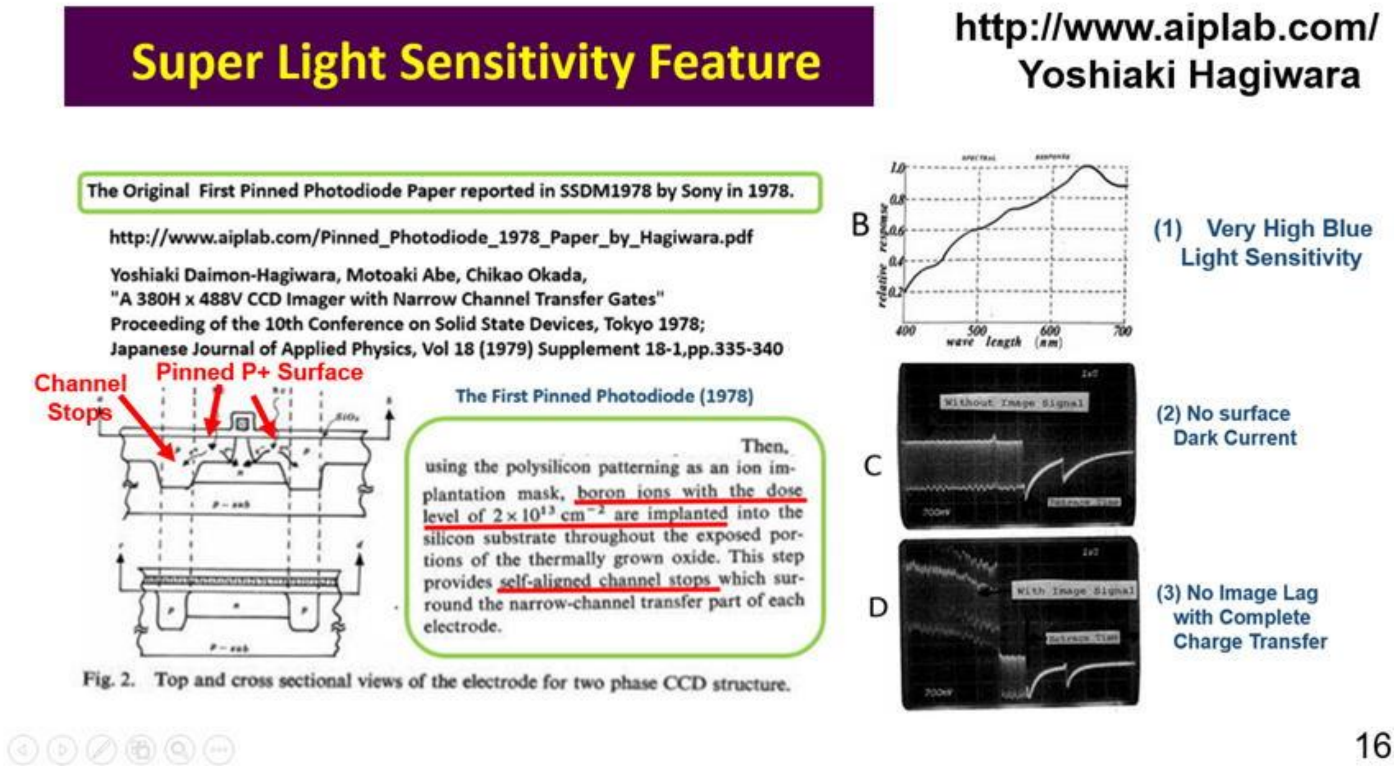
the PNP junction type Pinned Photodiode

developed by Hagiwara in 1978 .

The surface P layer must be exposed to the silicon oxide,

and must be pinned always to the substrate potential

by the adjacent channel stops.



Slide 16

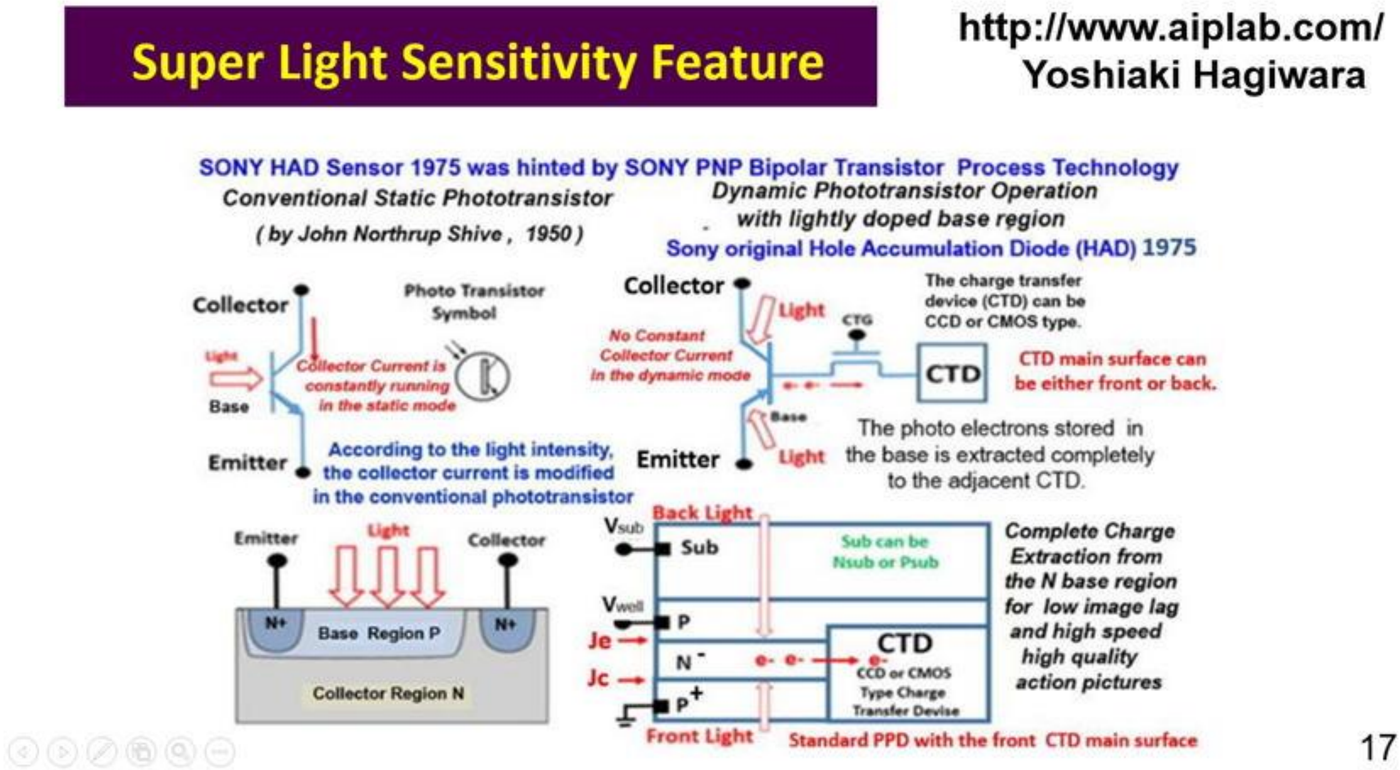
The surface P layer was formed by heavily doped ion implantation

of 2 times 10 to the 13 th power boron ions per cm square,

so that this surface P layer would be pinned always and

never be depleted of

the surface majority carrier hole accumulation layer.

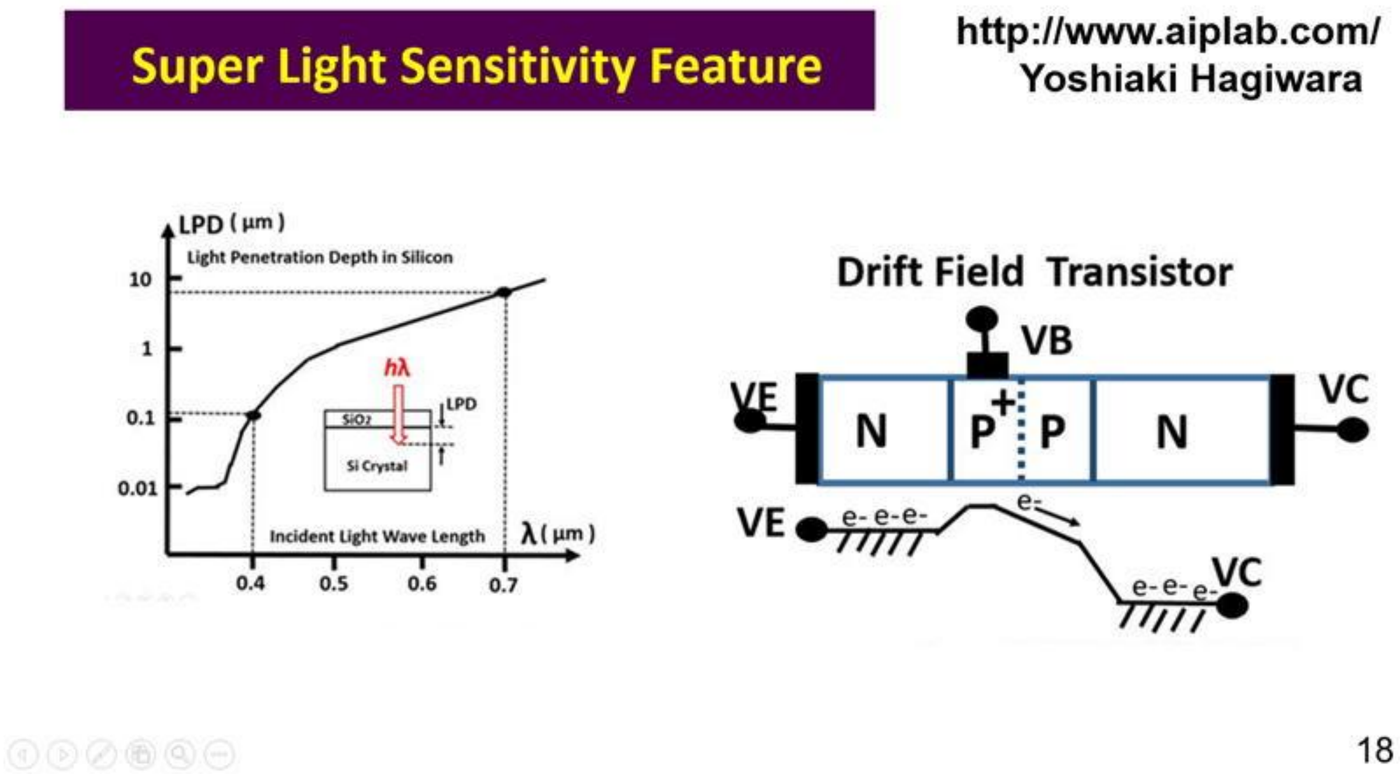


Slide 17

The static operation of the double junction type, the PNP photodiode, was invented by Shive in 1950 which is a static PNP phototransistor.

Hagiwara proposed in 1975 a dynamic PNP phototransistor, which is the origin of Pinned photodiode and which is also called as Hole Accumulation Diode (HAD).

It is well known that this heavily doped surface ion implantation creates the typical Gaussian P+P doping profile with the peak dose density at the surface and gradually deceasing to the substrate uniform impurity doping level.



Slide 18

The N+NP+PNN+ junction type Drift Field Transistor is

also known to have the P+P doping slope in the base region

which generates the drift electric field,

which helps the base-injected minority carriers

move out quickly from the base region,

enhances the high frequency characteristics

of bipolar transistors.

Hagiwara in 1975 proposed this physical effect

to the P+P pinned surface hole accumulation layer

to enhance the photo electron and hole pair separations

to achieve the excellent short wave blue light sensitivity.

Super Light Sensitivity Feature

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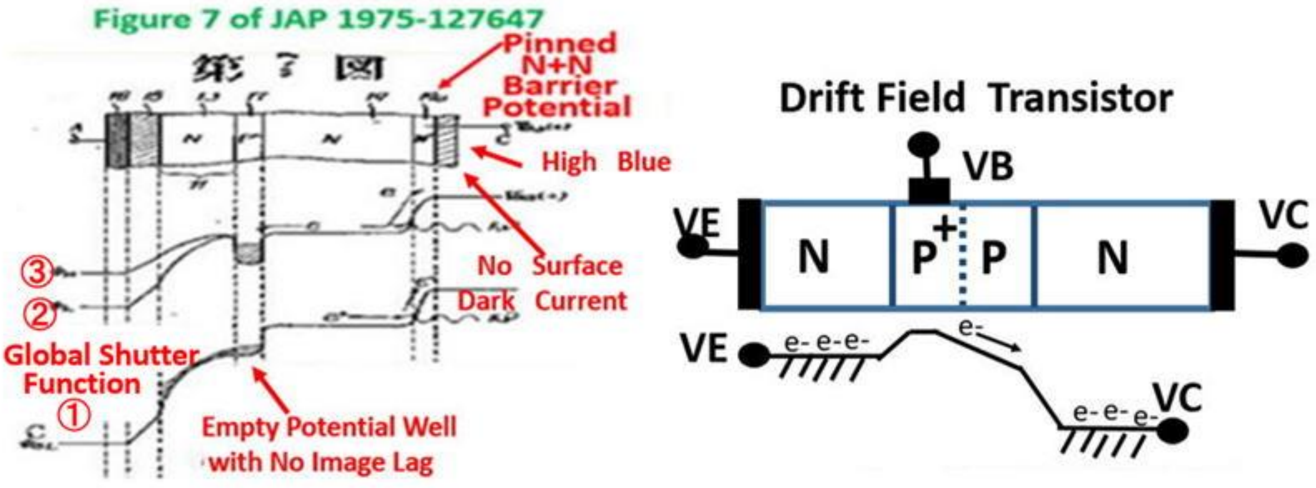

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Slide 19

Hagiwara proposed the N+NP+N junction type Pinned Photodiode in 1975.

The surface N+N doping slope profile is similar to the minority carrier electrons injected from the emitter terminal in the high frequency N+NP+PNN+ bipolar transistor, and drifting quickly , in Hagiwara 1975 invention, into the majority carrier hole-rich buried charge collecting and storage P+ region
the N+NP+N junction type Pinned Photodiode
which was proposed by Hagiwara in 1975.

If the base region width is narrow enough, one or two electrons may recombine with the holes in the base, but the most of the electrons can reach
the collector terminal of the strongly reverse-biased depletion region.

The buried N type region of Pinned Photodiode acts
as if the collector region of the NPN bipolar transistor does.

This photo electron generation separation physical mechanism
is unique and quite different from the ordinary electron hole pair separation
in the normal PN junction depletion region

The same surface P+P or N+N doping slope was utilized in the original 1975 pinned photodiode to realize the excellent short wave blue light sensitivity.

Super Light Sensitivity Feature

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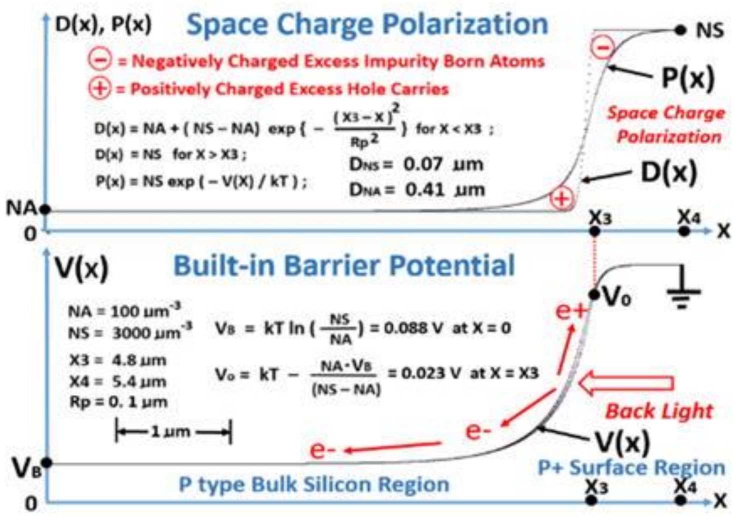

Fig. 4: Exact numerical calculations of Gaussian P+P doping profile D(x), the hole carrier density P(x) and the built-in barrier potential V(x).

Slide 20

The figure 4 shows the Exact numerical calculations of
Gaussian P+P doping profile D(x),
the hole carrier density P(x) and
the built-in barrier potential V(x).

The typical Gaussian P+P doping profile
with the peak dose density at the surface
and gradually deceasing to
the uniformly doped substrate impurity density
is analyzed by exact numerical calculation.

The difference of the hole carrier density P(x)
and the Gaussian P+P doping profile D(x)
creates the space charge polarization,
which in return creates the surface barrier electric field,
which enhances the electron hole separation at the surface
to achieve the very high quantum efficiency
at the short wave blue light spectrum.

Outline

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- Super Light Sensitivity Feature
- **Low Surface Dark Current Feature**
- No Image Lag Feature
- Schottky Barrier on Gallium Oxide
- Conclusions

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The low surface dark current is
also a very important feature
of image sensors.

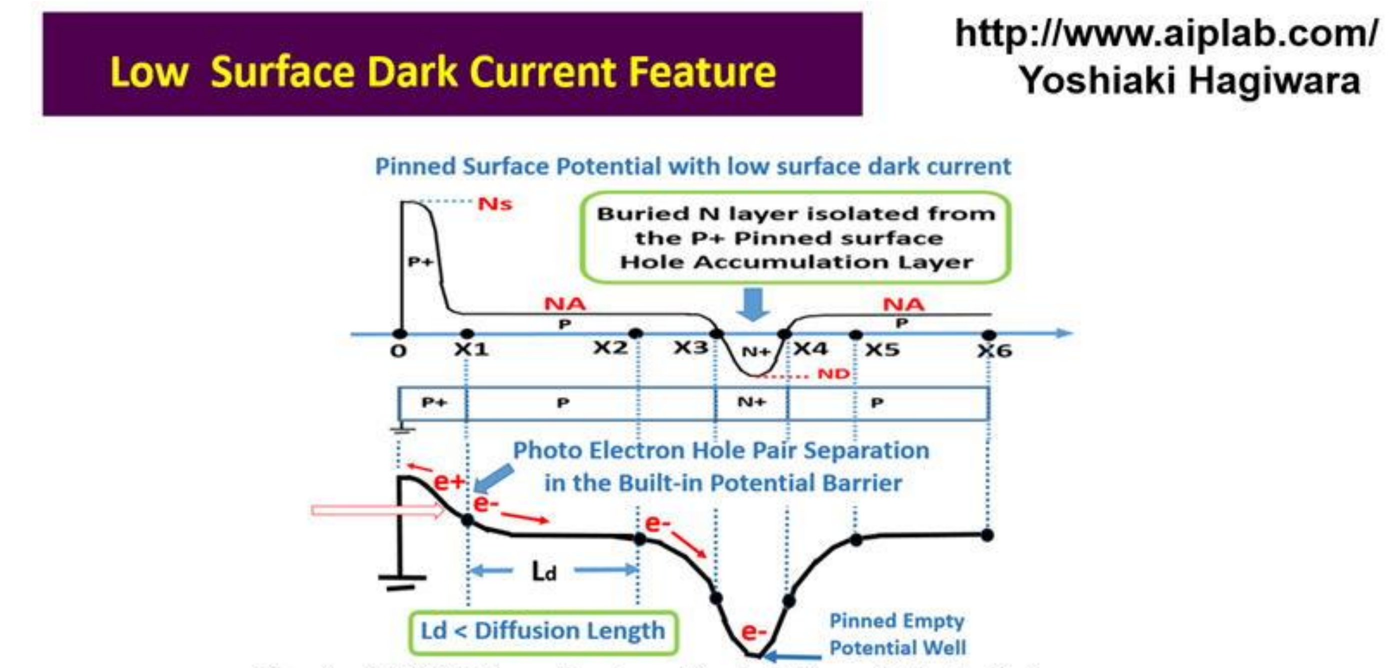

Fig. 5: P+PN+P junction type Buried Pinned Photodiode defined in Hagiwara Japanese 1975-127647 patent.

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The Figure 5 shows our proposed P+PN+P junction type Buried Depletion Pinned Photodiode. Normally the photo electron and hole pair generation and separation is performed in the electric field inside the depletion region of the PN junction or under the CCD/MOS capacitor.

But the photo electron and hole pair generation and separation of this P+PN+P junction Pinned Photodiode is different and quite unique.

The surface P+P impurity doping slope induces the built-in barrier potential and results in the built-in barrier electric field, enhancing the photo electron pair separation at the very near surface region of the silicon crystal to give the excellent blue light sensitivity.

This photo electron hole separation mechanism is unique, quite different from the usual photo electron hole pair separations in the normal PN junction depletion regions.

Simulation and the electrostatic analysis is based on the fact that the maximum depth for the blue light penetration into the silicon crystal is only 0. 2 micro meter in depth which is very close to the silicon crystal surface where we cannot have a shallow PN junction depletion region with the strong surface electric field causing the undesired surface dark current.

The life time of the photo generated minority carrier can be measured using the photoconduction effect and the diffusion length can be determined, which is needed for electrons to survive in the majority carrier hole-rich P substrate area. Most of the photo electrons are expected to reach the buried N charge collecting region.

Outline

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- Super Light Sensitivity Feature
- Low Surface Dark Current Feature
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- Schottky Barrier on Gallium Oxide
- Conclusions

Slide 23

No image lag is also a very important feature of image sensors.

No Image Lag Feature

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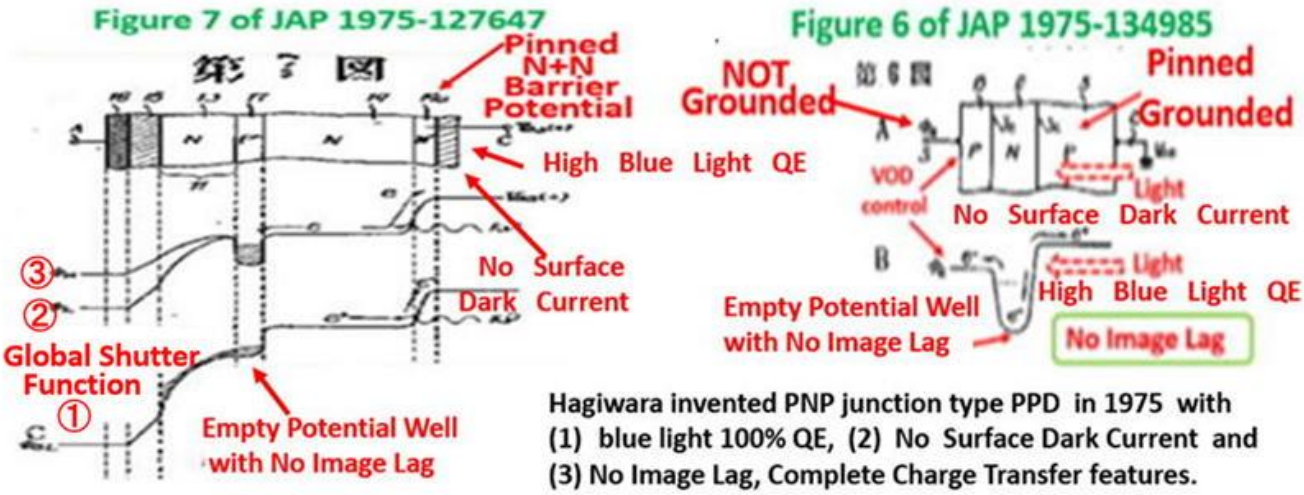

Hagiwara invented PNP junction type PPD in 1975 with (1) blue light 100% QE, (2) No Surface Dark Current and (3) No Image Lag, Complete Charge Transfer features.

Slide 24

The pinned photodiode originally invented in 1975 by Hagiwara have three important features.

They are,

Firstly, the excellent blue light sensitivity,

Secondly, the low surface dark current by the Pinned surface potential,

And thirdly the image lag free feature.

The empty potential wells

with the completely majority carrier depleted depletion region,

shown in these fugues are

the evidence that the Pinned Photodiode free of the image lag problem

was originally invented by Hagiwara at Sony in 1975.

No Image Lag Feature

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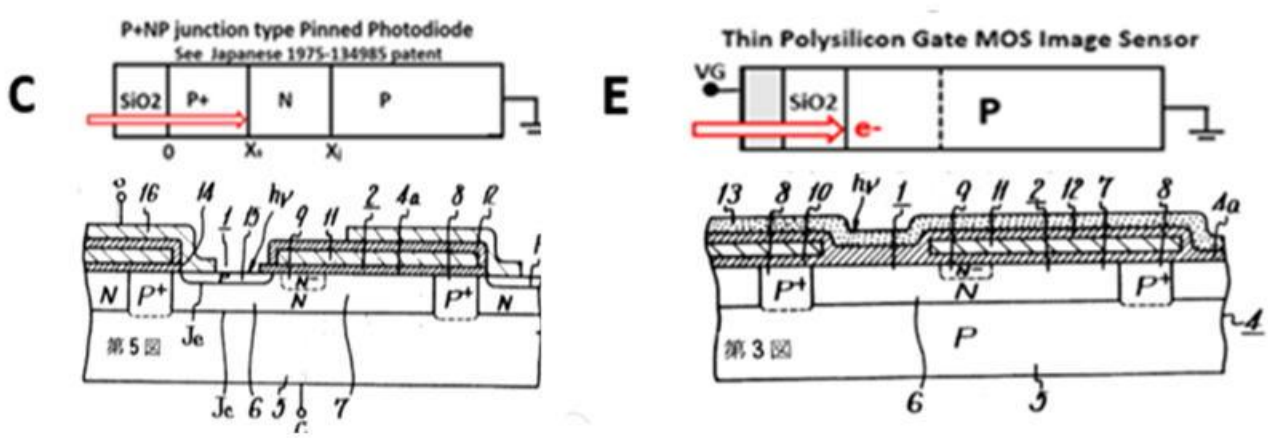

Fig. 6: Cross sectional views of Type C P+NP junction Pinned Photodiode sensor, Type E MOS capacitor photo sensor

Slide 25

Figure 6 shows the Cross sectional views of
the type C of the P+NP junction Pinned Photodiode sensor
and Type E of the MOS capacitor photo sensor in comparison.

Both structures do not have the image lag problems.

However, the Type C of the P+NP junction Pinned Photodiode sensor has,
in this example, the external metal contact pin as an option
to achieve the vertical overflow drain, that is, the VOD function.

But it is very clear that the surface P layer can be connected
to the adjacent P+ channel stops instead,
if the VOD function was not necessary.

In search for the low leakage and low dark current device,
related various historical silicon related photodiode structures
now have been reviewed.

Outline

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- Super Light Sensitivity Feature
- Low Surface Dark Current Feature
- No Image Lag Feature
- **Schottky Barrier on Gallium Oxide**
- Conclusions

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In search for the low leakage and low dark current device,

the Ga2O3 type semiconductor is

intensively being studied recently.

Schottky Barrier on Gallium Oxide

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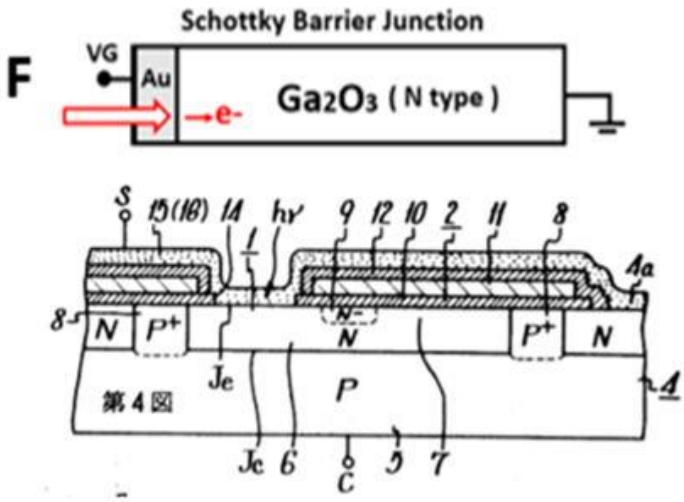

Fig. 6: Cross sectional view of Type F Schottky barrier photo sensor.

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The Cross sectional view the type F device

of the Schottky barrier photo sensor

is also shown in the figure 6.

The PN junction leakage is dependent on

the minority carrier density of

the semiconductor material itself.

Schottky Barrier on Gallium Oxide

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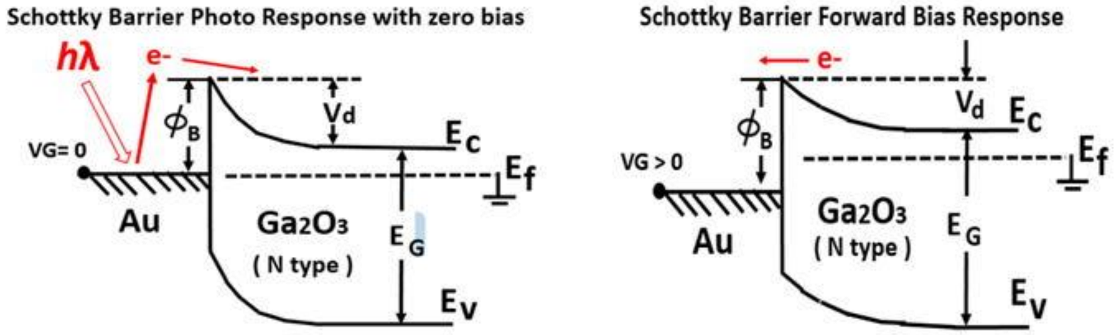

Fig. 7: Au/Ga2O3 Schottky Barrier Band Diagram

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Slide 28

The following slides show the early works

on the Ga2O3 Schottky Barrier

on Wide Bandgap Gallium Oxide

for the future low leakage image sensor applications.

This Figure 7 shows
the gold metal and Gallium Oxide Schottky Barrier Band Diagram

with the wide energy gap of 4.9 eV,

expecting a very low minority carrier density

and a very low leakage current device.

Schottky Barrier on Gallium Oxide

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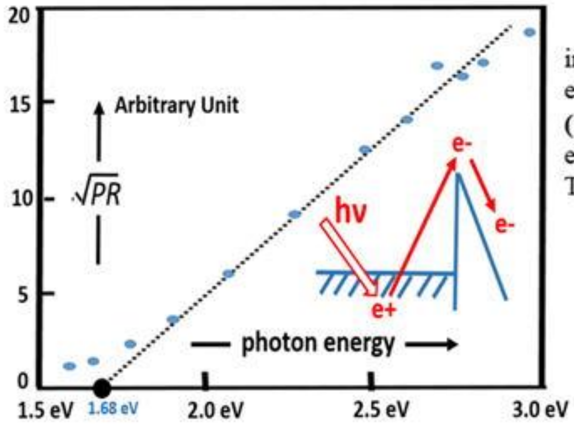

The square root of the photocurrent normalized to the incident photon flux when plotted as a function of the photon energy results in a straight line for photon energies above (Φ_B + 3 kT). The intercept for zero response of the extrapolated straight line yields a barrier height of 1.68 eV. Typical photo response data is presented in Fig. 8.

Fig. 8: Photo Response of Ga2O3-Au Schottky Barrier

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Figure 8 shows the typical Photo Response curve of

Ga2O3-gold metal Schottky Barrier.

The square root of the photocurrent normalized to

the incident photon flux

when plotted as a function of the photon energy

results in a straight line for photon energy.

The intercept for zero response of

the extrapolated straight line

yields a barrier height of 1.68 eV.

Schottky Barrier on Gallium Oxide

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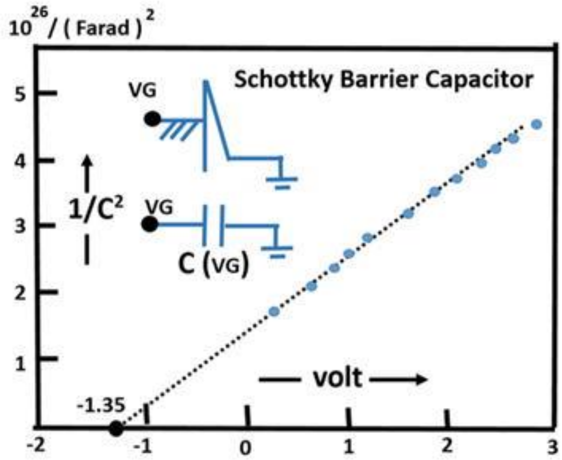

A typical plot of $1/C^2$ as a function of the reverse voltage is shown in Fig. 8. The concentration was found to be 4.1 ± 0.09 x 10^7 cm^{-3} from the slope using the relation:

$$N_d = \left(-2/q\varepsilon_{dc}\varepsilon_o \right)\left(\frac{\delta V}{\delta \left(\frac{S}{C} \right)^2} \right) \quad (1)$$

where S is the barrier area and ε_{dc} is the low frequency permitivity taken as 10.2 after Neville[5].

Fig. 9: CV measurement of Ga_2O_3-Au Schottky Barrier

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Figure 9 shows

the typical CV measurement of

Ga2O3-Gold Metal Schottky Barrier

with a typical plot of

one over C squared as a function of the reverse voltage.

The concentration was found to be

4.1 times 10 to the 7 th power per cubic cm from the slope.

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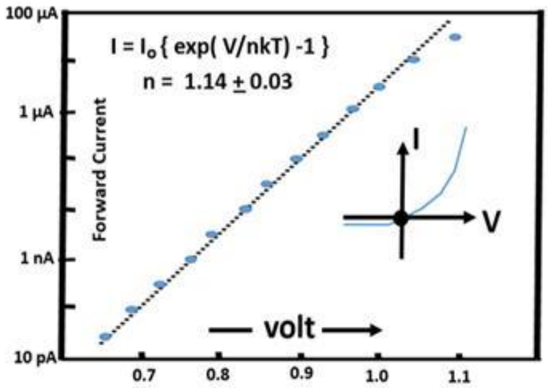

In Fig. 10, forward current characteristics are displayed at room temperature. The slope gives **q/nkT,** where **n** is the diode non-ideality factor, seen to be 1.14 ± 0.03, which is consistent with 1.08 ± 0.04 obtained by the capacitance-voltage method. The extrapolated current density at zero applied bias voltage is given by

$$J_o = A^* T^2 \exp\left(-\frac{q V_d}{nkT}\right) \tag{4}$$

where A * is the Richardson constant corresponding to the effective mass of the material taken as 0.2 $\mathbf{m_e}$. Using this equation the barrier height was found to be 1.69 ± 0.04 eV.

Fig. 10: IV measurement of Ga_2O_3-Au Schottky Barrier

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Figure 10 shows

the typical IV measurement of

Ga2O3-Gold Metal Schottky Barrier.

The forward current characteristics

are displayed at room temperature.

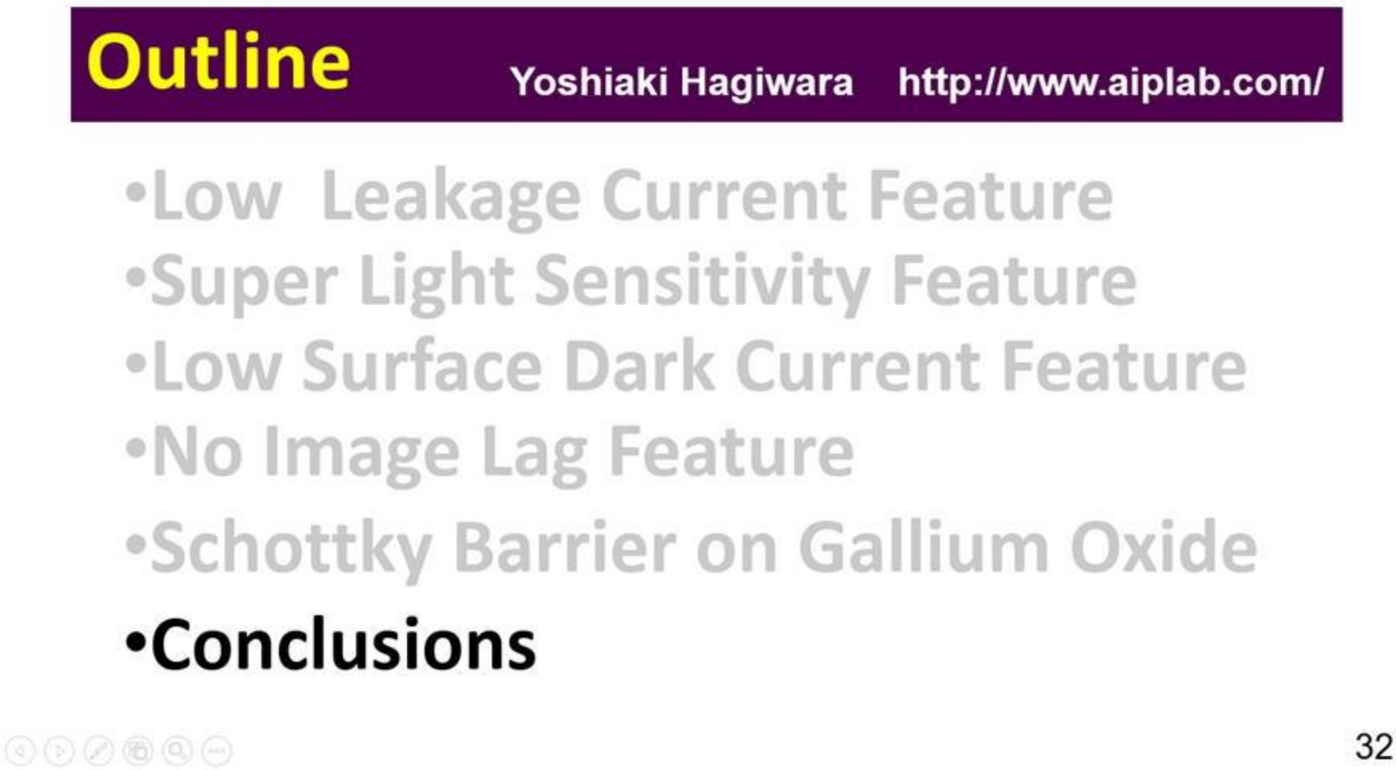
The slope gives q/nkT,

where n is the diode non-ideality factor,

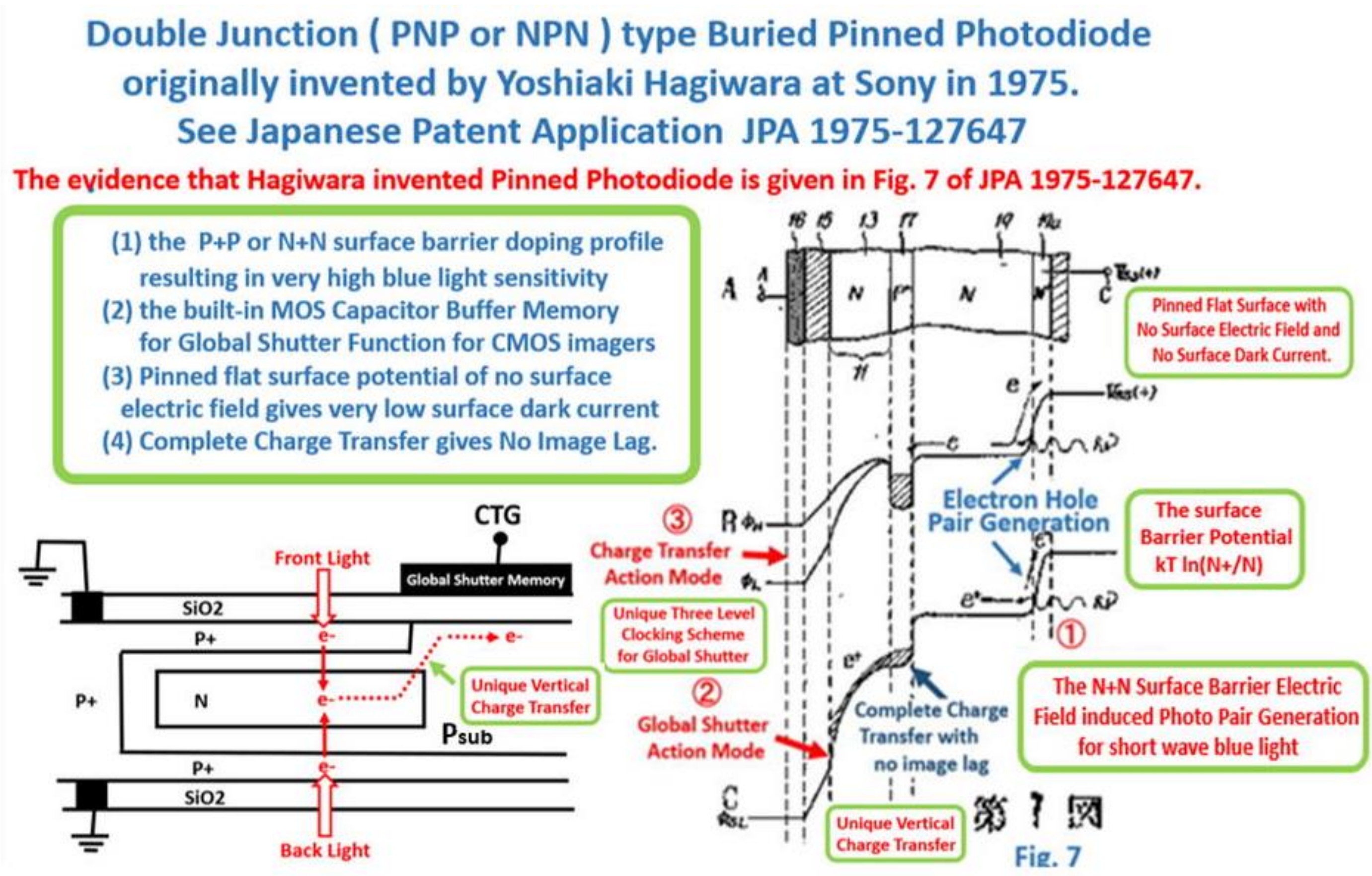
was found to be 1.14

which is close to the value of 1.08

obtained by the capacitance-voltage method.



Slide 32 now conclusion.....Before Hagiwara 1975 inventions, all image sensors were based on the single junction type floating N+P photodiode with the serious image lag problem or the CCD/MOS photo capacitor type with the very poor short wave blue light sensitivity and the large surface dark current noise.



Conclusions

The photo electron hole separation mechanism of the P+PNP junction type Pinned Photodiode was explained, which is unique and quite different from the conventional photo electron hole pair separation performed by the electric field inside the PN junction depletion region.

Related various historical photodiode structures are reviewed, including the 1971 work on the β- Ga2O3 Schottky barrier photo sensor in search for the low leakage dark current device which led to the 1975 invention of the Pinned Photodiode with the surface P+ heavily doped hole accumulation (HAD) with the vertical overflow drain (VOD).

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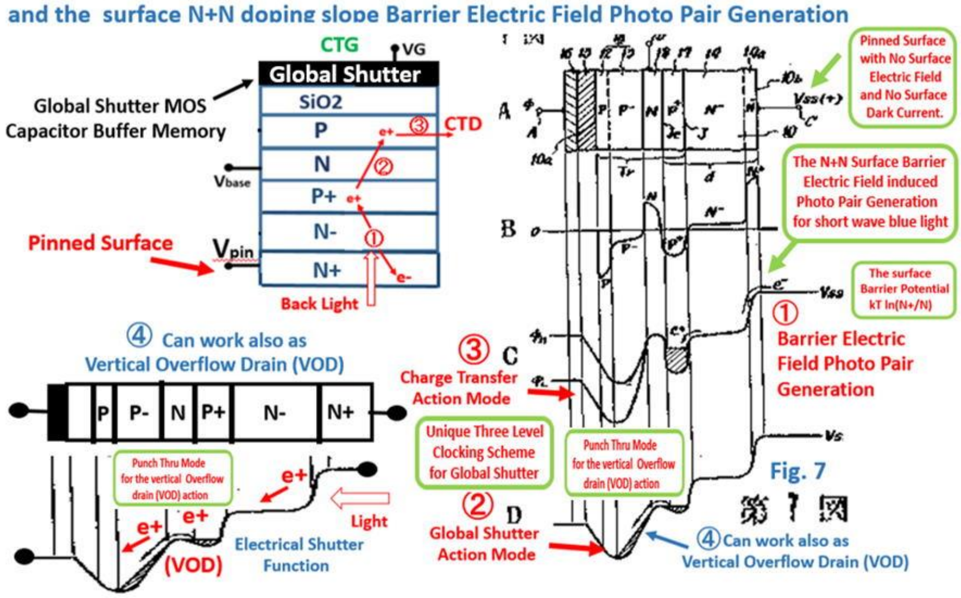
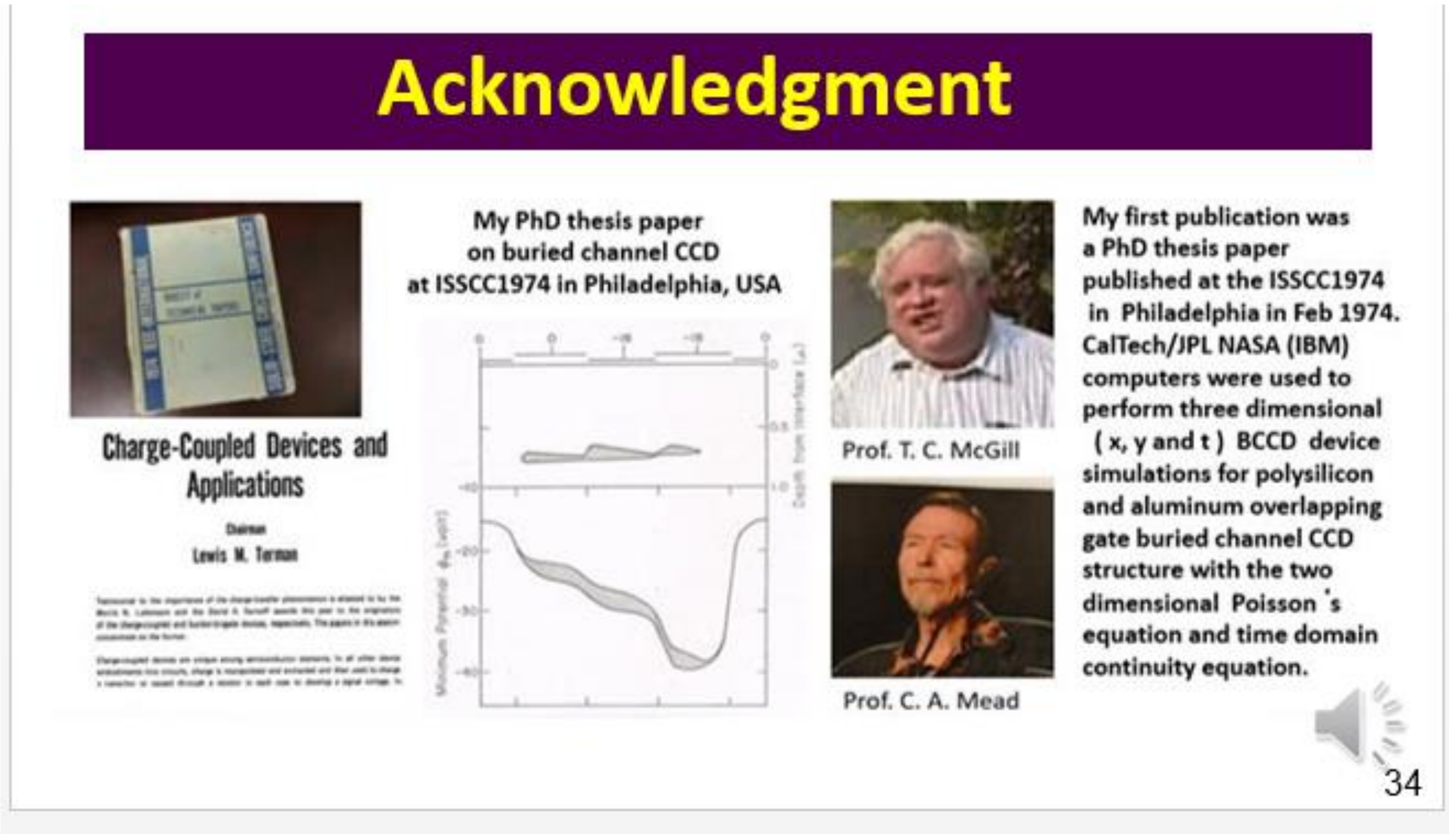
Slide 33 Conclusion.

Hagiwara proposed and invented in 1975 the double and triple junction type photo sensor as shown below with very excellent features including (1) an excellent short wave blue light sensitivity, (2) the very low surface dark current noise, (3) no serious image lag problem of the complete charge transfer capability shown by the empty potential well curve of the buried photo charge collecting storage region, (4) the triple junction photo thyristor with the punch-thru function that can be used for the VOD and the electrical shutter function and also (5) the in-pixel MOS capacitor buffer memory for the Global Shutter function needed in modern CMOS image sensors. Hagiwara also proposed in 1975 (6) Back light illumination type Pinned Photodiode as evidenced in the Japanese Patent Application 1975-127646.

Japanese Patent 1975-127646

Triple Junction N+N-P+NP-P junction type Buried Pinned Photodiode
with Built-in MOS Capacitor Buffer Memory Global Shutter Function
and the surface N+N doping slope Barrier Electric Field Photo Pair Generation

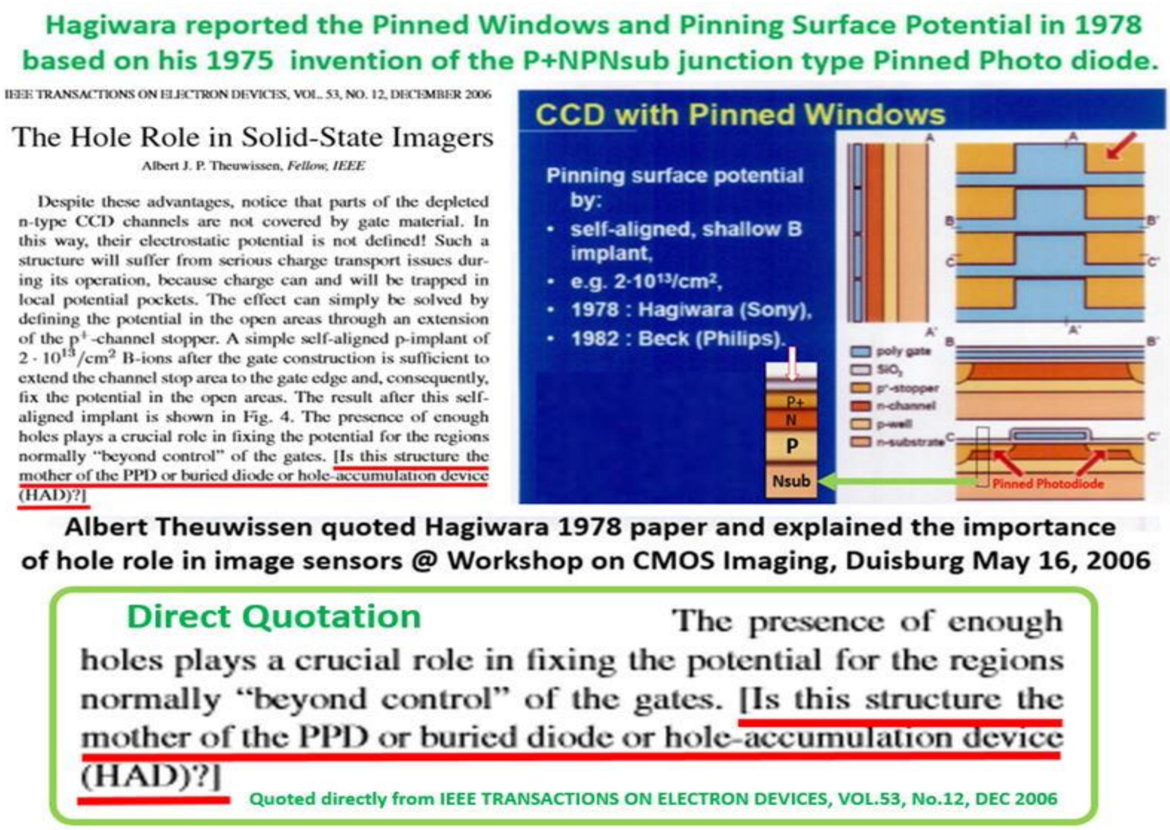




Slide 34

The author expresses sincere gratitude to Prof. C.A. Mead and Prof. T.C. McGill, for advising my original 1971 work at Caltech on the Ga2O3 – Au Schottky Barrier interface study and characterization, and also for guiding my original 1974 PhD thesis work. on the Charge Transfer Analysis of Buried Channel CCD Image sensors, Thank you very much.

Yoshiaki Hagiwara March 16 , 2020



To search page

1975-80
Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

~ Discrete Semiconductor/Others ~

https://www.shmj.or.jp/english/pdf/dis/exhibi1005E.pdf

Photodiodes are used for photodetectors of image sensors. In 1987, Sony introduced a 2 / 3-inch, 380,000-pixel CCD image sensor (ICX022) using a new type of photodetector, now called a Pinned Photodiode (Sony named it HAD: Hole Accumulation Diode)[1].

The Pinned Photodiode is a photodiode in which the entire N layer is covered with a P layer. The part of the P layer on the light incident surface is heavily doped P+ (Fig-1). Kodak named this structure Pinned Photodiode in 1984 because the P + surface of the light incident surface was pinned to the substrate potential. This device has features such as high light sensitivity, wide dynamic range, image lag free, much smaller dark current due to reduced influence of GR center on the light receiving surface, and no white scars.

In 1975, Sony proposed using a PNP transistor as the photodetector[3]. By providing a P + layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated, greatly improving the light sensitivity. This P + layer was also a proposal to reduce the dark current and image lag which became the basis of the pinned photodiode.

In 1978, Sony presented a 93,000-pixel FT (Frame Transfer) -CCD image sensor compliant with the Analog TV Broadcasting Standard (SDTV) for the first time in the world[5], using the photodiode with the same structure as above. Sony succeeded in 1981 in trial production of a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor by further improvement of this technology[6].

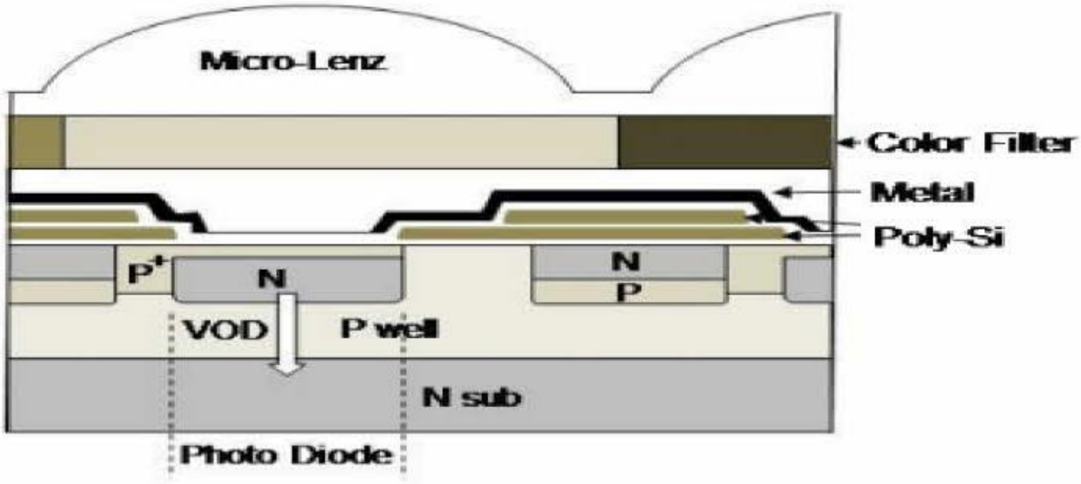


Fig-1 Recent Image Sensor with Pinned Photodiode

References:

【1】M. Hamasaki, T. Suzuki, Y. Kagawa, K. Ishikawa, K. Miyata and H. Kambe, "An IT-CCD imager with electronically variable shutter speed", Technical Report of The Institute of Image Information and Television Engineers. vol. 12, no. 12, pp. 31-36, (1988)

【3】Y. Hagiwara, Japanese Patent JP1975—134985

【5】Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978): Japanese Journal of Applied Physics, vol. 18, Supplements 18-1, pp. 335-340, (1979)

【6】I. Kajino, M. Shimada, Y. Nakada, Y. Hirata and Y. Hagiwara, "Single Chip Color Camera Using Narrow channel CCD Imager with Over Flow Drain", Technical Report of The Institute of Image Information and Television Engineers, vol. 5, no. 29, pp.

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Sony's Representative Inventions Supporting Stacked Multi-Functional CMOS Image Sensors

Sony Corporation
Sony Semiconductor Solutions Corporation

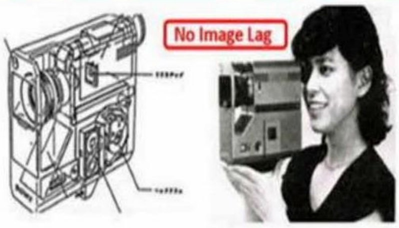
https://www.sony.net/SonyInfo/News/notice/20200626/

Pinned Photodiode Adopted for Back-Illuminated CMOS Image Sensors

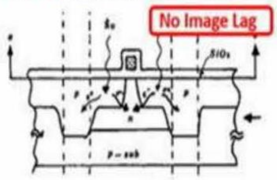
The history of Sony's inventions of image sensors goes back to the CCD era. Above all, Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development are as below.

In 1975, Sony invented a CCD image sensor that adopted a back-illuminated N+NP+N junction type and an N+NP+NP junction type Pinned Photodiode (PPD) (Japanese patent application number 1975-127646, 1975-127647 Yoshiaki Hagiwara). In the same year, inspired by such structure, Sony invented a PNP junction type PPD with VOD (vertical overflow drain) function (Japanese Patent No. 1215101 Yoshiaki Hagiwara). After that, Sony succeeded in making a principle prototype of a frame transfer CCD image sensor that adopted the PNP junction type PPD technology, having a high-impurity-concentration P+ channel stop region formed near a light receiving section by ion implantation technology for the first time in the world, and its technical paper was presented at the academic conference, SSDM 1978 (Y. Hagiwara, M. Abe, and C. Okada, "A 380H x 488V CCD imager with narrow channel transfer gates", Proc. The 10th Conference on Solid State Devices, Tokyo, (1978)). In 1980, Sony succeeded in making a camera integrated VTR which incorporated a one-chip frame transfer CCD image sensor that adopted the PNP junction type PPD. President Iwama in Tokyo, Chairperson Morita in New York, at the time held a press conference respectively on the same day, which surprised the world. In 1987, Sony succeeded in developing a 8 mm video camcorder that adopted, for the first time in the world, the interline transfer CCD image sensor, which incorporated "PPD having a high-impurity-concentration P+ channel stop region formed near the light receiving section by ion implantation technology" with VOD function, and became the pioneer of the video camera market. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors.

Sony original 570H x 498 V one-chip FT CCD Image Sensor with Pinned Photodiode, July 1980



P+NP Junction Pinned Photodiode



On July 1980, Iwama Kazuo at Sony Tokyo Press Conference and Morita Akio at New York Press Conference announced the one chip CCD video camera with the 8 mm VTR in one box.

See the Original 1978 Publication of the Pinned Photodiode Sensor

Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates," Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Apllied Physics, vol. 18, supplement 18–1, pp. 335–340, 1979

High quality picture of SONY CMOS Imager is also based on SONY HAD (Pinned Photodiode).

These figures shows (1) Excellent Blue Light Sensitivity (2) Low Surface Dark Current and (3) NO Image Lag Features of the P+NP junction type Pinned Photodiode.

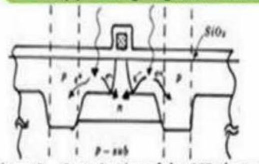
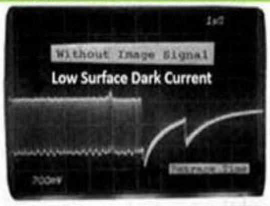


Figure 2 Cross Section of the CCD charge Transfer Region with the P+NP junction type Pinned Photodiode (PPD)



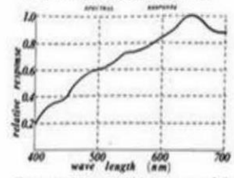


Figure 13 Spectral Response of the P+NP junction Pinned Photodiode (PPD) with the excellent blue light sensitivity

Figure 14 Comparison of CCD image sensor output signals with and without image signal.

Pinned Photodiode and Sony Hole Accumulation Diode (HAD)

PNPN junction Transistor type Pinned Photodiode

Visit https://www.j-platpat.inpit.go.jp/ and put the patent number 1975-134985

File	1975-134985	Filed	1975/11/10
Public	1975-058414	Public	1977/05/13
		Grant	1983/10/19

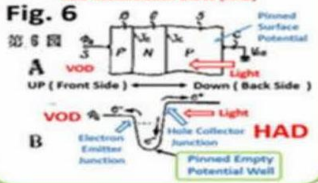
Patent Claim in English Translation

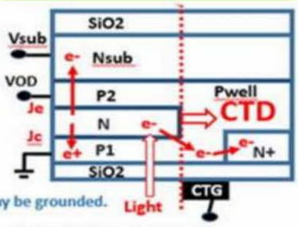
(1) In the semiconductor substrate (Nsub), the first region(P1) of the first impurity type is formed, (2) on which, the second region (N) of the second impurity type is formed. (3) The charge (e-) from the light collecting part (N) is is transferred to the adjacent charge transfer device (CTD). (4) Both are placed along the main surface of the semiconductor substrate. (5) In the solid stare image sensor so defined, a rectifying Emitter junction (Je) is formed on the second region (N) of the light collecting part (N) . And (6) Collector junction (Jc) is formed by the second region (N) and the first region (P1), forming a transistor structure (P2NP1) (7) Photo charge is stored in the Base region (N) according to the illuminated light intensity, and transferred to the adjacent CTD. The solid state image sensor so defined is in the scope of this patent claim.

Japanese Patent 1975-134985

Hole Accumulation Diode (HAD)

Fig. 6





VOD may be grounded.

Yoshiaki Hagiwara, Japanese Patent JP 1975-134985

Pinned Photodiode defined in JPA 1975-127647 by Hagiwara in 1975

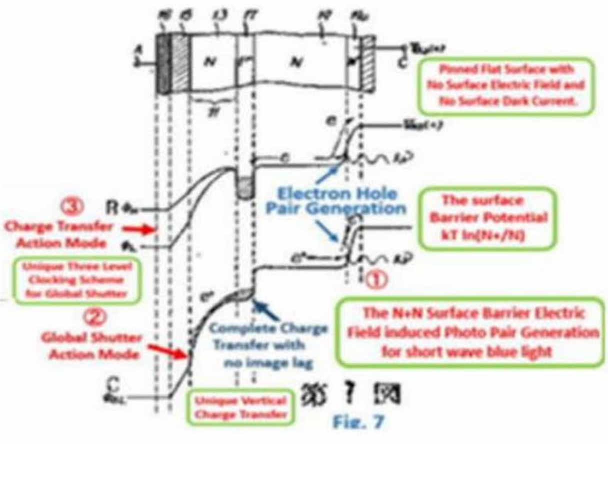


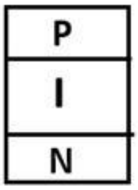
Fig. 7

Difference between Buried Photodiode and Pinned Photodiode

What is the difference between Buried Photodiode and Pinned Photodiode? I understand that the P+/N/P structure where the P+ and P layers have the same potential is the Pinned Photodiode. So what is the buried Photodiode?

https://electronics.stackexchange.com/questions/83018/difference-between-buried-photodiode-and-pinned-photodiode

PIN diode



In 1975 the first PPD was invented by Hagiwara at Sony and used in ILT CCD PDs by Hamazaki at Sony in 1987.

PPD must have the P+ channel stops nearby to pin the surface P+ layer.

This is a commonly misunderstood misused set of terminologies.

First off these are not PIN Photodiodes - which stands for P - Intrinsic- N. These have large depletion regions for higher internal QE (Quantum Efficiency) and faster response. You can't make an array with this design though.

Pinning, refers to fermi-level pinning or pinning to a certain voltage level. Or also the forcing or prevention of the fermi-level/voltage from moving in energy space.

You can get surface state pinning from the dangling Si/SiO2 bonds providing trapping centers. A buried PD (Photodiode) has a shallow implant that forces the charge carriers away from these surface traps. The Si/SiO2 surface contributes to increased leakage (dark current) and noise (particularly 1/f noise from trapping/de-trapping). So confusingly a buried PD avoids pinning of the fermi-level at the surface.

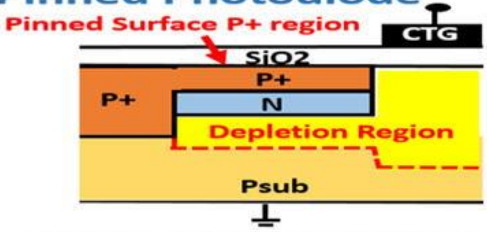
A pinned PD is by necessity a buried PD, but not all buried PD's are pinned. The first Pinned PD was invented by Hagiwara at Sony and is used in ILT CCD PD's, these same PD's and the principles behind this complete transfer of charge are used in most CMOS imagers built today.

A pinned PD is designed to have the collection region deplete out when reset. AS the PD depletes it becomes disconnected from the readout circuit and if designed properly will drain all charge out of the collection region (accomplishing complete charge transfer). An interesting side effect is that the capacitance of the PD drops to effectively zero and therefore the KTC noise $q_n = sqrt(KTC)$ also goes to zero. When you design the depletion of the PD to deplete at a certain voltage you are pinning that PD to that voltage. That is where the term comes from.

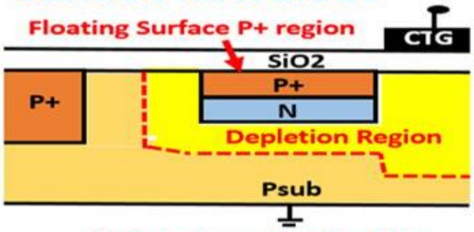
I've edited this Answer to acknowledge Hagiwara-san's contribution. It has long been incorrectly attributed to Teranishi and to Fossum (in CMOS image sensors)

Difference of Buried Photodiode and Pinned Photodiode

Pinned Photodiode

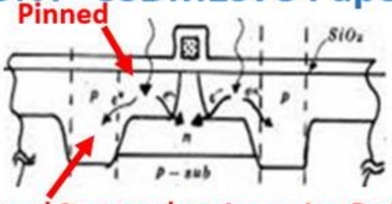


Buried Photodiode

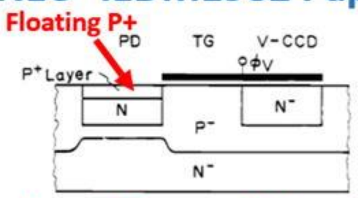


Serious Image Lag Problem

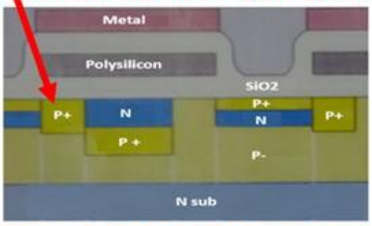
SONY SSDM1978 Paper



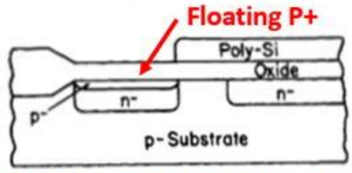
NEC IEDM1982 Paper



P+ Channel Stops and no Image Lag Problem



No P+ Channel Stops and Serious Image Lag



SONY 1987 HAD Sensor

KODAK IEDM1984 Paper

Sony Image Sensors do not use the LOCOS process of serious oxidation-stress induced defects and the possible isolation of the surface P+ hole accumulation layer from the the channel stops under the LOCOS.

Fossum insulted in his 2014 paper Sony and Hagiwara 1975 PPD invention.

Indeed, Hagiwara invented PPD with VOD and the virtual charge transfer in 1975 !!

IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY, VOL. 2, NO. 3, MAY 2014 33

Sony HAD (PPD+VOD) does not use LOCOS !!!

A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, Fellow, IEEE, and Donald B. Hondongwa, Student Member, IEEE

Many people now said this is a fake paper !

C. Other Contributions to the PPD Invention

False

The PPD structure, while invented for low lag ILT CCD application, shares a strong resemblance to the Hynecek virtual-phase CCD structure, with the exception of the VOD. The two inventions were solving different problems with essentially the same device structure and operating principles.

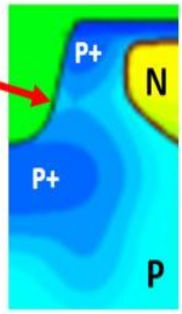
In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top *p* layer was connected by metal to a bias used to control full-well capacity and the *n*-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called "Hole Accumulation Diode," or HAD structure [25]. However, the 1975 application

False

did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the "narrow-gate" CCD with an open *p*-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

The PPD, as it is most commonly used today, bears the strongest resemblance to the Teranishi et al. ILT CCD device. Thus, these days Teranishi is considered as the primary inventor of the modern PPD [29].

The surface P+ layer is NOT connected to the LOCOS P+ layer. The surface P+ layer may be floating and this photodiode may have serious image lag.



Serious Image Lag ?

NOT connected

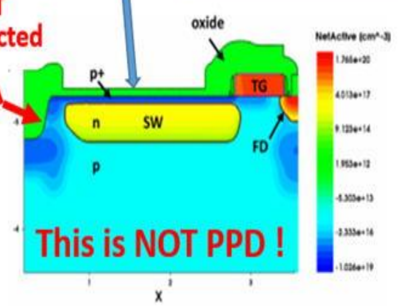
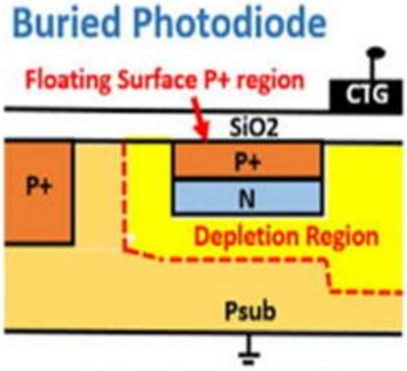


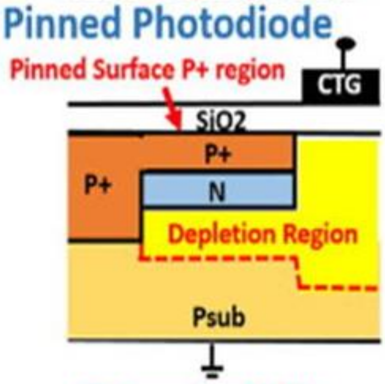
Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

Hagiwara in 1975 invented PPD with VOD and the virtual charge transfer. Study the Japanese Patents 1975-127646, 1975-127647 and 1975-134985.

Pinned Photodiode Must Have the Grounded P+ Channel Stops Nearby.



Serious Image Lag Problem



No Image Lag Problem

The resistivity ρ of the P+ hole accumulation layer is given by

$$\rho = R * W * d / L$$

In the 2/3 inch optical lens system, we have the optical image size of 8.8 mm (H) x 6.6 mm (V) which was a common size in 1980s. Hence, we then have L = 6.6 mm = 6600 μm

The short wave blue light cannot penetrate more than d = 0.2 μm into the silicon crystal in depth. Hagiwara reported in SSDM1978 paper $Qd = 2 \times 10^{13} cm^{-2}$ which gives $Nd = Qd/d = 1 \times 10^{18}\ cm^{-3}$

For $Nd = 1 \times 10^{18}\ cm^{-3}$ we have ρ = 0.04 ohm cm = 400 ohm μm

$$RC = \{ L\rho / (W^*d) \} \{ \varepsilon W^*L / Xo \} = \varepsilon \rho L^2 / (d\ Xo)$$

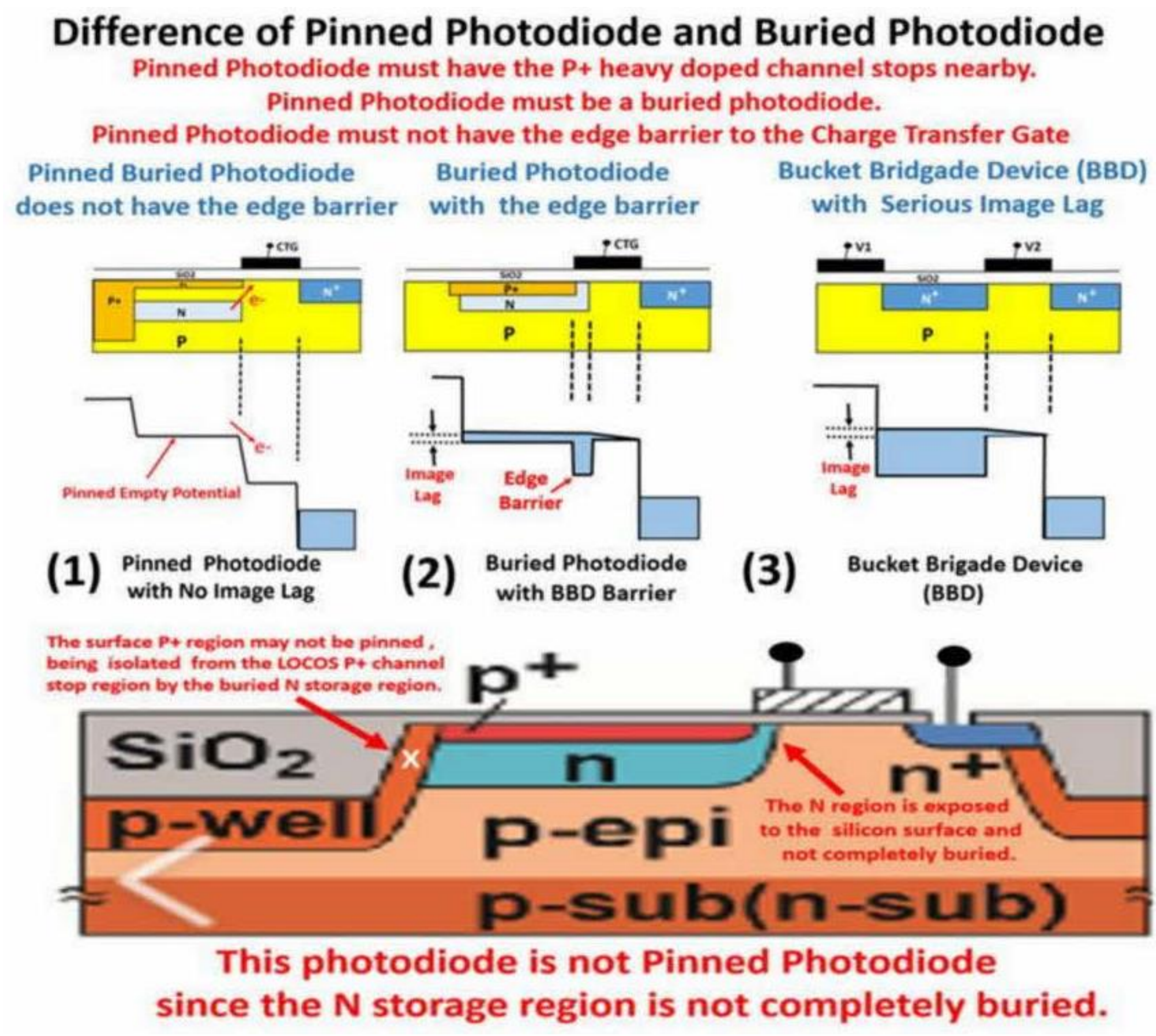
We have ε = 216 e/volt μm for silicon oxide and $e = 1.6 \times 10^{-19}$ Coulomb

$$RC = (216)(1.6 \times 10^{-19})(400)(6600)(6600) / (0.2)/(0.1) \ \text{sec}$$

RC = 30.1 μsec while one frame is 1/60 sec = 16.7 msec and the Vertical CCD register clock period is 16.7/500 = 33.4 μsec

Hence RC delay time may not be ignored and surface P+ may be floating ?

Photodiode with Serious Image Lag is NOT a Pinned Photodiode by definition ???



In the SSDM1978 paper, Yoshiaki Hagiwara at SONY reported the P+NP double junction dynamic photo transistor used in a Frame Transfer CCD image sensor. Hagiwara is the true inventor and also the pioneering developer of the P+NP double junction dynamic photo transistor, which was called differently by NEC1982, KODAK1984 and SONY1987. The problem is that, NEC, KODAK and even Sony1987 HAD product announcement did not quote Hagiwara's original 1975 inventions and Hagiwara SSDM1987 important works, which reported the P+NP double junction dynamic photo transistor, originally invented by Hagiwara in 1975. Evidence is shown in Hagiwara's Japanese Patent Applications, JPA1975-127646, 1975-127646 and 1975-1234985. Examine these important evidence. Then, you will see that Yoshiaki Hagiwara, at Sony in 1975, is the true inventor of the Buried Photodiode reported in the NEC IEDM 1982 paper, the Pinned Photodiode reported in the KODAK IEDM1984 paper, and the Sony 1987 Hole Accumulation Diode (HAD). They are all the same thing that Hagiwara invented in 1975. Before Hagiwara 1975 inventions, all image sensors were based on the floating N+P single junction type photodiode with the serious image lag or the CCD/MOS type photo capacitor with the serious surface dark current and the very poor blue light sensitivity.

Acknowledgment

Yoshiaki Hagiwara http://www.aiplab.com/

The author expresses sincere gratitude to Prof. C.A. Mead and Prof. T.C. McGill, for advising my original 1971 work at Caltech on the Ga2O3 – Au Schottky Barrier interface study and characterization, and for guiding my 1974 PhD thesis work on the Charge Transfer Analysis of Buried Channel CCD Image sensors, and also, Yoshiyuki Kawana and Toshio Kato for supporting my original 1978 work at Sony on the P+PNP junction type Pinned Photodiode. They are my dear friends and respectful mentors throughout my private and public life.

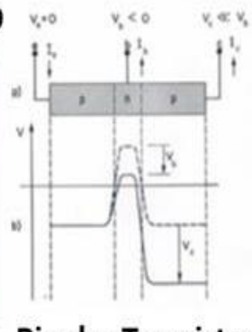
Thank You !

35

In Memory of Prof._T_C_McGill_and Prof. James_McCaldin at Caltech in,1998

with Prof. James McCaldin @Newport Beach

Feynman Physics 1967-1969



Bipolar Transistor

with Prof. Tom McGill @Caltech Campus